POWER MANAGEMENT

Design Parameters

Assumptions: The calculations in this document assume that V5V = 5V and electrolytic capacitors are used at the output.

- V_{IN} = 12V +/-5%
- V_{OUT} = 1V
- I_{OUT} = 6A

Switching Frequency (f_{SW})

Setting the switching frequency is a trade-off between efficiency, size, and cost of inductor and filter capacitors. A frequency of 250kHz will be used in this example.

R_{TON} Selection

The SC414 is a constant-on-time architecture, therefore frequency is set indirectly. The on-time is set using the duty cycle (D) governing the buck regulator input/output relationship, the frequency is determined.

$$D = \frac{t_{ON}}{T}$$

For a buck regulator:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Rearranging the equations results in the following equation.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times T$$

$$t_{ON} = \frac{1V}{12V} \times \frac{1}{250kHz} = 333ns$$

The following equation is used to set R_{TON}.

$$R_{TON} = \frac{1}{25pF \times f_{SW}} - 400\Omega \times \frac{V_{IN}}{V_{OUT}}$$

$$R_{TON} = \frac{1}{25pF \times 250kHz} - 400\Omega \times \frac{12V}{1V} = 155.2k\Omega$$

The closest 1% value to 155.2kΩ is 154 kΩ.

Choosing Input Capacitors

Input capacitors are used to provide energy to the power stage quickly when the high side FET turns on and to reduce the peak currents drawn from the input power source. The ripple current rating of the input capacitors must meet or exceed I_{RMS} ripple caused by the switching currents. The ripple current generated is calculated using the following equation.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = 6A \times \frac{\sqrt{1V \times (12V - 1V)}}{12V} = 1.658A$$

Because of their low ESR and ESL, ceramic capacitors are typically used. High quality dielectric capacitors should be used (for example X5R or X7R). As the rated current varies with both DC bias and temperature, the capacitors need to be checked to ensure specifications are not violated.

For example, a 1206 10μF 16V capacitor with an X5R dielectric has an allowable ripple current at 25 °C and 250 kHz at 4.2A. At 80°C, the allowable ripple current goes down to 2.1A. As long as the ambient temperature remains below 80 °C, a single ceramic capacitor is sufficient for this design example.

The effective capacitance of ceramic capacitors varies under DC bias and temperature. When using the above capacitor and a 12 V input, the effective capacitance can be 50% of the original value or lower (e.g. with a 12V bias the effective capacitance is ≤5μF). While a single capacitor is sufficient to handle the ripple current, additional ceramic capacitors or bulk capacitors may be needed to provide local energy storage and a low impedance input source to account for any PCB or input connector impedances.

Inductor Selection:

The output inductor should be selected based on cost, size, output ripple, and efficiency. Selecting a ripple current between 25% and 50% of the maximum output load current will provide an optimal trade-off between the above selection criteria. LIR is defined as the inductor current ratio expressed as a percentage of I_{OUT}.

This example uses 40% as the value for LIR.

$$I_{RIPPLE} = I_{OUT} \text{ x LIR}$$

$$I_{RIPPLE} = 6A \text{ x } 40\% = 2.4A$$

The differential equation for an inductor is shown by the following equation.

$$V = L \times \frac{di}{dt}$$

The above equation uses the following; $V = V_{IN} - V_{OUT}$; $di = I_{RIPPLE}$; and $dt = t_{ON}$.

The equation rearranged and calculated is:

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

$$L = \frac{(12V - 1V) \times 333ns}{2.4A} = 1.528\mu H$$

The closest standard value for L_{OUT} is 1.5µH. I_{RIPPLE} should be recalculated with the chosen L_{OUT} to minimize calculation error as shown by the following equation.

$$I_{RIPPLE} = \frac{(12V - 1V) \times 333ns}{1.5\mu H} = 2.4A$$

As the DC current is increased in an inductor, the amount of inductance decreases. When the inductance has decreased to 80% of its initial value due to the increase of DC current, the value of DC current is called I_{SAT}. When selecting an inductor, it is important to not exceed the I_{SAT}

rating. To figure out what minimum I_{SAT} current to select, the following equation is used.

$$I_{SAT} \geq I_{OUT} + \frac{I_{RIPPLE}}{2}$$

$$I_{SAT} \geq 6A + \frac{2.4A}{2}$$

This example shows that the I_{SAT} rating of the inductor needs to be greater than 7.2A.

Setting Current Limit

The current limit is set by comparing the voltage generated by a 8µA current source across the I_{LIM} resistor to the voltage drop across the low side FET during the off time. This represented by the following equation.

$$R_{LIM} = 1250 \text{ x } I_{LIM}$$

For a 6A load current limit, R_{LIM} is shown by the following equation.

$$R_{LIM} = 1250 \times \frac{\Omega}{A} \times 6A = 7.6k\Omega$$

The closest 1% resistor is 7.5kΩ.

Setting the Output Voltage

The regulator output is set by comparing the voltage at the feedback pin to an internal reference of 750mV. The voltage at the feedback pin is V_{OUT} through a resistor divider.

The top resistor of the divider (R1) is selected and the bottom resistor is calculated using the following equation.

$$R2 = \frac{R1 \times V_{FB}}{V_{OUT} - V_{FB}}$$

For our example, we will use R1 = 10kΩ, 1%. The bottom resistor (R2) is calculated using the following equation.

$$R2 = \frac{10k\Omega \times 0.75V}{1V - 0.75V} = 30k\Omega$$

The closest 1% value is 30.1kΩ.

The control method used for the SC414 regulates to the valley of the ripple voltage, so the DC output voltage is actually offset high by one half of the ripple voltage. Therefore, the output voltage is calculated by the following equation where $V_{FB} = 0.75V$.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) + \frac{V_{RIPPLE}}{2}$$

Output Capacitor Selection

Output capacitors are chosen based on the desired output ripple (minimum and maximum) and transient response requirements.

The architecture of the SC414 as a constant on-time regulator requires a minimum amount of ripple at the feedback pin to maintain stable operation. Unstable operation is avoided by maintaining >10mV of ripple at the feedback pin.

The amount of ripple seen at the feedback pin will be a fraction of the output ripple, as set by the feedback voltage divider.

$$V_{RIPPLE\_FB} = V_{RIPPLE} \times \frac{R2}{R1+R2}$$

Rearranging this equation gives the minimum amount of ripple required at the output.

$$V_{RIPPLE} = V_{RIPPLE\_FB} \times \frac{R1+R2}{R2}$$

$$V_{RIPPLE} = 10mV \times \frac{30k\Omega + 10k\Omega}{30k\Omega} = 13mV$$

Therefore the minimum ripple is 13mV.

Since the SC414 regulates to the valley, the DC tolerance of the output is affected by the ripple voltage. Therefore, to maintain DC tolerance there is a maximum placed on the ripple voltage. Other factors influencing the DC tolerance are the reference tolerance and the feedback resistor tolerance. The reference tolerance of the SC414 is +/- 1%. Since 1% resistors are used for the feedback network, the impact to overall tolerance from the feedback network is 0.64%. This example uses a desired DC tolerance of +/-4%.

$$DC_{TOL} = V_{RIPPLE\_TOL} + REF\_tol + Resistor\_tol$$

Rearranging and calculating for ripple current is shown by the following equation.

$$V_{RIPPLE\_TOL} = DC_{TOL} - (Ref\_tol + Resistor\_tol)$$

$$V_{RIPPLE\_TOL} = 4\% - (1\% + 0.64\%)$$

$$V_{RIPPLE\_TOL} = 2.36\%$$

To calculate the allowable ripple the V_{RIPPLE_TOL} number must be doubled because the error comes from ½ of the ripple voltage. Therefore the maximum allowable ripple is shown by the following equation.

$$V_{RIPPLE\_MAX} = V_{OUT} \times (2 \times V_{RIPPLE\_TOL})$$

$$V_{RIPPLE\_MAX} = 1V \times (2 \times 2.36\%_I) = 0.047V$$

The ripple voltage seen on the output is usually dominated by the ESR of the capacitor, with capacitance adding some amount to the ripple. V_{RIPPLE} is calculated using the following equation.

$$V_{RIPPLE} = V_{CESR} + V_C$$

$$V_{CESR} = I_{RIPPLE} \times C_{ESR}$$

$$V_C = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}$$

For this example a 220µF, 9mΩ capacitor is selected and the resulting ripple is calculated using the following equation.

$$V_{CESR} = 2.4A \times 9m\Omega = 22mV$$

$$V_C = \frac{2.4A}{8 \times 220\mu F \times 250kHz} = 6mV$$

$$V_{RIPPLE} = 22mV + 6mV = 28mV$$

This example shows that the ripple resulting from using the chosen capacitor is less than the maximum ripple allowed to maintain DC tolerance.

The amount of output capacitance also affects the size of the transient during load step and load release.

During load release, where the di/dt is unknown, the worst case overshoot transient can be approximated with the following equation.

$$V_{OVER} = \sqrt{\frac{L_{OUT} \times I_{PEAK}^2}{C_{OUT}} + V_{OUT}^2} - V_{OUT}$$

$$I_{PEAK} = I_{SAT} = I_{OUT} + \frac{I_{RIPPLE}}{2}$$

I_{PEAK} is the same value as the minimum I_{SAT} calculated before (7.2A).

The voltage overshoot for our example is as follows:

$$V_{OVER} = \sqrt{\frac{1.5\mu H \times (7.2A)^2}{220\mu F} + (1V)^2} - 1V = 0.163V$$

The maximum DC voltage seen will be 1.184V ($V_{OVER} + V_{OUT} + V_{RIPPLE}/2$). This assumes a load release from full load to no current.

$$V_{PEAK} = V_{OVER} + V_{OUT} + \frac{V_{RIPPLE}}{2}$$

$$V_{PEAK} = 163mV + 1V + \frac{28mV}{2} = 1.184V$$

If the maximum overshoot is known, the previous equation can be arranged to figure out the minimum C_{OUT} to meet the overshoot requirement.

$$C_{OUTMIN} = \frac{L_{OUT} \times I_{PEAK}^2}{V_{PEAK}^2 - V_{OUT}^2}$$

If the di/dt is known, the following equation can be used to calculate the minimum required output capacitance.

$$C_{OUT} = I_{STEP\_PEAK} \times \frac{L \times \dfrac{I_{STEP\_PEAK}}{V_{OUT}} - I_{STEP} \times \dfrac{dt}{di}}{2(V_{PEAK} - V_{OUT})}$$

Where I_{STEP_PEAK} for this equation is shown by the following.

$$I_{STEP\_PEAK} = I_{STEP} + \frac{I_{RIPPLE}}{2}$$

Note that for this equation the peak current is only important as it relates to the size of I_{STEP}, not the full load peak current.

The next example uses a full load release, and overshoot voltage of 100mV, as shown by the following equations.

$$I_{PEAK} = 3A + \frac{2.4A}{2} = 4.2A$$

$$C_{OUT} = 4.2A \times \frac{1.5\mu H \times \dfrac{4.2A}{1V} - 3A \times \dfrac{1\mu s}{1A}}{2(1.1V - 1.0V)} = 39.2\mu F$$

Either a single 150μF or a single 220μF capacitor can be used for this example.

To approximate the undershoot caused by a load step the following formula is used.

$$V_{UNDER} = \frac{L_{OUT} \times I_{STEP}^2}{2 \times C_{OUT} \times D_{MAX} \times (V_{IN} - V_{OUT})}$$

For the SC414, the duty cycle ratio changes during a load step by modulating the off-time and maintaining the on-time. As long as the feedback voltage is below the reference, the off time is kept at a minimum. Therefore, D_{MAX} in the above equation can be calculated using the following equation.

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

Where t_{ON} equals the value calculated above and t_{OFF_MIN} (500nS) is shown by the following equation.

$$D_{MAX} = \frac{333ns}{333ns + 500ns} = 0.40mV$$

The result for the V_{UNDER} calculation is shown by the following equation.

$$V_{UNDER} = \frac{1.5\mu H \times (6A)^2}{2 \times 220\mu F \times 0.40 \times (12V - 1V)} = 7mV$$

The minimum DC voltage measured is shown by the following equation.

$$V_{OUTMIN} = V_{OUT} + \frac{V_{RIPPLE}}{2} - V_{UNDER}$$

$$V_{OUTMIN} = 1V + \frac{13mV}{2} - 7mV = 1V$$

If V_{UNDER} is known, the equation can be rearranged to determine the minimum capacitance required using the following equation.

$$C_{OUT} = \frac{L \times I_{STEP}^2}{2 \times V_{UNDER} \times D_{MAX}(V_{IN} - V_{OUT})}$$

One additional specification to check when selecting output capacitors is the ripple current rating of the capacitors. The ripple current calculated above is 2.4A. For example, the Sanyo 2R5TPE220M9 meets the previous requirements (220μF/9mΩ) and has a ripple rating of 3900mA. A single capacitor can meet this current rating.

If the current rating had been below the calculated ripple current, then additional capacitors would be required. As a hypothetical, if the ripple current rating of a capacitor were 2000mA, then two capacitors would be required to meet the ripple current rating (making a total of 4000mA of ripple current rating). When adding additional capacitors it is important to check the resulting equivalent ESR (calculated as parallel resistors) to ensure enough ripple is available on the output.

LDO Output Capacitor

A minimum of 100nF is needed on the output of the LDO to ensure stability.

Bootstrap Capacitor

The minimum capacitance required depends on the total gate charge of the high side FET and the amount of droop allowed on the high side drive.

$$C_{BST} = \frac{Q_{HSG}}{V_{BSTDROOP}}$$

The Qg of the high side FET in the SC414 is 10nC. If the SC414 has a 5V gate drive, an acceptable droop on the bootstrap voltage is 100mV.

$$C_{BST} = \frac{10nC}{0.1V} = 0.1\mu F$$

A capacitor in the range of 0.1μF to 1.0μF will work. A high quality ceramic capacitor (X5R or X7R) is recommended.

Power Good Pull-up Requirements

Power good is an open-drain pin and requires a pull-up resistor. A value of 10kΩ to 20kΩ should be sufficient.

Additional Decoupling Requirements

A high quality 1μF ceramic capacitor is required between the V5V pin and PGND. If the LDO is used to bias the controller, this capacitor is in addition to the capacitor required for stability. If an external supply is used for the V5V voltage, another capacitor of at least 100nF value should be used between V5V and AGND.

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