



# Intel® 80219 General Purpose PCI Processor Datasheet

## Extended Temperature Support

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### Product Features

- Core Features
  - Integrated Intel XScale® Core
  - ARM® V5T Instruction Set
  - ARM V5E DSP Extensions
  - 400 MHz and 600 MHz
  - Write Buffer, Write-back Cache
- PCI Bus Interface
  - *PCI Local Bus Specification*, Rev. 2.2 compliant
  - *PCI-X Addendum to the PCI Local Bus Specification*, Rev. 1.0a
  - 64-bit/66 MHz Operation in PCI Mode
  - 64-bit/133 MHz Operation in PCI-X Mode
  - Support 32-bit PCI Initiators and Targets
  - Four Split Read Requests as Initiator
  - Eight Split Read Requests as Target
  - 64-bit Addressing Support
- Memory Controller
  - PC200 Double Data Rate (DDR) SDRAM
  - Up to 1 Gbyte of 64-bit DDR SDRAM
  - Up to 512 Mbytes of 32-bit DDR SDRAM
  - Single-bit Error Correction, Multi-bit Support (ECC)
  - 1024-byte Posted Memory Write Queue
  - 40- and 72-bit wide Memory Interface
- Address Translation Unit
  - 2 Kbyte or 4 Kbyte Outbound Read Queue
  - 4 Kbyte Outbound Write Queue
  - 4 Kbyte Inbound Read and Write Queue
  - Connects Internal Bus to PCI/PCI-X Bus
- DMA Controller
  - Two Independent Channels Connected to Internal Bus
  - Up to 1064 Mbytes/s Burst Support in PCI-X Mode
  - Up to 1600 Mbytes/s Burst Support for Internal Bus
  - Two 1-Kbyte Queues in Ch-0 and Ch-1
  - $2^{32}$  Addressing Range on Internal Bus Interface
  - $2^{64}$  Addressing Range on PCI Interface
- I<sup>2</sup>C Bus Interface Units
  - Two Separate I<sup>2</sup>C Units
  - Serial Bus
  - Master/Slave Capabilities
  - System Management Functions
- Peripheral Performance Monitoring Unit
  - One Dedicated Global Time Stamp Counter
  - Fourteen Programmable Event Counters
  - Three Control/Status Registers
- Timers
  - Two Dual-programmable 32-bit Timers
  - Watchdog Timer
- 544-Ball, Plastic Ball Grid Array (PBGA)
- Eight General Purpose I/O Pins
- Intel® 80219 General Purpose PCI Processor can operate at an ambient temperature of 0° to 85°C



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## Revision History

| Date          | Revision # | Description      |
|---------------|------------|------------------|
| November 2003 | 001        | Initial release. |



## 1.0 Introduction

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### 1.1 About This Document

This is the *Intel® 80219 General Purpose PCI Processor Datasheet*. This datasheet contains a functional overview, package signal locations, targeted electrical specifications, and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *Intel® 80219 General Purpose PCI Processor Developer's Manual*.

Intel Corporation assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

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#### 1.1.1 Terminology

To aid the discussion of the Intel® 80219 general purpose PCI processor (80219) architecture, the following terminology is used:

|                 |                                                                                               |
|-----------------|-----------------------------------------------------------------------------------------------|
| Downstream      | At or toward a PCI bus with a higher number (after configuration)                             |
| Host processor  | Processor located upstream from the 80219                                                     |
| Local processor | Intel XScale® core (ARM* architecture compliant) within the 80219                             |
| Local bus       | 80219 Internal Bus                                                                            |
| Local memory    | Memory subsystem on the Intel XScale® core PC200 DDR SDRAM or Peripheral Bus Interface busses |
| Upstream        | At or toward a PCI bus with a lower number (after configuration)                              |

## 1.1.2 Other Relevant Documents

**Table 1. Related Documentation**

| Document Title                                                                       | Document# / Contact                                                                                                 |
|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| <i>Intel® 80219 General Purpose PCI Processor Developer's Manual</i>                 | 274017                                                                                                              |
| <i>Intel® 80219 General Purpose PCI Processor Specification Update</i>               | 274020                                                                                                              |
| <i>Intel® 80219 General Purpose PCI Processor Design Guide</i>                       | 273354                                                                                                              |
| <i>PCI Local Bus Specification, Revision 2.2</i>                                     | PCI Special Interest Group<br>1-800-433-5177<br><a href="http://www.pcisig.com/home">http://www.pcisig.com/home</a> |
| <i>PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a</i>              |                                                                                                                     |
| <i>PCI-to-PCI Bridge Architecture Specification, Revision 1.1</i>                    |                                                                                                                     |
| <i>PCI System Design Guide, Revision 1.0</i>                                         |                                                                                                                     |
| <i>PCI Hot-Plug Specification, Revision 1.0</i>                                      |                                                                                                                     |
| <i>PCI Bus Power Management Interface Specification, Revision 1.1</i>                |                                                                                                                     |
| <i>I<sup>2</sup>C Peripherals for Microcontrollers</i>                               | Philips Semiconductor*                                                                                              |
| <i>Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)</i> | <a href="http://www.teleport.com/~acpi/">http://www.teleport.com/~acpi/</a>                                         |

**NOTE:** Also see our product web site at: <http://developer.intel.com/design/iio/>.



## 1.2 About the Intel® 80219 General Purpose PCI Processor

The 80219 is a single-function device that integrates the Intel XScale® core with intelligent peripherals, including a PCI bus application bridge. The 80219 consolidates into a single system:

- Intel XScale® core
- PCI - Local Memory Bus Address Translation Unit
- Messaging Unit
- Direct Memory Access (DMA) Controller
- Peripheral Bus Interface Unit
- Integrated Memory Controller
- Performance Monitor
- Two I<sup>2</sup>C Bus Interface Units
- Eight General Purpose Input Output (GPIO) ports

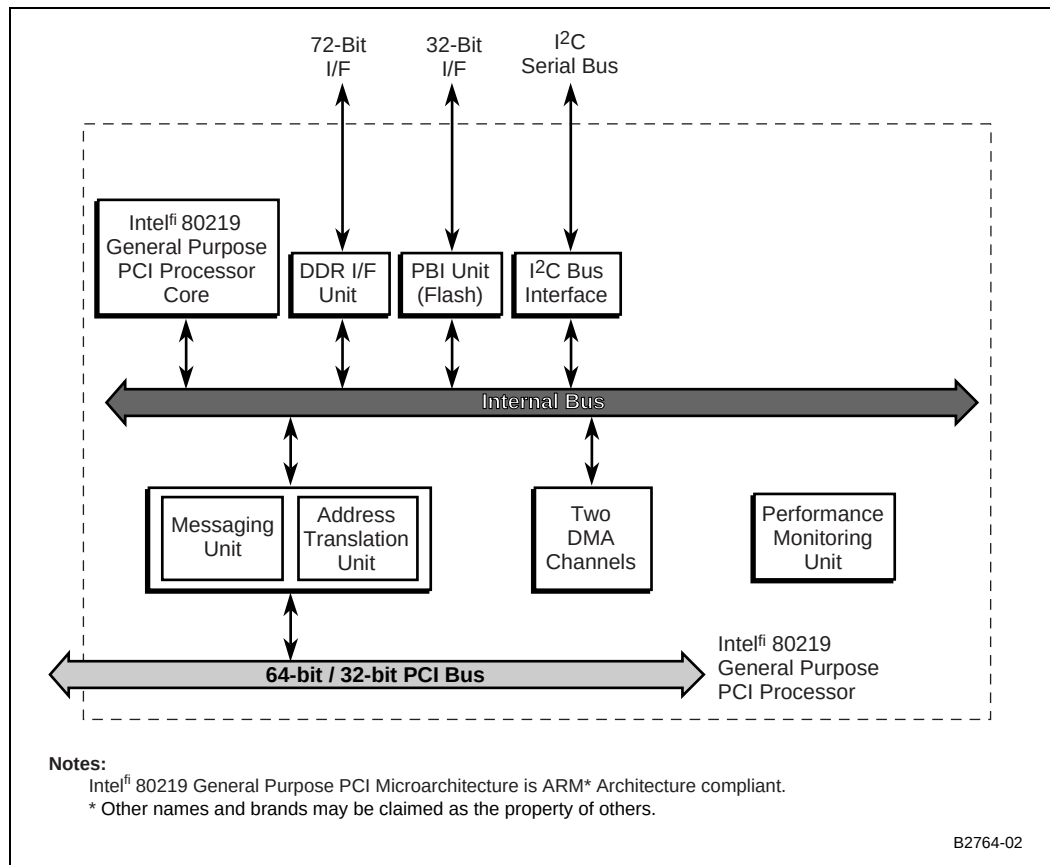
It is an integrated processor that addresses the needs of intelligent I/O applications and helps reduce intelligent I/O system costs.

The PCI Bus is an industry standard, high performance, low latency system bus. The 80219 PCI Bus is capable of 133 MHz operation in PCI-X mode as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. Also, the processor supports a 66 MHz conventional PCI mode as defined by the *PCI Local Bus Specification*, Revision 2.2. The addition of the Intel XScale® core brings intelligence to the PCI bus application bridge.

The 80219 is a single-function PCI device. This function represents the address translation unit. The address translation unit is an ‘application bridge’ as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. The 80219 contains PCI configuration space accessible through the PCI bus.

Figure 1 is a block diagram of the 80219.

**Figure 1. Intel® 80219 General Purpose PCI Processor Functional Block Diagram**



## 2.0 Features

---

The 80219 combines the Intel XScale<sup>®</sup> core with powerful new features to create a general embedded application processor. This single-function PCI device is fully compliant with the *PCI Local Bus Specification*, Revision 2.2. 80219-specific features include:

- Address Translation Unit
- Memory Controller
- Peripheral Bus Interface
- I<sup>2</sup>C Bus Interface Units
- DMA Controller
- Performance Monitoring Unit
- Messaging Unit
- I<sub>2</sub>O\* Compatibility

The subsections that follow briefly overview each feature. Refer to the appropriate chapter in the *Intel<sup>®</sup> 80219 General Purpose PCI Processor Developer's Manual* for full technical descriptions.

The 80219 core is based upon the Intel XScale<sup>®</sup> core. The core processor operates at a maximum frequency of 600 MHz. The instruction cache is 32 Kbytes in size and is 32-way set associative. Also, the core processor includes a data cache that is 32 Kbytes and is 32-way set associative and a mini data cache that is 2 Kbytes and is 2-way set associative.

The 80219 includes 8 General Purpose I/O (GPIO) pins.

### 2.1 Internal Bus

The Internal Bus is a high-speed interconnect between all internal units and controllers. The Internal Bus operates at 200 MHz and is 64 bits wide.

### 2.2 DMA Controller

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the local memory. Two separate DMA channels accommodate data transfers on the PCI bus. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale<sup>®</sup> core only.

## 2.3 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 80219 local memory. The ATU supports transactions between PCI address space and the 80219 address space. Address translation is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® core. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the following extended capability configuration headers:

1. Power Management header as defined by *PCI Bus Power Management Interface Specification*, Revision 1.1.
2. Message Signaled Interrupt capability structure specified in *PCI Local Bus Specification*, Revision 2.2.
3. PCI-X Capabilities List Item specified in the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

## 2.4 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80219. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms:

- Message Registers
- Doorbell Registers
- Circular Queues
- Index Registers

Each allows a host processor or external PCI device and the 80219 to communicate through message passing and interrupt generation.

## 2.5 Memory Controller

The Memory Controller allows direct control of a PC200 DDR SDRAM memory subsystem. It features programmable chip selects and support for error correction codes (ECC). External memory may be configured as PCI addressable memory or private 80219 memory.

## 2.6 Peripheral Bus Interface

The Peripheral Bus Interface Unit (PBI) is a data communication path to certain components of a 80219 hardware system that do not have PCI bus interfaces and/or do not optimally reside on the PCI Bus. Examples of such components include Flash Memory and DSP host interface ports. The PBI allows the processor to manipulate data and interact with these components in the I/O environment. To perform these tasks at high bandwidth, the bus features a burst transfer capability which allows successive 32-bit data transfers. The bus has a 33 MHz, 66 MHz and a 100 MHz operating mode.

## 2.7 Performance Monitoring Unit

The Performance Monitoring Unit (PMON) allows various events on the 80219 to be monitored. The 14 Event Counters may be programmed to observe events selected from a pre-defined set of events.

## 2.8 I<sup>2</sup>C Bus Interface Units

There are two I<sup>2</sup>C (Inter-Integrated Circuit) Bus Interface Units that allow the Intel XScale<sup>®</sup> core to serve as a master and slave device residing on the I<sup>2</sup>C bus. The I<sup>2</sup>C unit uses a serial bus developed by Philips Semiconductor\* consisting of a two-pin interface. The bus allows the 80219 to interface to other I<sup>2</sup>C peripherals and microcontrollers for system management functions. It requires a minimum of hardware for an economical system to relay status and reliability information on the I/O subsystem to an external device. Also refer to *I<sup>2</sup>C Peripherals for Microcontrollers* (Philips Semiconductor\*).

## 3.0 Package Information

### 3.1 Package Introduction

The 80219 is offered in a Plastic Ball Grid Array (PBGA) package. This is a perimeter array package with 508 ball connections in the outer area of the package and a square 6x6 grid of rows of ball connections in the middle area of the package. See [Figure 3 “544-Lead PBGA Package \(Bottom View\)”](#) on page 26.

#### 3.1.1 Functional Signal Definitions

This section defines the pins and signals.

**Table 2. Pin Description Nomenclature**

| Symbol              | Description                                                                                                                                                                                                                                                               |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I                   | Input pin only                                                                                                                                                                                                                                                            |
| O                   | Output pin only                                                                                                                                                                                                                                                           |
| I/O                 | Pin may be either an input or output.                                                                                                                                                                                                                                     |
| OD                  | Open Drain pin                                                                                                                                                                                                                                                            |
| -                   | Pin must be connected as described.                                                                                                                                                                                                                                       |
| Sync(...)           | Synchronous. Signal meets timings relative to an input clock.<br>Sync(P) Synchronous to <b>P_CLK</b><br>Sync(M) Synchronous to <b>M_CK[2:0]</b><br>Sync(PB) Synchronous to <b>PB_CLK</b><br>Sync(T) Synchronous to <b>TCK</b>                                             |
| Async               | Asynchronous. Inputs may be asynchronous relative to all clocks. All asynchronous signals are level-sensitive.                                                                                                                                                            |
| Rst(P)              | The pin is reset with <b>P_RST#</b> .                                                                                                                                                                                                                                     |
| Rst(M)              | The pin is reset with <b>M_RST#</b> .<br>Note that <b>M_RST#</b> is asserted when <b>P_RST#</b> is asserted or <b>PCSR[5]</b> is set with software.                                                                                                                       |
| Rst(T)              | The pin is reset with <b>TRST#</b> .                                                                                                                                                                                                                                      |
| (Configuration Pin) | These pins are used during reset to configure the processor.<br>These pins have internal pullup resistors which are turned on when <b>P_RST#</b> is low. To configure the pin low connect a 4.7KΩ resistor from the pin to ground. By default the pin is configured high. |

Table 3. DDR SDRAM Signals

| Name             | Count | Type                     | Description                                                                                                                                                                                                                          |
|------------------|-------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RCVENI#          | 1     | I                        | <b>RECEIVE ENABLE IN</b> provides delay information for enabling the input receivers and must be connected to <b>RCVENO#</b> of the 80219.                                                                                           |
| RCVENO#          | 1     | O                        | <b>RECEIVE ENABLE OUT</b> must be connected to <b>RCVENI#</b> of the 80219 and be trace length matched to Clock Trace plus average DQ Traces.                                                                                        |
| M_CK[2:0]        | 3     | O                        | <b>MEMORY CLOCKS</b> are used to provide the positive differential clocks to the external SDRAM memory subsystem.                                                                                                                    |
| M_CK[2:0]#       | 3     | O                        | <b>MEMORY CLOCKS</b> are used to provide the negative differential clocks to the external SDRAM memory subsystem.                                                                                                                    |
| M_RST#           | 1     | O<br>Async               | <b>MEMORY RESET</b> indicates when the memory subsystem has been reset with <b>P_RST#</b> or a software reset.                                                                                                                       |
| SA[12:0]         | 13    | O<br>Sync(M)<br>Rst(M)   | <b>MEMORY ADDRESS BUS</b> carries the multiplexed row and column addresses to the SDRAM memory banks. For <b>SA[10]</b> , See Note 1.                                                                                                |
| SBA[1:0]         | 2     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM BANK ADDRESS</b> indicates which of the SDRAM internal banks are read or written during the current transaction. See Note 1.                                                                                                |
| SRAS#            | 1     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM ROW ADDRESS STROBE</b> indicates the presence of a valid row address on the Multiplexed Address Bus <b>SA[12:0]</b> . See Note 1.                                                                                           |
| SCAS#            | 1     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM COLUMN ADDRESS STROBE</b> indicates the presence of a valid column address on the Multiplexed Address Bus <b>SA[12:0]</b> . See Note 1.                                                                                     |
| SWE#             | 1     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM WRITE ENABLE</b> indicates that the current memory transaction is a write operation. See Note 1.                                                                                                                            |
| SCE[1:0]#        | 2     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM CHIP SELECT</b> enables the SDRAM devices for a memory access (Physical banks 0 and 1). See Note 1.                                                                                                                         |
| SCKE[1:0]        | 2     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM CLOCK ENABLE</b> enables the clocks for the SDRAM memory. Deasserting places the SDRAM in self-refresh mode. See Note 1.                                                                                                    |
| DQ[63:0]         | 64    | I/O<br>Sync(M)<br>Rst(M) | <b>SDRAM DATA BUS</b> carries 64-bit data to and from memory. During a data cycle, read or write data is present on one or more contiguous bytes. During write operations, unused pins are driven to determinate values. See Note 1. |
| SCB[7:0]         | 8     | I/O<br>Sync(M)<br>Rst(M) | <b>SDRAM ECC CHECK BITS</b> carry the 8-bit ECC code to and from memory during data cycles. See Note 1.                                                                                                                              |
| DQS[8:0]         | 9     | I/O<br>Sync(M)<br>Rst(M) | <b>SDRAM DATA STROBES</b> carry the strobe signals which are used to capture data on the data bus. See Note 1.                                                                                                                       |
| SDQM[8:0]        | 9     | O<br>Sync(M)<br>Rst(M)   | <b>SDRAM DATA MASK</b> controls which bytes on the data bus should be written. When <b>SDQM[8:0]</b> is asserted, the SDRAM devices do not accept valid data from the byte lanes. See Note 1.                                        |
| V <sub>REF</sub> | 1     | I                        | <b>SDRAM VOLTAGE REFERENCE</b> is used to supply the reference voltage to the differential inputs of the memory controller pins.                                                                                                     |

**NOTE:**

1. These pins remain functional for 20 **M\_CK[2:0]** periods after **M\_RST#** is asserted for a warm boot. The designated Rst(M) state applies after 20 **M\_CK[2:0]** periods after **M\_RST#** is asserted. For more details, refer to the MCU Chapter of the *Intel® 80219 General Purpose PCI Processor Developer's Manual*.

**Table 4. Peripheral Bus Interface Signals (Sheet 1 of 3)**

| Name            | Count | Type                      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------|-------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>AD[31:0]</b> | 32    | I/O<br>Sync(PB)<br>Rst(M) | <b>ADDRESS / DATA BUS</b> During an address cycle bits 31-2 contain the physical word address and bits 1-0 specify the number of data transfers during the bus transaction.<br><br>00= 1 Transfer<br>01= 2 Transfers<br>10= 3 Transfers<br>11= 4 Transfers.<br><br>During a data cycle bits 31-0, 15-0 or 7-0 contain valid data, depending on the corresponding 32-, 16- or 8-bit bus width. During 16- and 8-bit bus write operations the unused bus pins are driven to determinate values.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>A[3:2]</b>   | 2     | O<br>Sync(PB)<br>Rst(M)   | <b>ADDRESS [3:2]</b> carries a demultiplexed version of bits 3 and 2 of the address bus. During an address cycle <b>A[3:2]</b> matches <b>AD[3:2]</b> . During a burst read or write data cycle <b>A[3:2]</b> represents the current DWORD address in the burst transaction.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>BE[3:0]#</b> | 4     | O<br>Sync(PB)<br>Rst(M)   | <b>BYTE ENABLES</b> select which of up to four data bytes on the bus participate in the current bus access. The byte enables are asserted during the address cycle. These signals do not toggle during a burst and they remain active through the last data cycle. Byte enable encoding is dependent on the bus width:<br><br>32-bit bus:<br><ul style="list-style-type: none"> <li><b>BE[3]#</b> enables data on <b>AD[31:24]</b></li> <li><b>BE[2]#</b> enables data on <b>AD[23:16]</b></li> <li><b>BE[1]#</b> enables data on <b>AD[15:8]</b></li> <li><b>BE[0]#</b> enables data on <b>AD[7:0]</b></li> </ul> 16-bit bus:<br><ul style="list-style-type: none"> <li><b>BE[3]#</b> enables data on <b>AD[15:8]</b></li> <li><b>BE[2]#</b> is not used (state is high)</li> <li><b>BE[1]#</b> becomes Address Bit 1 (<b>A[1]</b>)</li> <li><b>BE[0]#</b> enables data on <b>AD[7:0]</b></li> </ul> 8-bit bus:<br><ul style="list-style-type: none"> <li><b>BE[3]#</b> is not used (state is high)</li> <li><b>BE[2]#</b> is not used (state is high)</li> <li><b>BE[1]#</b> becomes Address Bit 1 (<b>A[1]</b>)</li> <li><b>BE[0]#</b> becomes Address Bit 0 (<b>A[0]</b>)</li> </ul> For 16- and 8-bit bus accesses these address bits are asserted in conjunction with <b>A[3:2]</b> . |
| <b>ALE</b>      | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>ADDRESS LATCH ENABLE</b> indicates the transfer of a physical address. The pin is asserted during the first address cycle and deasserted during the second address cycle. The pin floats whenever the bus is relinquished to an external device                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>ADS#</b>     | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>ADDRESS STROBE</b> indicates a valid address and the start of a new bus access. The pin is asserted during the second address cycle and deasserted during the first data cycle. The pin floats whenever the bus is relinquished to an external device                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>PB_CLK</b>   | 1     | O                         | <b>PERIPHERAL BUS CLOCK</b> is the reference clock for all signals on the peripheral bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>W/R#</b>     | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>WRITE / READ</b> indicates whether the bus access is a write or a read with respect to the 80219 and is valid during the entire bus access. This pin may be used to control the OE# input on the flash ROM. The pin floats whenever the bus is relinquished to an external device<br><br>0 = Read<br>1 = Write                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |



Table 4. Peripheral Bus Interface Signals (Sheet 2 of 3)

| Name                                                   | Count | Type                      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------------------------------------------------|-------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>FWE#</b>                                            | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>FLASH WRITE ENABLE</b> indicates whether the bus access is a write or a read with respect to the 80219 and is valid during the entire bus access. This pin is used for flash memory accesses and controls the <b>SWE#</b> input on the ROM. The pin floats whenever the bus is relinquished to an external device.<br><br>0 = Write<br>1 = Read                                                                                                                                                                                                                                                                                                     |
| <b>DEN#</b>                                            | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>DATA ENABLE</b> indicates data transfer cycles during a bus access. <b>DEN#</b> is asserted at the start of the first data cycle and deasserted at the end of the last data cycle. The pin is used to provide control for data transceivers connected to the bus. The pin floats whenever the bus is relinquished to an external device                                                                                                                                                                                                                                                                                                             |
| <b>BLAST#</b>                                          | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>BURST LAST</b> indicates the last data transfer of a bus access. <b>BLAST#</b> remains active when wait states are inserted and becomes inactive after the final data transfer is complete. The pin floats whenever the bus is relinquished to an external device                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>RDYRCV#</b>                                         | 1     | I/O<br>Sync(PB)<br>Rst(M) | <b>READY / RECOVER</b> During a data cycle the pin indicates that data may be sampled or removed.<br><br>0 = Sample data<br>1 = Insert wait state<br><br>During a recover state the pin indicates that the recover state is repeated. This function allows slow external devices longer to float their pins before the next address is driven.<br><br>0 = Insert recovery state<br>1 = Recovery complete<br><br><b>NOTE:</b> PBI Base Address Register 0 bit 9 (Flash Window Enable) is enabled for flash by default to support the boot process. See PBBAR0 description in the <i>Intel® 80219 General Purpose PCI Processor Developer's Manual</i> . |
| <b>HOLD</b>                                            | 1     | I<br>Sync(PB)             | <b>HOLD</b> is used by an external device to request access to the bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>HOLDA</b>                                           | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>HOLD ACKNOWLEDGE</b> indicates to an external device that it has been granted access to the bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>PB_RST#</b>                                         | 1     | O<br>Async                | <b>PERIPHERAL BUS RESET</b> indicates when the peripheral bus has been reset with <b>P_RST#</b> or a software reset.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>PCE[5]# / PBI100MHZ#</b><br><br>(Configuration Pin) | 1     | I/O<br>Sync(PB)<br>Rst(M) | <b>PERIPHERAL CHIP ENABLES</b> specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access.<br><br><b>PERIPHERAL BUS 100 MHz ENABLE</b> is latched at the deasserting edge of <b>P_RST#</b> and it indicates the speed at which the PBI bus operates.<br><b>[PBI100MHZ#, PBI66MHZ#]</b><br>11 = 33 MHz (Default Mode)<br>10 = 66 MHz<br>01 = 100 MHz<br>00 = Undefined (Reserved - Do Not Use)                                                                                                                                                                       |
| <b>PCE[4]# / PBI66MHZ#</b><br><br>(Configuration Pin)  | 1     | I/O<br>Sync(PB)<br>Rst(M) | <b>PERIPHERAL CHIP ENABLES</b> specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access.<br><br><b>PERIPHERAL BUS 66MHz ENABLE</b> is latched at the deasserting edge of <b>P_RST#</b> and it indicates the speed at which the PBI bus operates.<br><b>[PBI100MHZ#, PBI66MHZ#]</b><br>11 = 33 MHz (Default Mode)<br>10 = 66 MHz<br>01 = 100 MHz<br>00 = Undefined (Reserved - Do Not Use)                                                                                                                                                                         |

**Table 4. Peripheral Bus Interface Signals (Sheet 3 of 3)**

| Name                                                  | Count | Type                      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------------------------------------|-------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>PCE[3]# / P_BOOT16#</b><br><br>(Configuration Pin) | 1     | O<br>Sync(PB)<br>Rst(M)   | <b>PERIPHERAL CHIP ENABLES</b> specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access.<br><br><b>PERIPHERAL BUS BOOT WIDTH 16 ENABLE</b> specifies the width of the peripheral bus for flash accesses during boot up.<br>0 = 16-bit bus width (Requires Pull-Down Resistor)<br>1 = 8-bit bus width (Default Mode)                                                                                                                                                      |
| <b>PCE[2]# / 32BITPCI#</b><br><br>(Configuration Pin) | 1     | I/O<br>Sync(PB)<br>Rst(M) | <b>PERIPHERAL CHIP ENABLES</b> specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access.<br><br><b>32 BIT PCI</b> is latched at the deasserting edge of P_RST# and it indicates the width of the PCI-X bus to the PCI-X Status Register (bit 16 of the PCI-X Status Register).<br>0 = 32-Bit PCI-X Bus (Requires pull-down resistor)<br>1 = 64-Bit PCI-X Bus (Default mode)                                                                                              |
| <b>PCE[1]# / RETRY</b><br><br>(Configuration Pin)     | 1     | I/O<br>Sync(PB)<br>Rst(M) | <b>PERIPHERAL CHIP ENABLES</b> specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access.<br><br><b>RETRY</b> is latched at the deasserting edge of P_RST# and it determines when the Primary PCI interface disables PCI configuration cycles by signaling a Retry until the Configuration Cycle Retry bit is cleared in the PCI Configuration and Status Register.<br>0 = Configuration Cycles enabled (Requires pull-down resistor)<br>1 = Retry enabled (Default mode) |
| <b>PCE[0]# / RST_MODE#</b><br><br>(Configuration Pin) | 1     | I/O<br>Sync(PB)<br>Rst(M) | <b>PERIPHERAL CHIP ENABLES</b> specify which of the six memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access.<br><br><b>RESET MODE</b> is latched at the deasserting edge of P_RST# and it determines when the 80219 is held in reset until the Intel XScale® microarchitecture Reset bit is cleared in the PCI Configuration and Status Register.<br>0 = Hold in reset (Requires pull-down resistor)<br>1 = Don't hold in reset (Default mode)                                               |
| <b>WIDTH[1:0]</b>                                     | 2     | O<br>Sync(PB)<br>Rst(M)   | <b>WIDTH</b> denotes the physical memory attributes for a bus transaction. The pins float whenever the bus is relinquished to an external device.<br>00 = 8 Bits Wide<br>01 = 16 Bits Wide<br>10 = 32 Bits Wide<br>11 = Reserved                                                                                                                                                                                                                                                                                                                              |

Table 5. PCI Bus Signals (Sheet 1 of 2)

| Name         | Count | Type                           | Description                                                                                                                                                                                                                                                                            |
|--------------|-------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P_AD[31:0]   | 32    | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI ADDRESS/DATA</b> is the multiplexed PCI address and bottom 32 bits of the data bus.                                                                                                                                                                                             |
| P_AD[63:32]  | 32    | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI DATA</b> is the upper 32 bits of the PCI data bus driven during the data phase.                                                                                                                                                                                                 |
| P_PAR        | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS PARITY</b> is even parity across P_AD[31:0] and P_C/BE[3:0]#.                                                                                                                                                                                                               |
| P_PAR64      | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS UPPER DWORD PARITY</b> is even parity across P_AD[63:32] and P_C/BE[7:4]#.                                                                                                                                                                                                  |
| P_C/BE[3:0]# | 4     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS COMMAND and BYTE ENABLES</b> are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables for P_AD[31:0].                                                                              |
| P_C/BE[7:4]# | 4     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS BYTE ENABLES</b> are as byte enables for P_AD[63:32] during the data phase.                                                                                                                                                                                                 |
| P_REQ#       | 1     | O<br>Rst(P)                    | <b>PCI BUS REQUEST</b> indicates to the PCI bus arbiter that the 80219 desires use of the PCI bus.                                                                                                                                                                                     |
| P_REQ64#     | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS REQUEST 64-BIT TRANSFER</b> indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of P_ACK64#.                                                                            |
| P_GNT#       | 1     | I<br>Sync(P)                   | <b>PCI BUS GRANT</b> indicates that access to the PCI bus has been granted.                                                                                                                                                                                                            |
| P_ACK64#     | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS ACKNOWLEDGE 64-BIT TRANSFER</b> indicates that the device has positively decoded its address as the target of the current access and the target transfers data using the full 64-bit data bus.                                                                              |
| P_FRAME#     | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS CYCLE FRAME</b> is asserted to indicate the beginning and duration of an access.                                                                                                                                                                                            |
| P_IRDY#      | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS INITIATOR READY</b> indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the Address/Data bus. During a read, it indicates the processor is ready to accept the data. |
| P_TRDY#      | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS TARGET READY</b> indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the Address/Data bus. During a write, it indicates the target is ready to accept the data.           |
| P_STOP#      | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS STOP</b> indicates a request to stop the current transaction on the PCI bus.                                                                                                                                                                                                |
| P_DEVSEL#    | 1     | I/O<br>Sync(P)<br>Rst(P)       | <b>PCI BUS DEVICE SELECT</b> is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.                                                                                                               |
| P_SERR#      | 1     | I/O<br>OD<br>Sync(P)<br>Rst(P) | <b>PCI BUS SYSTEM ERROR</b> is driven for address parity errors on the PCI bus.                                                                                                                                                                                                        |
| P_CLK        | 1     | I                              | <b>PCI BUS INPUT CLOCK</b> provides the timing for all PCI transactions and is the clock source for most internal 80219 units.                                                                                                                                                         |

**Table 5. PCI Bus Signals (Sheet 2 of 2)**

| Name               | Count | Type                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------|-------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>P_RST#</b>      | 1     | I<br>Async                 | <b>RESET</b> brings PCI-specific registers, sequencers, and signals to a consistent state. When <b>P_RST#</b> is asserted: PCI output signals are driven to a known consistent state.<br><br>PCI bus interface output signals are three-stated.<br><br>Open drain signals such as <b>P_SERR#</b> are floated. <b>P_RST#</b> may be asynchronous to <b>P_CLK</b> when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge. |
| <b>P_PERR#</b>     | 1     | I/O<br>Sync(P)<br>Rst(P)   | <b>PCI BUS PARITY ERROR</b> is asserted when a data parity error occurs during a PCI bus transaction.                                                                                                                                                                                                                                                                                                                                                                               |
| <b>P_IDSEL</b>     | 1     | I<br>Sync(P)               | <b>PCI BUS INITIALIZATION DEVICE SELECT</b> is used to select the 80219 during a Configuration Read or Write command on the PCI bus.                                                                                                                                                                                                                                                                                                                                                |
| <b>P_INT[A:D]#</b> | 4     | O<br>OD<br>Async<br>Rst(P) | <b>PCI BUS INTERRUPT</b> requests an interrupt. The assertion and deassertion of <b>P_INT[A:D]#</b> is asynchronous to <b>P_CLK</b> . A device asserts its <b>P_INT[A:D]#</b> line when requesting attention from its device driver. Once the <b>P_INT[A:D]#</b> signal is asserted, it remains asserted until the device driver clears the pending request. <b>P_INT[A:D]#</b> Interrupts are level sensitive.                                                                     |
| <b>P_M66EN</b>     | 1     | I                          | <b>PCI BUS 66 MHz ENABLE</b> indicates the speed of the PCI bus. When this signal is sampled high the PCI bus speed is 66 MHz, when low the bus speed is 33 MHz.                                                                                                                                                                                                                                                                                                                    |

Table 6. Miscellaneous Signals (Sheet 1 of 2)

| Name              | Count | Type                                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------|-------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P_BMI             | 1     | O<br>Async<br>Rst(M)                          | <b>PCI-X Bus Master Indicator</b> is an output used for hiding an I/O Controller on the same bus segment as the 80219 by controlling the IDSEL line of that I/O Controller. The output state of this signal is controlled by bit 0 of the GPOD register and the default state at Reset is 0. When not being used, this pin will be a NC. Please see the 80219 Specification Update, Specification Clarification section for more details.                                                                                                                  |
| XINT[3:0]#        | 4     | I<br>Async                                    | <b>EXTERNAL INTERRUPT REQUESTS</b> are used by external devices to request interrupt service. These pins are level-detect only and are internally synchronized. These interrupts may be directed to either the PCI pins <b>P_INT[A:D]#</b> or to the 80219 interrupt controller pins <b>XINT[3:0]#</b> as shown below.<br><b>XINT[0]#</b> ⇒ <b>P_INT[A]#</b> or <b>XINT[0]#</b><br><b>XINT[1]#</b> ⇒ <b>P_INT[B]#</b> or <b>XINT[1]#</b><br><b>XINT[2]#</b> ⇒ <b>P_INT[C]#</b> or <b>XINT[2]#</b><br><b>XINT[3]#</b> ⇒ <b>P_INT[D]#</b> or <b>XINT[3]#</b> |
| HPI#              | 1     | I<br>Async                                    | <b>HIGH PRIORITY INTERRUPT</b> causes a high priority non-maskable interrupt to the 80219. This pin is level-detect only and is internally synchronized.                                                                                                                                                                                                                                                                                                                                                                                                   |
| GPIO[3:0]         | 4     | I/O<br>Async<br>Rst(M)                        | <b>GENERAL PURPOSE INPUT/OUTPUT.</b> These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input.                                                                                                                                                                                                                                                                                                                                                                                      |
| GPIO[4] /<br>SDA1 | 1     | I/O<br>Async<br>Rst(P)<br>I/O<br>OD<br>Rst(M) | <b>GENERAL PURPOSE INPUT/OUTPUT.</b> These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input.<br><b>I<sup>2</sup>C DATA</b> is used for data transfer and arbitration on the I <sup>2</sup> C bus. This is one of two I <sup>2</sup> C buses that the user may enable. 2.7K pull-up is required.                                                                                                                                                                                   |
| GPIO[5] /<br>SCL1 | 1     | I/O<br>Async<br>Rst(P)<br>I/O<br>OD<br>Rst(M) | <b>GENERAL PURPOSE INPUT/OUTPUT.</b> These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input.<br><b>I<sup>2</sup>C CLOCK</b> provides synchronous operation of the I <sup>2</sup> C bus. This is one of two I <sup>2</sup> C buses that the user may enable. 2.7K pull-up is required.                                                                                                                                                                                             |
| GPIO[6] /<br>SDA0 | 1     | I/O<br>Async<br>Rst(P)<br>I/O<br>OD<br>Rst(M) | <b>GENERAL PURPOSE INPUT/OUTPUT.</b> These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input.<br><b>I<sup>2</sup>C DATA</b> is used for data transfer and arbitration on the I <sup>2</sup> C bus. This is one of two I <sup>2</sup> C buses that the user may enable. 2.7K pull-up is required.                                                                                                                                                                                   |
| GPIO[7] /<br>SCL0 | 1     | I/O<br>Async<br>Rst(P)<br>I/O<br>OD<br>Rst(M) | <b>GENERAL PURPOSE INPUT/OUTPUT.</b> These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input.<br><b>I<sup>2</sup>C CLOCK</b> provides synchronous operation of the I <sup>2</sup> C bus. This is one of two I <sup>2</sup> C buses that the user may enable. 2.7K pull-up is required.                                                                                                                                                                                             |
| TCK               | 1     | I<br>Rst(T)                                   | <b>TEST CLOCK</b> is an input which provides the clocking function for the IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the component on the rising edge and data is clocked out of the component on the falling edge.                                                                                                                                                                                                                                                                                            |
| TDI               | 1     | I<br>Sync(T)<br>Rst(T)                        | <b>TEST DATA INPUT</b> is the serial input pin for the JTAG feature. TDI is sampled on the rising edge of <b>TCK</b> , during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.                                                                                                                                                                                                                                                                |
| TDO               | 1     | O<br>Sync(T)<br>Rst(T)                        | <b>TEST DATA OUTPUT</b> is the serial output pin for the JTAG feature. <b>TDO</b> is driven on the falling edge of <b>TCK</b> during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, <b>TDO</b> floats. The behavior of <b>TDO</b> is independent of <b>P_RST#</b> .                                                                                                                                                                                                                                                             |

**Table 6. Miscellaneous Signals (Sheet 2 of 2)**

| Name                | Count | Type                   | Description                                                                                                                                                                                                                                                                                               |
|---------------------|-------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TRST#               | 1     | I<br>Asyn<br>Rst(T)    | <b>TEST RESET</b> asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan Testing (JTAG). This signal has a weak internal pull-up.                                                                                                                              |
| TMS                 | 1     | I<br>Sync(T)<br>Rst(T) | <b>TEST MODE SELECT</b> is sampled at the rising edge of <b>TCK</b> to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.                                                  |
| RCOMP               | 1     | I                      | <b>RESISTER COMPENSATION</b> is connected through a 30.1 $\Omega$ 1% 1/4 W resistor to ground. This is used to minimize the PCI pin variations due to voltage and temperature variations.                                                                                                                 |
| PWRDELAY            | 1     | I<br>Asyn              | <b>POWER FAIL DELAY</b> is used with external delay circuits to delay the reset of the memory controller in a power-fail condition. This allows the self-refresh command to be sent to the DDR SDRAM array.                                                                                               |
| POR#                | 1     | I                      | <b>POWER ON RESET</b> should be tied to the 1.3 V supply. It is used to provide clocks to the core from an internal ring oscillator during power up, which prevents internal contention. It also tri-states the other pins to prevent external power sequencing contention.                               |
| NC[5:0]             | 5     | I/O                    | <b>NO CONNECT</b> pins have no usable function. However they are in the boundary scan chain and must not be connected to any signal, power or ground.<br><b>Please note:</b> NC2 has been renamed to P_BMI.                                                                                               |
| V <sub>CCPLL1</sub> | 1     | PWR                    | <b>PLL POWER</b> is a separate V <sub>CC13</sub> supply ball for the phase lock loop clock generator. It is to be connected to the board V <sub>CC13</sub> plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships. |
| V <sub>CCPLL2</sub> | 1     | PWR                    | <b>PLL POWER</b> is a separate V <sub>CC13</sub> supply ball for the phase lock loop clock generator. It is to be connected to the board V <sub>CC13</sub> plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships. |
| V <sub>CC33</sub>   | 51    | PWR                    | <b>3.3 V POWER</b> balls to be connected to a 3.3 V power board plane.                                                                                                                                                                                                                                    |
| V <sub>CC25</sub>   | 38    | PWR                    | <b>2.5 V POWER</b> balls to be connected to a 2.5 V power board plane.                                                                                                                                                                                                                                    |
| V <sub>CC13</sub>   | 34    | PWR                    | <b>1.3 V POWER</b> balls to be connected to a 1.3 V power board plane.                                                                                                                                                                                                                                    |
| V <sub>SS</sub>     | 120   | GND                    | <b>GROUND</b> balls to be connected to a ground board plane.                                                                                                                                                                                                                                              |

Table 7. Pin Mode Behavior (Sheet 1 of 2)

| Pin                     | Reset | Norm | Hold | 32-Bit PCI | 32-Bit Mem | ECC Off |
|-------------------------|-------|------|------|------------|------------|---------|
| RCVENI#                 | VI    | VI   | -    | -          | -          | -       |
| RCVENO#                 | 1*    | VO   | -    | -          | -          | -       |
| M_CK[2:0]               | VO    | VO   | -    | -          | -          | -       |
| M_CK[2:0]#              | VO    | VO   | -    | -          | -          | -       |
| M_RST#                  | 0     | VO   | -    | -          | -          | -       |
| SA[12:0]                | 0*    | VO   | -    | -          | -          | -       |
| SBA[1:0]                | 0*    | VO   | -    | -          | -          | -       |
| SRAS#                   | 1*    | VO   | -    | -          | -          | -       |
| SCAS#                   | 1*    | VO   | -    | -          | -          | -       |
| SWE#                    | 1*    | VO   | -    | -          | -          | -       |
| SCE[1:0]#               | 1*    | VO   | -    | -          | -          | -       |
| SCKE[1:0]               | 0*    | VO   | -    | -          | -          | -       |
| DQ[63:32]               | Z*    | VB   | -    | -          | ID         | -       |
| Q[31:0]                 | Z*    | VB   | -    | -          | -          | -       |
| SCB[7:0]                | Z*    | VB   | -    | -          | -          | ID      |
| DQS[7:4]                | Z*    | VB   | -    | -          | ID         | -       |
| DQS[3:0]                | Z*    | VB   | -    | -          | -          | -       |
| DQS[8]                  | Z*    | VB   | -    | -          | -          | ID      |
| SDQM[7:4]               | Z*    | VO   | -    | -          | Z          | -       |
| SDQM[3:0]               | Z*    | VO   | -    | -          | -          | -       |
| SDQM[8]                 | Z*    | VO   | -    | -          | -          | Z       |
| AD[31:16]               | 0     | VB   | Z    | -          | -          | -       |
| AD[15:8]                | 0     | VB   | Z    | -          | -          | -       |
| AD[7:0]                 | 0     | VB   | Z    | -          | -          | -       |
| A[3:2]                  | 0     | VO   | Z    | -          | -          | -       |
| BE[3:0]#                | 1     | VO   | Z    | -          | -          | -       |
| ALE                     | 0     | VO   | Z    | -          | -          | -       |
| ADS#                    | 1     | VO   | Z    | -          | -          | -       |
| PB_CLK                  | VO    | VO   | -    | -          | -          | -       |
| W/R#                    | 0     | VO   | Z    | -          | -          | -       |
| FWE#                    | 1     | VO   | Z    | -          | -          | -       |
| DEN#                    | 1     | VO   | Z    | -          | -          | -       |
| BLAST#                  | 1     | VO   | Z    | -          | -          | -       |
| RDYRCV#                 | VO    | VI   | -    | -          | -          | -       |
| HOLD                    | VI    | VI   | -    | -          | -          | -       |
| HOLDA                   | VO    | VO   | 1    | -          | -          | -       |
| PB_RST#                 | 0     | VO   | -    | -          | -          | -       |
| PCE[5]# /<br>PBI100MHZ# | H     | VO   | 1    | -          | -          | -       |
| PCE[4]# /<br>PBI66MHZ#  | H     | VO   | 1    | -          | -          | -       |
| PCE[3]# /<br>P_BOOT16#  | H     | VO   | 1    | -          | -          | -       |
| PCE[2]# /<br>32BITPCI#  | H     | VO   | 1    | -          | -          | -       |
| PCE[1]# /<br>RETRY      | H     | VO   | 1    | -          | -          | -       |
| PCE[0]# /<br>RST_MODE#  | H     | VO   | 1    | -          | -          | -       |
| WIDTH[1:0]              | 0     | VO   | Z    | -          | -          | -       |

**Table 7. Pin Mode Behavior (Sheet 2 of 2)**

| Pin          | Reset | Norm | Hold | 32-Bit PCI | 32-Bit Mem | ECC Off |
|--------------|-------|------|------|------------|------------|---------|
| P_AD[63:32]  | Z     | VB   | -    | H          | -          | -       |
| P_AD[31:16]  | Z     | VB   | -    | -          | -          | -       |
| P_AD[15:0]   | Z     | VB   | -    | -          | -          | -       |
| P_PAR        | Z     | VB   | -    | -          | -          | -       |
| P_PAR64      | Z     | VB   | -    | H          | -          | -       |
| P_C/BE[3:0]# | Z     | VB   | -    | -          | -          | -       |
| P_C/BE[7:4]# | Z     | VB   | -    | H          | -          | -       |
| P_REQ#       | Z     | VO   | -    | -          | -          | -       |
| P_REQ64#     | Z     | VB   | -    | -          | -          | -       |
| P_GNT#       | VI    | VI   | -    | -          | -          | -       |
| P_ACK64#     | Z     | VB   | -    | -          | -          | -       |
| P_FRAME#     | VI    | VB   | -    | -          | -          | -       |
| P_IRDY#      | VI    | VB   | -    | -          | -          | -       |
| P_TRDY#      | VI    | VB   | -    | -          | -          | -       |
| P_STOP#      | VI    | VB   | -    | -          | -          | -       |
| P_DEVSEL#    | VI    | VB   | -    | -          | -          | -       |
| P_SERR#      | Z     | VB   | -    | -          | -          | -       |
| P_CLK        | VI    | VI   | -    | -          | -          | -       |
| P_RST#       | VI    | VI   | -    | -          | -          | -       |
| P_PERR#      | Z     | VB   | -    | -          | -          | -       |
| P_IDSEL      | VI    | VI   | -    | -          | -          | -       |
| P_INT[A:D]#  | Z     | VO   | -    | -          | -          | -       |
| P_M66EN      | VI    | VI   | -    | -          | -          | -       |
| P_BMI        | 0     | VO   | -    | -          | -          | -       |
| XINT[3:0]#   | VI    | VI   | -    | -          | -          | -       |
| HPI#         | VI    | VI   | -    | -          | -          | -       |
| GPIO[7]      | VI    | VB   | -    | -          | -          | -       |
| GPIO[6]      | VI    | VB   | -    | -          | -          | -       |
| GPIO[5]      | VI    | VB   | -    | -          | -          | -       |
| GPIO[4:0]    | VI    | VB   | -    | -          | -          | -       |
| TCK          | VI    | VI   | -    | -          | -          | -       |
| TDI          | H     | H    | -    | -          | -          | -       |
| TDO          | Z     | VO   | -    | -          | -          | -       |
| TRST#        | H     | H    | -    | -          | -          | -       |
| TMS          | H     | H    | -    | -          | -          | -       |
| PWRDELAY     | VI    | VI   | -    | -          | -          | -       |
| NC[5:0]      | H     | H    | -    | -          | -          | -       |

**NOTES:**

1 = driven to V<sub>CC</sub>  
0 = driven to V<sub>SS</sub>  
X = driven to unknown state  
ID = The input is disabled  
H = pulled up to V<sub>CC</sub>  
PD = pull-up disabled

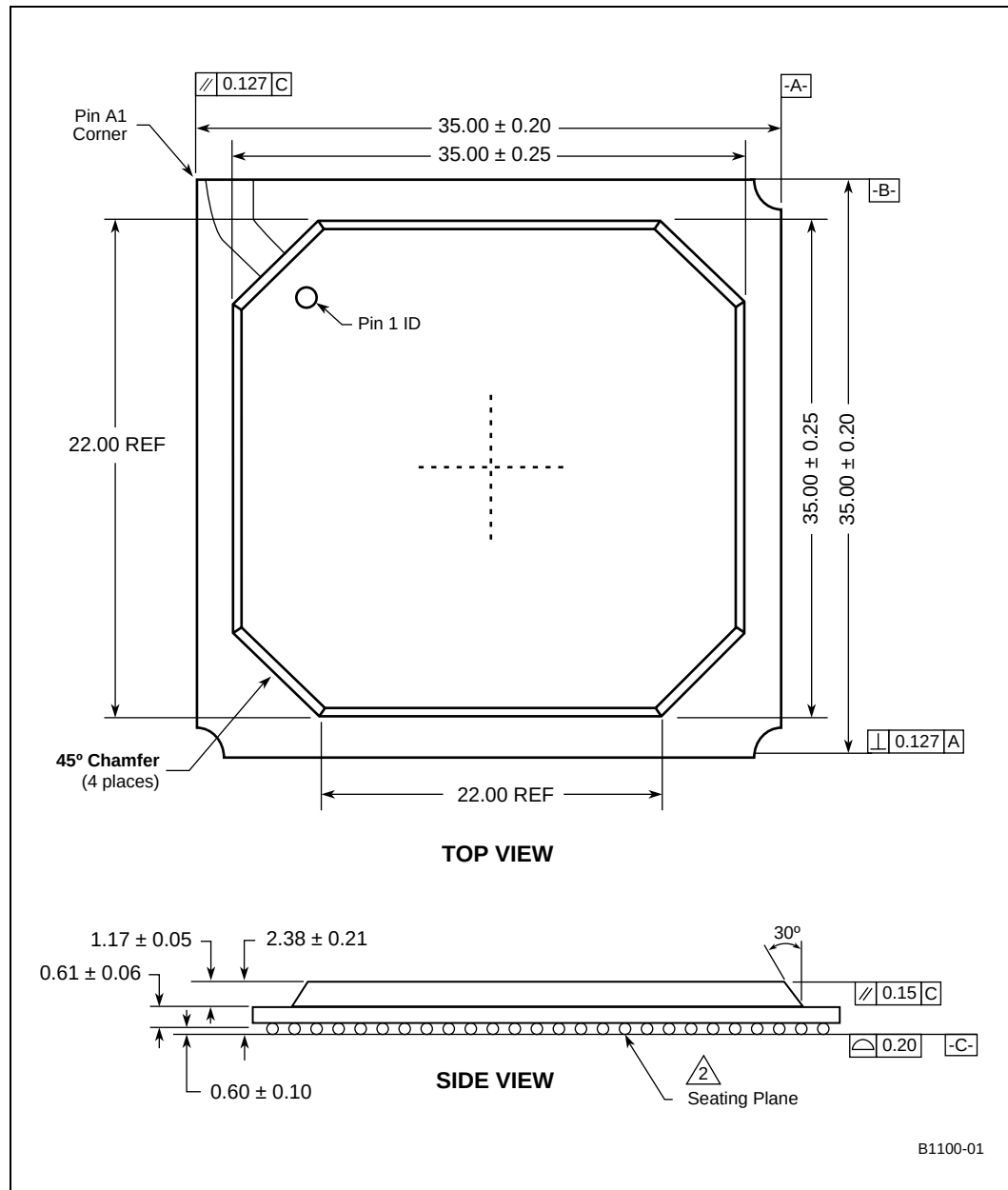
**NOTES:(continued)**

L = pulled down to V<sub>SS</sub>  
Z = output disabled (Floats)  
VB = acts like a Valid Bidirectional pin.  
VO = a Valid Output level is driven.  
VI = Need to drive a Valid Input level.  
\* = After power fail sequence completes.  
\*\* = Caused by Hi-Z from mode pins only.



### 3.1.2 544-Lead PBGA Package

**Figure 2. 544-Lead PBGA Package (Top View)**



**Figure 3. 544-Lead PBGA Package (Bottom View)**

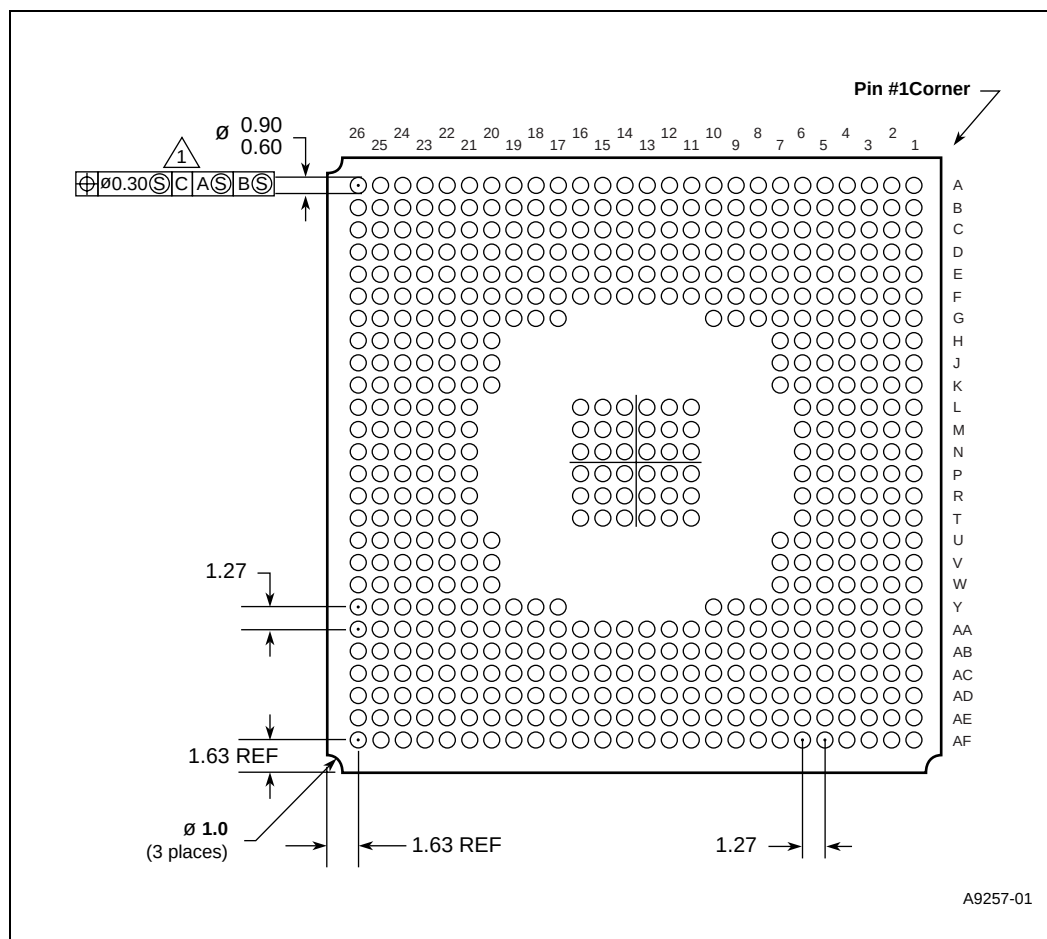


Figure 4. Ball Map - Left Side - Top View

|    | 1                     | 2                   | 3                    | 4                   | 5                  | 6                   | 7                 | 8                  | 9                | 10                   | 11                   | 12                  | 13                |
|----|-----------------------|---------------------|----------------------|---------------------|--------------------|---------------------|-------------------|--------------------|------------------|----------------------|----------------------|---------------------|-------------------|
| A  | SA1                   | DQ35                | DQ38                 | DQ34                | DQ33               | VREF                | SCB3              | SDQM <sub>8</sub>  | SCB0             | SA2                  | DQ30T                | SDQM <sub>3</sub>   | DQ28              |
| B  | SA0                   | DQ39                | VSS                  | DQS4                | VSS                | REV VENO#           | VSS               | DQS8               | VSS              | SA3                  | VSS                  | DQ29                | VSS               |
| C  | SA10                  | VSS                 | VCC25                | SDQM <sub>4</sub>   | DQ36               | VCC25               | SCB7              | SCB1               | VCC25            | SA4                  | DQ27                 | VCC25               | DQ24              |
| D  | SRAS#                 | SBA0                | SBA1                 | VSS                 | DQ37               | DQ32                | REV VENI#         | SCB2               | SCB5             | DQ31                 | DQ26                 | DQ25                | SA6               |
| E  | DQ45                  | VSS                 | DQ44                 | DQ40                | VCC25              | VSS                 | SCB6              | VSS                | SCB4             | VSS                  | DQ53                 | VSS                 | SA5               |
| F  | SDQM5                 | DQS5                | VCC25                | DQ41                | VSS                | VCC25               | VCC25             | VCC25              | VCC25            | VCC25                | VCC25                | VCC25               | VCC25             |
| G  | DQ46                  | VSS                 | DQ47                 | DQ43                | DQ42               | VCC25               | VCC13             | VCC13              | VCC13            | VCC13                |                      |                     |                   |
| H  | DQ49                  | DQ48                | SCAS#                | SWE#                | VSS                | VCC25               | VCC13             |                    |                  |                      |                      |                     |                   |
| J  | DQS6                  | VSS                 | VCC25                | DQ53                | DQ52               | VCC25               | VCC13             |                    |                  |                      |                      |                     |                   |
| K  | DQ50                  | DQ54                | SDQM6                | DQ55                | VSS                | VCC25               | VCC13             |                    |                  |                      |                      |                     |                   |
| L  | DQ60                  | VSS                 | DQ51                 | SCE1#               | SCE0#              | VCC25               |                   |                    |                  |                      | VSS                  | VSS                 | VSS               |
| M  | DQ57                  | DQ61                | VCC25                | DQ56                | VSS                | VCC25               |                   |                    |                  |                      | VSS                  | VSS                 | VSS               |
| N  | DQ62                  | VSS                 | DQ58                 | SDQM7               | DQ57               | VCC25               |                   |                    |                  |                      | VSS                  | VSS                 | VSS               |
| P  | DQ59                  | M <sub>CK2</sub> #  | M <sub>CK2</sub>     | DQ63                | VSS                | VCC25               |                   |                    |                  |                      | VSS                  | VSS                 | VSS               |
| R  | M <sub>CK1</sub>      | VSS                 | VCC13                | M <sub>CK0</sub> #  | M <sub>CK0</sub>   | VCC25               |                   |                    |                  |                      | VSS                  | VSS                 | VSS               |
| T  | M <sub>CK1</sub> #    | P <sub>INTB</sub> # | P <sub>INTA</sub> #  | R <sub>COMP</sub>   | VSS                | VCC33               |                   |                    |                  |                      | VSS                  | VSS                 | VSS               |
| U  | P <sub>INTD</sub> #   | VSS                 | R <sub>REQ</sub> #   | R <sub>INTC</sub> # | R <sub>RST</sub> # | VCC33               | VCC13             |                    |                  |                      |                      |                     |                   |
| V  | P <sub>AD31</sub>     | P <sub>GNT</sub> #  | VCC33                | P <sub>AD30</sub>   | VSS                | VCC33               | VCC13             |                    |                  |                      |                      |                     |                   |
| W  | P <sub>AD29</sub>     | VSS                 | P <sub>AD27</sub>    | P <sub>AD28</sub>   | P <sub>AD26</sub>  | VCC33               | VCC13             |                    |                  |                      |                      |                     |                   |
| Y  | P <sub>AD25</sub>     | P <sub>CBE3</sub> # | P <sub>AD24</sub>    | P <sub>IDSEL</sub>  | VSS                | VCC33               | VCC13             | VCC13              | VCC13            | VCC13                |                      |                     |                   |
| AA | P <sub>AD23</sub>     | VSS                 | VCC33                | P <sub>AD22</sub>   | P <sub>AD20</sub>  | VCC33               | VCC33             | VCC33              | VCC33            | VCC33                | VCC33                | VCC13               | VCC33             |
| AB | P <sub>AD19</sub>     | P <sub>AD21</sub>   | P <sub>AD18</sub>    | P <sub>AD16</sub>   | VSS                | P <sub>AD9</sub>    | VSS               | P <sub>AD4</sub>   | VSS              | P <sub>CBE7</sub> #  | VSS                  | P <sub>AD62</sub>   | VSS               |
| AC | P <sub>AD17</sub>     | VSS                 | P <sub>FRAME</sub> # | P <sub>TRDY</sub> # | P <sub>AD13</sub>  | P <sub>CBE0</sub> # | P <sub>CLK</sub>  | P <sub>AD2</sub>   | P <sub>AD0</sub> | P <sub>REQ64</sub> # | P <sub>PAR64</sub>   | P <sub>CBE4</sub> # | P <sub>AD58</sub> |
| AD | P <sub>CBE2</sub> #   | P <sub>STOP</sub> # | VCC33                | P <sub>AD15</sub>   | P <sub>AD11</sub>  | VCC33               | P <sub>AD6</sub>  | P <sub>M66EN</sub> | VCC33            | P <sub>AD3</sub>     | P <sub>CBE5</sub> #  | VCC33               | P <sub>AD60</sub> |
| AE | P <sub>IRDY</sub> #   | VSS                 | P <sub>PAR</sub>     | VSS                 | P <sub>AD14</sub>  | VSS                 | VCC PLL2          | VSS                | P <sub>AD7</sub> | VSS                  | P <sub>ACK64</sub> # | VSS                 | P <sub>AD61</sub> |
| AF | P <sub>DEVSEL</sub> # | P <sub>PERR</sub> # | P <sub>SERR</sub> #  | P <sub>CBE1</sub> # | VCC PLL1           | P <sub>AD12</sub>   | P <sub>AD10</sub> | P <sub>AD8</sub>   | P <sub>AD5</sub> | P <sub>AD1</sub>     | P <sub>CBE6</sub> #  | P <sub>AD63</sub>   | P <sub>AD59</sub> |
|    | 1                     | 2                   | 3                    | 4                   | 5                  | 6                   | 7                 | 8                  | 9                | 10                   | 11                   | 12                  | 13                |

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Figure 5. Ball Map - Right Side - Top View

| 14     | 15     | 16     | 17     | 18     | 19     | 20     | 21     | 22      | 23        | 24      | 25      | 26      |    |
|--------|--------|--------|--------|--------|--------|--------|--------|---------|-----------|---------|---------|---------|----|
| SA8    | DQ18   | DQS2   | DQ20   | SCKE0  | DQ14   | DQS1   | DQS8   | DQS6    | DQS0      | DQ5     | DQ0     | AD31    | A  |
| SA7    | VSS    | DQ21   | VSS    | SCKE1  | VSS    | DQ13   | VSS    | DQ2     | VSS       | DQ4     | VSS     | AD30    | B  |
| DQ23   | VCC25  | DQ17   | SA9    | VCC25  | SDQM1  | DQ12   | VCC25  | SDQM0   | DQ1       | VCC25   | AD29    | AD28    | C  |
| DQ19   | SDQM2  | DQ16   | SA11   | DQ11   | DQ15   | DQ9    | M-RST# | DQ7     | AD25      | AD27    | VSS     | AD26    | D  |
| VSS    | DQ22   | VSS    | SA12   | VSS    | DQ10   | VSS    | DQ3    | VSS     | BE3#      | AD22    | AD24    | AD23    | E  |
| VCC25  | VCC25  | VCC25  | VCC25  | VCC25  | VCC25  | VCC25  | VCC25  | BE2#    | AD21      | VCC23   | VSS     | AD20    | F  |
|        |        |        | VCC13  | VCC13  | VCC13  | VCC13  | VCC33  | VSS     | BE1#      | AD17    | AD19    | AD18    | G  |
|        |        |        |        |        |        | VCC13  | VCC33  | WIDTH 1 | AD14      | AD16    | VSS     | AD15    | H  |
|        |        |        |        |        |        | VCC13  | VCC33  | VSS     | AD11      | VCC33   | AD13    | AD12    | J  |
|        |        |        |        |        |        | VCC13  | VCC33  | WIDTH 0 | AD8       | AD10    | VSS     | AD9     | K  |
| VSS    | VSS    | VSS    |        |        |        |        | VCC33  | VSS     | BE0#      | AD5     | AD7     | AD8     | L  |
| VSS    | VSS    | VSS    |        |        |        |        | VCC13  | A3      | AD4       | VCC33   | VSS     | AD3     | M  |
| VSS    | VSS    | VSS    |        |        |        |        | VCC33  | VSS     | A2        | AD0     | AD2     | AD1     | N  |
| VSS    | VSS    | VSS    |        |        |        |        | VCC13  | FWE#    | W/R#      | ADS#    | VSS     | ALE     | P  |
| VSS    | VSS    | VSS    |        |        |        |        | VCC33  | VSS     | RDY RCV#  | VCC33   | BLAST # | DEN#    | R  |
| VSS    | VSS    | VSS    |        |        |        |        |        | PB-RST# | HOLDA     | HOLD    | VSS     | PB-CLK  | T  |
|        |        |        |        |        |        | VCC13  | VCC33  | VSS     | PCE5#     | PCE4#   | PCE3#   | PCE2#   | U  |
|        |        |        |        |        |        | VCC13  | VCC33  | PCE0#   | NC0       | VCC33   | VSS     | PCE1#   | V  |
|        |        |        |        |        |        | VCC13  | VCC33  | VSS     | GPIO7     | GPIO6   | GPIO5   | GPIO4   | W  |
|        |        |        | VCC13  | VCC13  | VCC13  | VCC13  | VCC33  | GPIO3   | GPIO2     | GPIO1   | VSS     | GPIO0   | Y  |
| VCC13  | VCC33  | VCC13  | VCC33  | VCC33  | VCC33  | VCC33  | VCC33  | VSS     | NC4       | VCC33   | VSS     | NC3     | AA |
| P-AD54 | VSS    | P-AD48 | VSS    | P-AD40 | VSS    | P-AD32 | VSS    | VCC33   | HPI#      | VSS     | VSS     | NC5     | AB |
| P-AD56 | P-AD52 | P-AD50 | P-AD44 | P-AD42 | P-AD36 | P-AD34 | TDO    | TRST#   | VSS       | XINT 3# | XINT 2# | XINT 1# | AC |
| P-AD57 | VCC33  | P-AD49 | P-AD46 | VCC33  | P-AD38 | P-AD35 | VCC33  | TCK     | NC1       | VCC33   | VSS     | XINT 0# | AD |
| VSS    | P-AD53 | VSS    | P-AD45 | VSS    | P-AD39 | VSS    | TDI    | VSS     | P-BMI     | VSS     | VCC33   | VCC33   | AE |
| P-AD55 | P-AD51 | P-AD47 | P-AD43 | P-AD41 | P-AD37 | P-AD33 | POR#   | TMS     | PWR DELAY | VCC33   | VCC33   | VCC33   | AF |
| 14     | 15     | 16     | 17     | 18     | 19     | 20     | 21     | 22      | 23        | 24      | 25      | 26      |    |

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**Table 8. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 1 of 5)**

| Ball | Signal           | Ball | Signal            | Ball | Signal            |
|------|------------------|------|-------------------|------|-------------------|
| A1   | SA1              | B13  | V <sub>SS</sub>   | C25  | AD29              |
| A2   | DQ35             | B14  | SA7               | C26  | AD28              |
| A3   | DQ38             | B15  | V <sub>SS</sub>   | D1   | SRAS#             |
| A4   | DQ34             | B16  | DQ21              | D2   | SBA0              |
| A5   | DQ33             | B17  | V <sub>SS</sub>   | D3   | SBA1              |
| A6   | V <sub>REF</sub> | B18  | SCKE1             | D4   | V <sub>SS</sub>   |
| A7   | SCB3             | B19  | V <sub>SS</sub>   | D5   | DQ37              |
| A8   | SDQM8            | B20  | DQ13              | D6   | DQ32              |
| A9   | SCB0             | B21  | V <sub>SS</sub>   | D7   | RCVENI#           |
| A10  | SA2              | B22  | DQ2               | D8   | SCB2              |
| A11  | DQ30             | B23  | V <sub>SS</sub>   | D9   | SCB5              |
| A12  | SDQM3            | B24  | DQ4               | D10  | DQ31              |
| A13  | DQ28             | B25  | V <sub>SS</sub>   | D11  | DQ26              |
| A14  | SA8              | B26  | AD30              | D12  | DQ25              |
| A15  | DQ18             | C1   | SA10              | D13  | SA6               |
| A16  | DQS2             | C2   | V <sub>SS</sub>   | D14  | DQ19              |
| A17  | DQ20             | C3   | V <sub>CC25</sub> | D15  | SDQM2             |
| A18  | SCKE0            | C4   | SDQM4             | D16  | DQ16              |
| A19  | DQ14             | C5   | DQ36              | D17  | SA11              |
| A20  | DQS1             | C6   | V <sub>CC25</sub> | D18  | DQ11              |
| A21  | DQ8              | C7   | SCB7              | D19  | DQ15              |
| A22  | DQ6              | C8   | SCB1              | D20  | DQ9               |
| A23  | DQS0             | C9   | V <sub>CC25</sub> | D21  | M_RST#            |
| A24  | DQ5              | C10  | SA4               | D22  | DQ7               |
| A25  | DQ0              | C11  | DQ27              | D23  | AD25              |
| A26  | AD31             | C12  | V <sub>CC25</sub> | D24  | AD27              |
| B1   | SA0              | C13  | DQ24              | D25  | V <sub>SS</sub>   |
| B2   | DQ39             | C14  | DQ23              | D26  | AD26              |
| B3   | V <sub>SS</sub>  | C15  | V <sub>CC25</sub> | E1   | DQ45              |
| B4   | DQS4             | C16  | DQ17              | E2   | V <sub>SS</sub>   |
| B5   | V <sub>SS</sub>  | C17  | SA9               | E3   | DQ44              |
| B6   | RCVENO#          | C18  | V <sub>CC25</sub> | E4   | DQ40              |
| B7   | V <sub>SS</sub>  | C19  | SDQM1             | E5   | V <sub>CC25</sub> |
| B8   | DQS8             | C20  | DQ12              | E6   | V <sub>SS</sub>   |
| B9   | V <sub>SS</sub>  | C21  | V <sub>CC25</sub> | E7   | SCB6              |
| B10  | SA3              | C22  | SDQM0             | E8   | V <sub>SS</sub>   |
| B11  | V <sub>SS</sub>  | C23  | DQ1               | E9   | SCB4              |
| B12  | DQ29             | C24  | V <sub>CC25</sub> | E10  | V <sub>SS</sub>   |

**Table 8. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 2 of 5)**

| Ball | Signal            | Ball | Signal            | Ball | Signal            |
|------|-------------------|------|-------------------|------|-------------------|
| E11  | DQS3              | F23  | AD21              | J1   | DQS6              |
| E12  | V <sub>SS</sub>   | F24  | V <sub>CC33</sub> | J2   | V <sub>SS</sub>   |
| E13  | SA5               | F25  | V <sub>SS</sub>   | J3   | V <sub>CC25</sub> |
| E14  | V <sub>SS</sub>   | F26  | AD20              | J4   | DQ53              |
| E15  | DQ22              | G1   | DQ46              | J5   | DQ52              |
| E16  | V <sub>SS</sub>   | G2   | V <sub>SS</sub>   | J6   | V <sub>CC25</sub> |
| E17  | SA12              | G3   | DQ47              | J7   | V <sub>CC13</sub> |
| E18  | V <sub>SS</sub>   | G4   | DQ43              | J20  | V <sub>CC13</sub> |
| E19  | DQ10              | G5   | DQ42              | J21  | V <sub>CC33</sub> |
| E20  | V <sub>SS</sub>   | G6   | V <sub>CC25</sub> | J22  | V <sub>SS</sub>   |
| E21  | DQ3               | G7   | V <sub>CC13</sub> | J23  | AD11              |
| E22  | V <sub>SS</sub>   | G8   | V <sub>CC13</sub> | J24  | V <sub>CC33</sub> |
| E23  | BE3#              | G9   | V <sub>CC13</sub> | J25  | AD13              |
| E24  | AD22              | G10  | V <sub>CC13</sub> | J26  | AD12              |
| E25  | AD24              | G17  | V <sub>CC13</sub> | K1   | DQ50              |
| E26  | AD23              | G18  | V <sub>CC13</sub> | K2   | DQ54              |
| F1   | SDQM5             | G19  | V <sub>CC13</sub> | K3   | SDQM6             |
| F2   | DQS5              | G20  | V <sub>CC13</sub> | K4   | DQ55              |
| F3   | V <sub>CC25</sub> | G21  | V <sub>CC33</sub> | K5   | V <sub>SS</sub>   |
| F4   | DQ41              | G22  | V <sub>SS</sub>   | K6   | V <sub>CC25</sub> |
| F5   | V <sub>SS</sub>   | G23  | BE1#              | K7   | V <sub>CC13</sub> |
| F6   | V <sub>CC25</sub> | G24  | AD17              | K20  | V <sub>CC13</sub> |
| F7   | V <sub>CC25</sub> | G25  | AD19              | K21  | V <sub>CC33</sub> |
| F8   | V <sub>CC25</sub> | G26  | AD18              | K22  | WIDTH0            |
| F9   | V <sub>CC25</sub> | H1   | DQ49              | K23  | AD8               |
| F10  | V <sub>CC25</sub> | H2   | DQ48              | K24  | AD10              |
| F11  | V <sub>CC25</sub> | H3   | SCAS#             | K25  | V <sub>SS</sub>   |
| F12  | V <sub>CC25</sub> | H4   | SWE#              | K26  | AD9               |
| F13  | V <sub>CC25</sub> | H5   | V <sub>SS</sub>   | L1   | DQ60              |
| F14  | V <sub>CC25</sub> | H6   | V <sub>CC25</sub> | L2   | V <sub>SS</sub>   |
| F15  | V <sub>CC25</sub> | H7   | V <sub>CC13</sub> | L3   | DQ51              |
| F16  | V <sub>CC25</sub> | H20  | V <sub>CC13</sub> | L4   | SCE1#             |
| F17  | V <sub>CC25</sub> | H21  | V <sub>CC33</sub> | L5   | SCE0#             |
| F18  | V <sub>CC25</sub> | H22  | WIDTH1            | L6   | V <sub>CC25</sub> |
| F19  | V <sub>CC25</sub> | H23  | AD14              | L11  | V <sub>SS</sub>   |
| F20  | V <sub>CC25</sub> | H24  | AD16              | L12  | V <sub>SS</sub>   |
| F21  | V <sub>CC25</sub> | H25  | V <sub>SS</sub>   | L13  | V <sub>SS</sub>   |
| F22  | BE2#              | H26  | AD15              | L14  | V <sub>SS</sub>   |

**Table 8. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 3 of 5)**

| Ball | Signal            | Ball | Signal            | Ball | Signal            |
|------|-------------------|------|-------------------|------|-------------------|
| L15  | V <sub>SS</sub>   | N21  | V <sub>CC33</sub> | R23  | RDYRCV#           |
| L16  | V <sub>SS</sub>   | N22  | V <sub>SS</sub>   | R24  | V <sub>CC33</sub> |
| L21  | V <sub>CC33</sub> | N23  | A2                | R25  | BLAST#            |
| L22  | V <sub>SS</sub>   | N24  | AD0               | R26  | DEN#              |
| L23  | BE0#              | N25  | AD2               | T1   | M_CK1#            |
| L24  | AD5               | N26  | AD1               | T2   | P_INTB#           |
| L25  | AD7               | P1   | DQ59              | T3   | P_INTA#           |
| L26  | AD6               | P2   | M_CK2#            | T4   | RCOMP             |
| M1   | DQ57              | P3   | M_CK2             | T5   | V <sub>SS</sub>   |
| M2   | DQ61              | P4   | DQ63              | T6   | V <sub>CC33</sub> |
| M3   | V <sub>CC25</sub> | P5   | V <sub>SS</sub>   | T11  | V <sub>SS</sub>   |
| M4   | DQ56              | P6   | V <sub>CC25</sub> | T12  | V <sub>SS</sub>   |
| M5   | V <sub>SS</sub>   | P11  | V <sub>SS</sub>   | T13  | V <sub>SS</sub>   |
| M6   | V <sub>CC25</sub> | P12  | V <sub>SS</sub>   | T14  | V <sub>SS</sub>   |
| M11  | V <sub>SS</sub>   | P13  | V <sub>SS</sub>   | T15  | V <sub>SS</sub>   |
| M12  | V <sub>SS</sub>   | P14  | V <sub>SS</sub>   | T16  | V <sub>SS</sub>   |
| M13  | V <sub>SS</sub>   | P15  | V <sub>SS</sub>   | T21  | V <sub>CC13</sub> |
| M14  | V <sub>SS</sub>   | P16  | V <sub>SS</sub>   | T22  | PB_RST#           |
| M15  | V <sub>SS</sub>   | P21  | V <sub>CC13</sub> | T23  | HOLDA             |
| M16  | V <sub>SS</sub>   | P22  | FWE#              | T24  | HOLD              |
| M21  | V <sub>CC13</sub> | P23  | W/R#              | T25  | V <sub>SS</sub>   |
| M22  | A3                | P24  | ADS#              | T26  | PB_CLK            |
| M23  | AD4               | P25  | V <sub>SS</sub>   | U1   | P_INTD#           |
| M24  | V <sub>CC33</sub> | P26  | ALE               | U2   | V <sub>SS</sub>   |
| M25  | V <sub>SS</sub>   | R1   | M_CK1             | U3   | P_REQ#            |
| M26  | AD3               | R2   | V <sub>SS</sub>   | U4   | P_INTC#           |
| N1   | DQ62              | R3   | V <sub>CC25</sub> | U5   | P_RST#            |
| N2   | V <sub>SS</sub>   | R4   | M_CK0#            | U6   | V <sub>CC33</sub> |
| N3   | DQ58              | R5   | M_CK0             | U7   | V <sub>CC13</sub> |
| N4   | SDQM7             | R6   | V <sub>CC25</sub> | U20  | V <sub>CC13</sub> |
| N5   | DQS7              | R11  | V <sub>SS</sub>   | U21  | V <sub>CC33</sub> |
| N6   | V <sub>CC25</sub> | R12  | V <sub>SS</sub>   | U22  | V <sub>SS</sub>   |
| N11  | V <sub>SS</sub>   | R13  | V <sub>SS</sub>   | U23  | PCE5#             |
| N12  | V <sub>SS</sub>   | R14  | V <sub>SS</sub>   | U24  | PCE4#             |
| N13  | V <sub>SS</sub>   | R15  | V <sub>SS</sub>   | U25  | PCE3#             |
| N14  | V <sub>SS</sub>   | R16  | V <sub>SS</sub>   | U26  | PCE2#             |
| N15  | V <sub>SS</sub>   | R21  | V <sub>CC33</sub> | V1   | P_AD31            |
| N16  | V <sub>SS</sub>   | R22  | V <sub>SS</sub>   | V2   | P_GNT#            |

**Table 8. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 4 of 5)**

| Ball | Signal            | Ball | Signal            | Ball | Signal            |
|------|-------------------|------|-------------------|------|-------------------|
| V3   | V <sub>CC33</sub> | Y19  | V <sub>CC13</sub> | AB5  | V <sub>SS</sub>   |
| V4   | P_AD30            | Y20  | V <sub>CC13</sub> | AB6  | P_AD9             |
| V5   | V <sub>SS</sub>   | Y21  | V <sub>CC33</sub> | AB7  | V <sub>SS</sub>   |
| V6   | V <sub>CC33</sub> | Y22  | GPIO3             | AB8  | P_AD\$            |
| V7   | V <sub>CC13</sub> | Y23  | GPIO2             | AB9  | V <sub>SS</sub>   |
| V20  | V <sub>CC13</sub> | Y24  | GPIO1             | AB10 | P_CBE7#           |
| V21  | V <sub>CC33</sub> | Y25  | V <sub>SS</sub>   | AB11 | V <sub>SS</sub>   |
| V22  | PCE0#             | Y26  | GPIO0             | AB12 | P_AD62            |
| V23  | NC0               | AA1  | P_AD23            | AB13 | V <sub>SS</sub>   |
| V24  | V <sub>CC33</sub> | AA2  | V <sub>SS</sub>   | AB14 | P_AD54            |
| V25  | V <sub>SS</sub>   | AA3  | V <sub>CC33</sub> | AB15 | V <sub>SS</sub>   |
| V26  | PCE1#             | AA4  | P_AD22            | AB16 | P_AD48            |
| W1   | P_AD29            | AA5  | P_AD20            | AB17 | V <sub>SS</sub>   |
| W2   | V <sub>SS</sub>   | AA6  | V <sub>CC33</sub> | AB18 | P_AD40            |
| W3   | P_AD27            | AA7  | V <sub>CC33</sub> | AB19 | V <sub>SS</sub>   |
| W4   | P_AD28            | AA8  | V <sub>CC33</sub> | AB20 | P_AD32            |
| W5   | P_AD26            | AA9  | V <sub>CC33</sub> | AB21 | V <sub>SS</sub>   |
| W6   | V <sub>CC33</sub> | AA10 | V <sub>CC33</sub> | AB22 | V <sub>CC33</sub> |
| W7   | V <sub>CC13</sub> | AA11 | V <sub>CC33</sub> | AB23 | HPI#              |
| W20  | V <sub>CC13</sub> | AA12 | V <sub>CC13</sub> | AB24 | V <sub>SS</sub>   |
| W21  | V <sub>CC33</sub> | AA13 | V <sub>CC33</sub> | AB25 | V <sub>SS</sub>   |
| W22  | V <sub>SS</sub>   | AA14 | V <sub>CC13</sub> | AB26 | NC3               |
| W23  | GPIO7             | AA15 | V <sub>CC33</sub> | AC1  | P_AD17            |
| W24  | GPIO6             | AA16 | V <sub>CC13</sub> | AC2  | V <sub>SS</sub>   |
| W25  | GPIO5             | AA17 | V <sub>CC33</sub> | AC3  | P_FRAME#          |
| W26  | GPIO4             | AA18 | V <sub>CC33</sub> | AC4  | P_TRDY#           |
| Y1   | P_AD25            | AA19 | V <sub>CC33</sub> | AC5  | P_AD13            |
| Y2   | P_CBE3#           | AA20 | V <sub>CC33</sub> | AC6  | P_CBE0#           |
| Y3   | P_AD24            | AA21 | V <sub>CC33</sub> | AC7  | P_CLK             |
| Y4   | P_IDSEL           | AA22 | V <sub>SS</sub>   | AC8  | P_AD2             |
| Y5   | V <sub>SS</sub>   | AA23 | NC4               | AC9  | P_AD0             |
| Y6   | V <sub>CC33</sub> | AA24 | V <sub>CC33</sub> | AC10 | P_REQ64#          |
| Y7   | V <sub>CC13</sub> | AA25 | V <sub>SS</sub>   | AC11 | P_PAR64           |
| Y8   | V <sub>CC13</sub> | AA26 | NC5               | AC12 | P_CBE4#           |
| Y9   | V <sub>CC13</sub> | AB1  | P_AD19            | AC13 | P_AD58            |
| Y10  | V <sub>CC13</sub> | AB2  | P_AD21            | AC14 | P_AD56            |
| Y17  | V <sub>CC13</sub> | AB3  | P_AD18            | AC15 | P_AD52            |
| Y18  | V <sub>CC13</sub> | AB4  | P_AD16            | AC16 | P_AD50            |



**Table 8. 544-Lead PBGA Package - Alphabetical Ball Listing (Sheet 5 of 5)**

| Ball | Signal            | Ball | Signal              | Ball | Signal              |
|------|-------------------|------|---------------------|------|---------------------|
| AC17 | P_AD44            | AD21 | V <sub>CC33</sub>   | AE24 | V <sub>SS</sub>     |
| AC18 | P_AD42            | AD22 | TCK                 | AE25 | V <sub>CC33</sub>   |
| AC19 | P_AD36            | AD23 | NC1                 | AE26 | V <sub>CC33</sub>   |
| AC20 | P_AD34            | AD24 | V <sub>CC33</sub>   | AF1  | P_DEVSEL#           |
| AC21 | TDO               | AD25 | V <sub>SS</sub>     | AF2  | P_PERR#             |
| AC22 | TRST#             | AD26 | XINT0#              | AF3  | P_SERR#             |
| AC23 | V <sub>SS</sub>   | AE1  | P_IRDY#             | AF4  | P_CBE1#             |
| AC24 | XINT3#            | AE2  | V <sub>SS</sub>     | AF5  | V <sub>CCPLL1</sub> |
| AC25 | XINT2#            | AE3  | P_PAR               | AF6  | P_AD12              |
| AC26 | XINT1#            | AE4  | V <sub>SS</sub>     | AF7  | P_AD10              |
| AD1  | P_CBE2#           | AE5  | P_AD14              | AF8  | P_AD8               |
| AD2  | P_STOP#           | AE6  | V <sub>SS</sub>     | AF9  | P_AD5               |
| AD3  | V <sub>CC33</sub> | AE7  | V <sub>CCPLL2</sub> | AF10 | P_AD1               |
| AD4  | P_AD15            | AE8  | V <sub>SS</sub>     | AF11 | P_CBE6#             |
| AD5  | P_AD11            | AE9  | P_AD7               | AF12 | P_AD63              |
| AD6  | V <sub>CC33</sub> | AE10 | V <sub>SS</sub>     | AF13 | P_AD59              |
| AD7  | P_AD6             | AE11 | P_ACK64#            | AF14 | P_AD55              |
| AD8  | P_M66EN           | AE12 | V <sub>SS</sub>     | AF15 | P_AD51              |
| AD9  | V <sub>CC33</sub> | AE13 | P_AD61              | AF16 | P_AD47              |
| AD10 | P_AD3             | AE14 | V <sub>SS</sub>     | AF17 | P_AD43              |
| AD11 | P_CBE5#           | AE15 | P_AD53              | AF18 | P_AD41              |
| AD12 | V <sub>CC33</sub> | AE16 | V <sub>SS</sub>     | AF19 | P_AD37              |
| AD13 | P_AD60            | AE17 | P_AD45              | AF20 | P_AD33              |
| AD14 | P_AD57            | AE18 | V <sub>SS</sub>     | AF21 | POR#                |
| AD15 | V <sub>CC33</sub> | AE19 | P_AD39              | AF22 | TMS                 |
| AD16 | P_AD49            | AE20 | V <sub>SS</sub>     | AF23 | PWRDELAY            |
| AD17 | P_AD46            | AE21 | TDI                 | AF24 | V <sub>CC33</sub>   |
| AD18 | V <sub>CC33</sub> | AE22 | V <sub>SS</sub>     | AF25 | V <sub>CC33</sub>   |
| AD19 | P_AD38            | AE23 | P_BMI               | AF26 | V <sub>CC33</sub>   |
| AD20 | P_AD35            |      |                     |      |                     |

**Table 9. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 1 of 5)**

| Signal | Ball | Signal | Ball | Signal | Ball |
|--------|------|--------|------|--------|------|
| A2     | N23  | BE2#   | F22  | DQ34   | A4   |
| A3     | M22  | BE3#   | E23  | DQ35   | A2   |
| AD0    | N24  | BLAST# | R25  | DQ36   | C5   |
| AD1    | N26  | DEN#   | R26  | DQ37   | D5   |
| AD2    | N25  | DQ0    | A25  | DQ38   | A3   |
| AD3    | M26  | DQ1    | C23  | DQ39   | B2   |
| AD4    | M23  | DQ2    | B22  | DQ40   | E4   |
| AD5    | L24  | DQ3    | E21  | DQ41   | F4   |
| AD6    | L26  | DQ4    | B24  | DQ42   | G5   |
| AD7    | L25  | DQ5    | A24  | DQ43   | G4   |
| AD8    | K23  | DQ6    | A22  | DQ44   | E3   |
| AD9    | K26  | DQ7    | D22  | DQ45   | E1   |
| AD10   | K24  | DQ8    | A21  | DQ46   | G1   |
| AD11   | J23  | DQ9    | D20  | DQ47   | G3   |
| AD12   | J26  | DQ10   | E19  | DQ48   | H2   |
| AD13   | J25  | DQ11   | D18  | DQ49   | H1   |
| AD14   | H23  | DQ12   | C20  | DQ50   | K1   |
| AD15   | H26  | DQ13   | B20  | DQ51   | L3   |
| AD16   | H24  | DQ14   | A19  | DQ52   | J5   |
| AD17   | G24  | DQ15   | D19  | DQ53   | J4   |
| AD18   | G26  | DQ16   | D16  | DQ54   | K2   |
| AD19   | G25  | DQ17   | C16  | DQ55   | K4   |
| AD20   | F26  | DQ18   | A15  | DQ56   | M4   |
| AD21   | F23  | DQ19   | D14  | DQ57   | M1   |
| AD22   | E24  | DQ20   | A17  | DQ58   | N3   |
| AD23   | E26  | DQ21   | B16  | DQ59   | P1   |
| AD24   | E25  | DQ22   | E15  | DQ60   | L1   |
| AD25   | D23  | DQ23   | C14  | DQ61   | M2   |
| AD26   | D26  | DQ24   | C13  | DQ62   | N1   |
| AD27   | D24  | DQ25   | D12  | DQ63   | P4   |
| AD28   | C26  | DQ26   | D11  | DQS0   | A23  |
| AD29   | C25  | DQ27   | C11  | DQS1   | A20  |
| AD30   | B26  | DQ28   | A13  | DQS2   | A16  |
| AD31   | A26  | DQ29   | B12  | DQS3   | E11  |
| ADS#   | P24  | DQ30   | A11  | DQS4   | B4   |
| ALE    | P26  | DQ31   | D10  | DQS5   | F2   |
| BE0#   | L23  | DQ32   | D6   | DQS6   | J1   |
| BE1#   | G23  | DQ33   | A5   | DQS7   | N5   |

**Table 9. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 2 of 5)**

| Signal   | Ball | Signal | Ball | Signal    | Ball |
|----------|------|--------|------|-----------|------|
| DQS8     | B8   | P_AD12 | AF6  | P_AD50    | AC16 |
| FWE#     | P22  | P_AD13 | AC5  | P_AD51    | AF15 |
| GPIO0    | Y26  | P_AD14 | AE5  | P_AD52    | AC15 |
| GPIO1    | Y24  | P_AD15 | AD4  | P_AD53    | AE15 |
| GPIO2    | Y23  | P_AD16 | AB4  | P_AD54    | AB14 |
| GPIO3    | Y22  | P_AD17 | AC1  | P_AD55    | AF14 |
| GPIO4    | W26  | P_AD18 | AB3  | P_AD56    | AC14 |
| GPIO5    | W25  | P_AD19 | AB1  | P_AD57    | AD14 |
| GPIO6    | W24  | P_AD20 | AA5  | P_AD58    | AC13 |
| GPIO7    | W23  | P_AD21 | AB2  | P_AD59    | AF13 |
| HOLD     | T24  | P_AD22 | AA4  | P_AD60    | AD13 |
| HOLDA    | T23  | P_AD23 | AA1  | P_AD61    | AE13 |
| HPI#     | AB23 | P_AD24 | Y3   | P_AD62    | AB12 |
| M_CK0    | R5   | P_AD25 | Y1   | P_AD63    | AF12 |
| M_CK0#   | R4   | P_AD26 | W5   | P_BMI     | AE23 |
| M_CK1    | R1   | P_AD27 | W3   | P_CBE0#   | AC6  |
| M_CK1#   | T1   | P_AD28 | W4   | P_CBE1#   | AF4  |
| M_CK2    | P3   | P_AD29 | W1   | P_CBE2#   | AD1  |
| M_CK2#   | P2   | P_AD30 | V4   | P_CBE3#   | Y2   |
| M_RST#   | D21  | P_AD31 | V1   | P_CBE4#   | AC12 |
| NC0      | V23  | P_AD32 | AB20 | P_CBE5#   | AD11 |
| NC1      | AD23 | P_AD33 | AF20 | P_CBE6#   | AF11 |
| NC3      | AB26 | P_AD34 | AC20 | P_CBE7#   | AB10 |
| NC4      | AA23 | P_AD35 | AD20 | P_CLK     | AC7  |
| NC5      | AA26 | P_AD36 | AC19 | P_DEVSEL# | AF1  |
| P_ACK64# | AE11 | P_AD37 | AF19 | P_FRAME#  | AC3  |
| P_AD0    | AC9  | P_AD38 | AD19 | P_GNT#    | V2   |
| P_AD1    | AF10 | P_AD39 | AE19 | P_IDSEL   | Y4   |
| P_AD2    | AC8  | P_AD40 | AB18 | P_INTA#   | T3   |
| P_AD3    | AD10 | P_AD41 | AF18 | P_INTB#   | T2   |
| P_AD4    | AB8  | P_AD42 | AC18 | P_INTC#   | U4   |
| P_AD5    | AF9  | P_AD43 | AF17 | P_INTD#   | U1   |
| P_AD6    | AD7  | P_AD44 | AC17 | P_IRDY#   | AE1  |
| P_AD7    | AE9  | P_AD45 | AE17 | P_M66EN   | AD8  |
| P_AD8    | AF8  | P_AD46 | AD17 | P_PAR     | AE3  |
| P_AD9    | AB6  | P_AD47 | AF16 | P_PAR64   | AC11 |
| P_AD10   | AF7  | P_AD48 | AB16 | P_PERR#   | AF2  |
| P_AD11   | AD5  | P_AD49 | AD16 | P_REQ#    | U3   |

**Table 9. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 3 of 5)**

| Signal   | Ball | Signal            | Ball | Signal            | Ball |
|----------|------|-------------------|------|-------------------|------|
| P_REQ64# | AC10 | SCB3              | A7   | V <sub>CC13</sub> | K20  |
| P_RST#   | U5   | SCB4              | E9   | V <sub>CC13</sub> | U7   |
| P_SERR#  | AF3  | SCB5              | D9   | V <sub>CC13</sub> | U20  |
| P_STOP#  | AD2  | SCB6              | E7   | V <sub>CC13</sub> | V7   |
| P_TRDY#  | AC4  | SCB7              | C7   | V <sub>CC13</sub> | W7   |
| PB_CLK   | T26  | SCKE0             | A18  | V <sub>CC13</sub> | W20  |
| PB_RST#  | T22  | SCKE1             | B18  | V <sub>CC13</sub> | Y7   |
| PCE0#    | V22  | SCE0#             | L5   | V <sub>CC13</sub> | Y8   |
| PCE1#    | V26  | SCE1#             | L4   | V <sub>CC13</sub> | Y9   |
| PCE2#    | U26  | SDQM0             | C22  | V <sub>CC13</sub> | Y10  |
| PCE3#    | U25  | SDQM1             | C19  | V <sub>CC13</sub> | Y17  |
| PCE4#    | U24  | SDQM2             | D15  | V <sub>CC13</sub> | Y19  |
| PCE5#    | U23  | SDQM3             | A12  | V <sub>CC13</sub> | Y20  |
| POR#     | AF21 | SDQM4             | C4   | V <sub>CC13</sub> | M21  |
| PWRDELAY | AF23 | SDQM5             | F1   | V <sub>CC13</sub> | P21  |
| RCOMP    | T4   | SDQM6             | K3   | V <sub>CC13</sub> | T21  |
| RCVENI#  | D7   | SDQM7             | N4   | V <sub>CC13</sub> | V20  |
| RCVENO#  | B6   | SDQM8             | A8   | V <sub>CC13</sub> | Y18  |
| RDYRCV#  | R23  | SRAS#             | D1   | V <sub>CC13</sub> | AA12 |
| SA0      | B1   | TCK               | AD22 | V <sub>CC13</sub> | AA14 |
| SA1      | A1   | TDI               | AE21 | V <sub>CC13</sub> | AA16 |
| SA2      | A10  | TDO               | AC21 | V <sub>CC25</sub> | C3   |
| SA3      | B10  | TMS               | AF22 | V <sub>CC25</sub> | C6   |
| SA4      | C10  | TRST#             | AC22 | V <sub>CC25</sub> | C9   |
| SA5      | E13  | V <sub>CC25</sub> | F20  | V <sub>CC25</sub> | C12  |
| SA6      | D13  | V <sub>CC13</sub> | G7   | V <sub>CC25</sub> | C15  |
| SA7      | B14  | V <sub>CC13</sub> | G8   | V <sub>CC25</sub> | C18  |
| SA8      | A14  | V <sub>CC13</sub> | G9   | V <sub>CC25</sub> | C21  |
| SA9      | C17  | V <sub>CC13</sub> | G10  | V <sub>CC25</sub> | C24  |
| SA10     | C1   | V <sub>CC13</sub> | G17  | V <sub>CC25</sub> | E5   |
| SA11     | D17  | V <sub>CC13</sub> | G18  | V <sub>CC25</sub> | F3   |
| SA12     | E17  | V <sub>CC13</sub> | G19  | V <sub>CC25</sub> | F6   |
| SBA0     | D2   | V <sub>CC13</sub> | G20  | V <sub>CC25</sub> | F7   |
| SBA1     | D3   | V <sub>CC13</sub> | H7   | V <sub>CC25</sub> | F8   |
| SCAS#    | H3   | V <sub>CC13</sub> | H20  | V <sub>CC25</sub> | F9   |
| SCB0     | A9   | V <sub>CC13</sub> | J7   | V <sub>CC25</sub> | F10  |
| SCB1     | C8   | V <sub>CC13</sub> | J20  | V <sub>CC25</sub> | F11  |
| SCB2     | D8   | V <sub>CC13</sub> | K7   | V <sub>CC25</sub> | F12  |

**Table 9. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 4 of 5)**

| Signal            | Ball | Signal              | Ball | Signal          | Ball |
|-------------------|------|---------------------|------|-----------------|------|
| V <sub>CC25</sub> | F13  | V <sub>CC33</sub>   | AB22 | V <sub>SS</sub> | B7   |
| V <sub>CC25</sub> | F14  | V <sub>CC33</sub>   | AD24 | V <sub>SS</sub> | B9   |
| V <sub>CC25</sub> | F15  | V <sub>CC33</sub>   | AA3  | V <sub>SS</sub> | B11  |
| V <sub>CC25</sub> | F16  | V <sub>CC33</sub>   | AA6  | V <sub>SS</sub> | B13  |
| V <sub>CC25</sub> | F17  | V <sub>CC33</sub>   | AA7  | V <sub>SS</sub> | B15  |
| V <sub>CC25</sub> | F18  | V <sub>CC33</sub>   | AA8  | V <sub>SS</sub> | B17  |
| V <sub>CC25</sub> | F19  | V <sub>CC33</sub>   | AA9  | V <sub>SS</sub> | B19  |
| V <sub>CC25</sub> | F21  | V <sub>CC33</sub>   | AA10 | V <sub>SS</sub> | B21  |
| V <sub>CC25</sub> | G6   | V <sub>CC33</sub>   | AA11 | V <sub>SS</sub> | B23  |
| V <sub>CC25</sub> | H6   | V <sub>CC33</sub>   | AA13 | V <sub>SS</sub> | B25  |
| V <sub>CC25</sub> | J3   | V <sub>CC33</sub>   | AA15 | V <sub>SS</sub> | C2   |
| V <sub>CC25</sub> | J6   | V <sub>CC33</sub>   | AA17 | V <sub>SS</sub> | D25  |
| V <sub>CC25</sub> | K6   | V <sub>CC33</sub>   | AA18 | V <sub>SS</sub> | D4   |
| V <sub>CC25</sub> | L6   | V <sub>CC33</sub>   | AA19 | V <sub>SS</sub> | E2   |
| V <sub>CC25</sub> | M3   | V <sub>CC33</sub>   | AA20 | V <sub>SS</sub> | E6   |
| V <sub>CC25</sub> | M6   | V <sub>CC33</sub>   | AD3  | V <sub>SS</sub> | E8   |
| V <sub>CC25</sub> | N6   | V <sub>CC33</sub>   | AD6  | V <sub>SS</sub> | E10  |
| V <sub>CC25</sub> | P6   | V <sub>CC33</sub>   | AD9  | V <sub>SS</sub> | E12  |
| V <sub>CC25</sub> | R3   | V <sub>CC33</sub>   | AD12 | V <sub>SS</sub> | E14  |
| V <sub>CC25</sub> | R6   | V <sub>CC33</sub>   | AD15 | V <sub>SS</sub> | E16  |
| V <sub>CC33</sub> | F24  | V <sub>CC33</sub>   | AD18 | V <sub>SS</sub> | E18  |
| V <sub>CC33</sub> | G21  | V <sub>CC33</sub>   | AD21 | V <sub>SS</sub> | E20  |
| V <sub>CC33</sub> | H21  | V <sub>CC33</sub>   | AE25 | V <sub>SS</sub> | E22  |
| V <sub>CC33</sub> | J21  | V <sub>CC33</sub>   | AE26 | V <sub>SS</sub> | F5   |
| V <sub>CC33</sub> | J24  | V <sub>CC33</sub>   | AF24 | V <sub>SS</sub> | F25  |
| V <sub>CC33</sub> | K21  | V <sub>CC33</sub>   | AF25 | V <sub>SS</sub> | G2   |
| V <sub>CC33</sub> | L21  | V <sub>CC33</sub>   | AF26 | V <sub>SS</sub> | G22  |
| V <sub>CC33</sub> | M24  | V <sub>CC33</sub>   | T6   | V <sub>SS</sub> | H5   |
| V <sub>CC33</sub> | N21  | V <sub>CC33</sub>   | U6   | V <sub>SS</sub> | H25  |
| V <sub>CC33</sub> | R21  | V <sub>CC33</sub>   | V3   | V <sub>SS</sub> | J2   |
| V <sub>CC33</sub> | R24  | V <sub>CC33</sub>   | V6   | V <sub>SS</sub> | J22  |
| V <sub>CC33</sub> | U21  | V <sub>CC33</sub>   | W6   | V <sub>SS</sub> | K5   |
| V <sub>CC33</sub> | V21  | V <sub>CC33</sub>   | Y6   | V <sub>SS</sub> | K25  |
| V <sub>CC33</sub> | V24  | V <sub>CCPLL1</sub> | AF5  | V <sub>SS</sub> | L2   |
| V <sub>CC33</sub> | W21  | V <sub>CCPLL2</sub> | AE7  | V <sub>SS</sub> | L11  |
| V <sub>CC33</sub> | Y21  | V <sub>REF</sub>    | A6   | V <sub>SS</sub> | L12  |
| V <sub>CC33</sub> | AA21 | V <sub>SS</sub>     | B3   | V <sub>SS</sub> | L13  |
| V <sub>CC33</sub> | AA24 | V <sub>SS</sub>     | B5   | V <sub>SS</sub> | L14  |

**Table 9. 544-Lead PBGA Package - Alphabetical Signal Listing (Sheet 5 of 5)**

| Signal          | Ball | Signal          | Ball | Signal          | Ball |
|-----------------|------|-----------------|------|-----------------|------|
| V <sub>SS</sub> | L15  | V <sub>SS</sub> | R13  | V <sub>SS</sub> | AB13 |
| V <sub>SS</sub> | L16  | V <sub>SS</sub> | R14  | V <sub>SS</sub> | AB15 |
| V <sub>SS</sub> | L22  | V <sub>SS</sub> | R15  | V <sub>SS</sub> | AB17 |
| V <sub>SS</sub> | M5   | V <sub>SS</sub> | R16  | V <sub>SS</sub> | AB19 |
| V <sub>SS</sub> | M11  | V <sub>SS</sub> | R22  | V <sub>SS</sub> | AB21 |
| V <sub>SS</sub> | M12  | V <sub>SS</sub> | T5   | V <sub>SS</sub> | AB25 |
| V <sub>SS</sub> | M13  | V <sub>SS</sub> | T11  | V <sub>SS</sub> | AC2  |
| V <sub>SS</sub> | M14  | V <sub>SS</sub> | T12  | V <sub>SS</sub> | AC23 |
| V <sub>SS</sub> | M15  | V <sub>SS</sub> | T13  | V <sub>SS</sub> | AD25 |
| V <sub>SS</sub> | M16  | V <sub>SS</sub> | T14  | V <sub>SS</sub> | AE2  |
| V <sub>SS</sub> | M25  | V <sub>SS</sub> | T15  | V <sub>SS</sub> | AE4  |
| V <sub>SS</sub> | N2   | V <sub>SS</sub> | T16  | V <sub>SS</sub> | AE6  |
| V <sub>SS</sub> | N11  | V <sub>SS</sub> | T25  | V <sub>SS</sub> | AE8  |
| V <sub>SS</sub> | N12  | V <sub>SS</sub> | U2   | V <sub>SS</sub> | AE10 |
| V <sub>SS</sub> | N13  | V <sub>SS</sub> | U22  | V <sub>SS</sub> | AE12 |
| V <sub>SS</sub> | N14  | V <sub>SS</sub> | V5   | V <sub>SS</sub> | AE14 |
| V <sub>SS</sub> | N15  | V <sub>SS</sub> | V25  | V <sub>SS</sub> | AE16 |
| V <sub>SS</sub> | N16  | V <sub>SS</sub> | W2   | V <sub>SS</sub> | AE18 |
| V <sub>SS</sub> | N22  | V <sub>SS</sub> | W22  | V <sub>SS</sub> | AE20 |
| V <sub>SS</sub> | P5   | V <sub>SS</sub> | Y5   | V <sub>SS</sub> | AE22 |
| V <sub>SS</sub> | P11  | V <sub>SS</sub> | Y25  | V <sub>SS</sub> | AE24 |
| V <sub>SS</sub> | P12  | V <sub>SS</sub> | AA2  | SWE#            | H4   |
| V <sub>SS</sub> | P13  | V <sub>SS</sub> | AA22 | WIDTH00         | K22  |
| V <sub>SS</sub> | P14  | V <sub>SS</sub> | AA25 | WIDTH01         | H22  |
| V <sub>SS</sub> | P15  | V <sub>SS</sub> | AB24 | W/R#            | P23  |
| V <sub>SS</sub> | P16  | V <sub>SS</sub> | AB5  | XINT0#          | AD26 |
| V <sub>SS</sub> | P25  | V <sub>SS</sub> | AB7  | XINT1#          | AC26 |
| V <sub>SS</sub> | R2   | V <sub>SS</sub> | AB9  | XINT2#          | AC25 |
| V <sub>SS</sub> | R11  | V <sub>SS</sub> | AB11 | XINT3#          | AC24 |
| V <sub>SS</sub> | R12  |                 |      |                 |      |

## 3.2 Package Thermal Specifications

The device is specified for operation when  $T_C$  (case temperature) is within the range of 0° C to 105° C, depending on operating conditions. Refer to the “Thermal Data for the 544-lead PBGA package” application note for more information regarding maximum case temperatures on the 544-lead PBGA package. Case temperature may be measured in any environment to determine whether the processor is within specified operating range. Measure the case temperature at the center of the top surface, opposite the ballpad.

### 3.2.1 Thermal Specifications

This section defines the terms used for thermal analysis.

#### 3.2.1.1 Ambient Temperature

Ambient temperature,  $T_A$ , is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package.

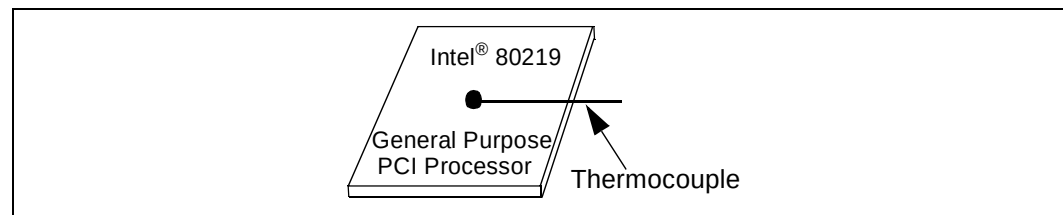
#### 3.2.1.2 Case Temperature

When measuring case temperature, attention to detail is required to ensure accuracy. When a thermocouple is used, calibrate it before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die (Figure 6). The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead at a 0° angle with respect to the package as shown in Figure 6, when no heatsink is attached.

Figure 6. Thermocouple Attachment - No Heatsink



#### 3.2.1.3 Thermal Resistance

The thermal resistance value for the case-to-ambient,  $\theta_{CA}$ , is used as a measure of the cooling solution's thermal performance.

### 3.2.2 Thermal Analysis

Table 10 lists the case-to-ambient thermal resistances of the 80219 for different air flow rates with and without a heat sink.

To calculate  $T_A$ , the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P (\theta_{CA})$$

Compute P by multiplying  $I_{CC}$  and  $V_{CC}$ . Values for  $\theta_{JC}$  and  $\theta_{CA}$  are given in Table 10.

Junction temperature ( $T_J$ ) is commonly used in reliability calculations.  $T_J$  may be calculated from  $\theta_{JC}$  (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P (\theta_{JC})$$

Similarly, when  $T_A$  is known, the corresponding case temperature ( $T_C$ ) may be calculated as follows:

$$T_C = T_A + P (\theta_{CA})$$

The  $\theta_{JA}$  (Junction to Ambient) for this package is currently estimated at 16.87° C/Watt with no airflow and no heatsink.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

**Table 10. 544-Lead PBGA Package Thermal Characteristics**

| Thermal Resistance — ° C/Watt                       |                          |              |               |               |               |               |               |               |
|-----------------------------------------------------|--------------------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Parameter                                           | Airflow — ft/min (m/sec) |              |               |               |               |               |               |               |
|                                                     | 0<br>(0)                 | 50<br>(0.25) | 100<br>(0.50) | 200<br>(1.01) | 300<br>(1.52) | 400<br>(2.03) | 600<br>(3.04) | 800<br>(4.06) |
| $\Psi_{JT}$ (Junction-to-Case)                      | 1.00                     | 1.00         | 1.00          | 1.00          | 1.00          | 1.00          | 1.00          | 1.00          |
| $\theta_{CA}$ (Case-to-Ambient)<br>Without Heatsink | 15.87                    | 14.72        | 13.99         | 12.94         | 12.20         | 11.73         | 10.90         | 10.39         |

**NOTES:**

1. This table applies to a H-PBGA device soldered directly onto a board.
2. Estimated value.



### 3.3 Socket Information

Table 11 and Table 12 provide vendor details for socket-headers and burn-in sockets for the 80219. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

#### 3.3.1 Socket-Header Vendor

Table 11. Socket-Header Vendor

| Company                                                                | Factory Representative | Phone/Fax #                  | Part #             |                            |
|------------------------------------------------------------------------|------------------------|------------------------------|--------------------|----------------------------|
|                                                                        |                        |                              | BGA 544-Pin Header | BGA 544-Pin Socket Carrier |
| Adapter Technologies<br>214-218 South 4th Street<br>Perkasie, PA 18944 | John Miller            | 215 258-5750<br>215 258-5760 | TBD                | TBD                        |

#### 3.3.2 Burn-in Socket Vendor

Table 12. Burn-in Socket Vendor

| Company                                            | Factory Representative | Phone # | Burn-in Socket Part #    |
|----------------------------------------------------|------------------------|---------|--------------------------|
| Yamaichi<br>2235 Zanker Road<br>San Jose, CA 95131 | Steve Drake            | TBD     | NP276-67613.<br>AC-14847 |

#### 3.3.3 Shipping Tray Vendor

Table 13. Shipping Tray Vendor

| Company              | Factory Representative | Phone #        | Shipping Tray Part # |
|----------------------|------------------------|----------------|----------------------|
| Daewon Semiconductor | Sunna Chung            | 82.31.794.2001 | 127-3535-919, Rev. D |

#### 3.3.4 Logic Analyzer Interposer Vendor

Table 14. Logic Analyzer Interposer Vendor

| Company                                                                        | Factory Representative | Phone/Fax #                  | Part # |
|--------------------------------------------------------------------------------|------------------------|------------------------------|--------|
| Delphi Connection Systems<br>17150 Von Karmann Avenue<br>Irvine, CA 92614-0968 | Bob Betz               | 949 660-6968<br>949 660-5825 | TBD    |

### 3.3.5 JTAG Emulator Vendor

**Table 15. Logic Analyzer Interposer Vendor**

| Company                                                                        | Factory Representative | Phone/Fax #                  | Part # |
|--------------------------------------------------------------------------------|------------------------|------------------------------|--------|
| Delphi Connection Systems<br>17150 Von Karmann Avenue<br>Irvine, CA 92614-0968 | Bob Betz               | 949 660-6968<br>949 660-5825 | TBD    |

### 3.3.6 Heat Sink Vendor

**Table 16. Heat Sink Vendor**

| Company | Part # |
|---------|--------|
| TBD     | TBD    |

For extended temperature operation, a heat sink may be required. Thermal simulations and analyses will need to be performed to determine the heat sink requirements for the specific application.

## 4.0 Electrical Specifications

### 4.1 Absolute Maximum Ratings

| Parameter                               | Maximum Rating              | <b>NOTICE:</b> The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design. |
|-----------------------------------------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Storage Temperature                     | –55° C to +125° C           |                                                                                                                                             |
| Case Temperature Under Bias             | 0° C to +105° C             |                                                                                                                                             |
| Supply Voltage $V_{CC33}$ wrt. $V_{SS}$ | –0.5 V to +4.1 V            |                                                                                                                                             |
| Supply Voltage $V_{CC25}$ wrt. $V_{SS}$ | –0.5 V to +3.6 V            |                                                                                                                                             |
| Supply Voltage $V_{CC13}$ wrt. $V_{SS}$ | –0.5 V to +2.1 V            |                                                                                                                                             |
| Voltage on Any Ball wrt. $V_{SS}$       | –0.5 V to $V_{CCP} + 0.5$ V |                                                                                                                                             |

**†WARNING:** Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

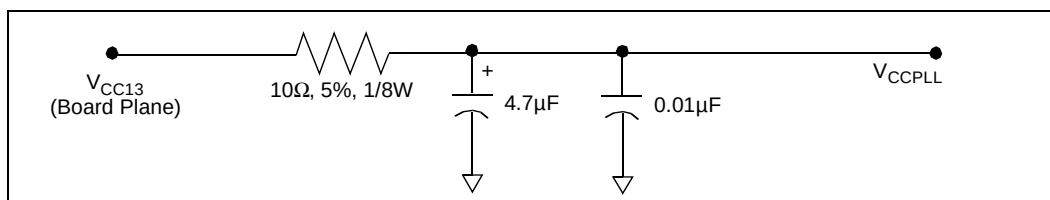
Table 17. Operating Conditions

| Symbol       | Parameter                    | Min                  | Max                 | Units | Notes |
|--------------|------------------------------|----------------------|---------------------|-------|-------|
| $V_{CC33}$   | 3.3 V PCI Supply Voltage     | 3.0                  | 3.6                 | V     |       |
| $V_{CC25}$   | 2.5 V DDR Supply Voltage     | 2.375                | 2.7                 | V     |       |
| $V_{CC13}$   | 1.3 V CORE Supply Voltage    | 1.235                | 1.365               | V     |       |
| $V_{CCPLL1}$ | PLL Supply Voltage           | $V_{CC13}$           | $V_{CC13}$          | V     |       |
| $V_{CCPLL2}$ | PLL Supply Voltage           | $V_{CC13}$           | $V_{CC13}$          | V     |       |
| $V_{REF}$    | Memory I/O Reference Voltage | $V_{CC25}/2 - 0.013$ | $V_{CC25}/2 + 0.05$ | V     |       |
| $F_P\_CLK$   | Input Clock Frequency        | 16                   | 133                 | MHz   |       |
| $T_C$        | Case Temperature Under Bias  | 0                    | 105                 | °C    |       |

### 4.2 $V_{CCPLL}$ Pin Requirements

To reduce clock skew, the  $V_{CCPLL1}$ ,  $V_{CCPLL2}$ ,  $V_{SSPLL1}$  and  $V_{SSPLL2}$  balls for the Phase Lock Loop (PLL) circuit are isolated on the package. The lowpass filter, as shown in Figure 7, reduces noise induced clock jitter and its effects on timing relationships in system designs. The 4.7  $\mu$ F capacitor must be (low ESR solid tantalum), the 0.01  $\mu$ F capacitor must be of the type X7R and the node connecting  $V_{CCPLL}$  must be as short as possible. The  $V_{SSPLL}$  balls should be connected to the board ground plane.

Figure 7.  $V_{CCPLL}$  Lowpass Filter



## 4.3 Targeted DC Specifications

Table 18. DC Characteristics

| Symbol    | Parameter                      | Min              | Max              | Units | Notes                              |
|-----------|--------------------------------|------------------|------------------|-------|------------------------------------|
| $V_{IL1}$ | Input Low Voltage (SDRAM)      | -0.3             | $V_{REF} - 0.15$ | V     | 3, 5                               |
| $V_{IH1}$ | Input High Voltage (SDRAM)     | $V_{REF} + 0.15$ | $V_{CC25} + 0.3$ | V     | 3, 5                               |
| $V_{IL2}$ | Input Low Voltage (Misc.)      | -0.3             | 0.8              | V     | 4                                  |
| $V_{IH2}$ | Input High Voltage (Misc.)     | 2.0              | $V_{CC33} + 0.3$ | V     | 4                                  |
| $V_{IL3}$ | Input Low Voltage (PCI-X)      | -0.5             | $0.35 V_{CC33}$  | V     | 1                                  |
| $V_{IH3}$ | Input High Voltage (PCI-X/PCI) | $0.5 V_{CC33}$   | $V_{CC33} + 0.5$ | V     | 1                                  |
| $V_{IL4}$ | Input Low Voltage (PCI)        | -0.5             | $0.3 V_{CC33}$   | V     | 1                                  |
| $V_{OL1}$ | Output Low Voltage (Misc.)     |                  | 0.4              | V     | $I_{OL} = 6 \text{ mA}$ (4)        |
| $V_{OH1}$ | Output High Voltage (Misc.)    | 2.4              |                  | V     | $I_{OH} = -2 \text{ mA}$ (4)       |
| $V_{OL2}$ | Output Low Voltage (SDRAM)     |                  | 0.35             | V     | $I_{OL} = 15.2 \text{ mA}$ (3, 5)  |
| $V_{OH2}$ | Output High Voltage (SDRAM)    | 1.95             |                  | V     | $I_{OH} = -15.2 \text{ mA}$ (3, 5) |
| $V_{OL3}$ | Output Low Voltage (PCI-X)     |                  | $0.1 V_{CC33}$   | V     | $I_{OL} = 1500 \mu\text{A}$ (1)    |
| $V_{OH3}$ | Output HIGH Voltage (PCI-X)    | $0.9 V_{CC33}$   |                  | V     | $I_{OH} = -500 \mu\text{A}$ (1)    |
| $C_{IN}$  | Input pin Capacitance          |                  | 8                | pF    | 1, 2                               |
| $C_{CLK}$ | Clock pin Capacitance          | 5                | 8                | pF    | 1, 2                               |
| $L_{PIN}$ | Ball Inductance                |                  | 15               | nH    | 1, 2                               |

**NOTES:**

1. As required by the PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a.
2. Not tested.
3. SDRAM signals include **MA[12:0]**, **BA[1:0]**, **CAS#**, **CS[1:0]#**, **CKE[1:0]**, **DM[8:0]**, **RAS#**, **WE#**, **RCVENI#**, **RCVENO#**, **M\_CK[2:0]**, **M\_CK[2:0]#**, **DQ[63:0]**, **DQS[8:0]** and **CB[7:0]**.
4. Miscellaneous signals include all signals that are not PCI or SDRAM signals.
5. Only 2.5 V DDR SDRAM is supported.

Table 19.  $I_{CC}$  Characteristics

| Symbol                           | Parameter                                                                                          | Typ  | Max     | Units   | Notes                     |
|----------------------------------|----------------------------------------------------------------------------------------------------|------|---------|---------|---------------------------|
| $I_{LI1}$                        | Input Leakage Current for each signal except <b>TCK</b> , <b>TMS</b> , <b>TRST#</b> , <b>TDI</b> . |      | $\pm 2$ | $\mu A$ | $0 < V_{IN} < V_{CC}$ (1) |
| $I_{LI2}$                        | Input Leakage Current for <b>TCK</b> , <b>TMS</b> , <b>TRST#</b> , <b>TDI</b> .                    | -140 | -250    | $\mu A$ | $V_{IN} = 0.45 V$ (1)     |
| $I_{CC13}$ Active (Thermal)      | Core and Analog Current – 600 MHz.                                                                 | 1.2  |         | A       | (2)                       |
| $I_{CC13}$ Active (Thermal)      | Core and Analog Current – 400 MHz.                                                                 | 1.08 |         | A       | (2)                       |
| $I_{CC25}$ Active (Thermal)      | DDR Current – 200 MHz at 2.5 V.                                                                    | 0.38 |         | A       | (2)                       |
| $I_{CC33}$ Active (Thermal)      | PCI/PBI Current – 100 MHz/133 MHz at 3.3 V.                                                        | 0.34 |         | A       | (2)                       |
| $I_{CC13}$ Active (Power Supply) | Core and Analog Current – 600 MHz                                                                  |      | 1.72    | A       | (3)                       |
| $I_{CC13}$ Active (Power Supply) | Core and Analog Current – 400 MHz                                                                  |      | 1.55    | A       | (3)                       |
| $I_{CC25}$ Active (Power Supply) | DDR Current – 200 MHz at 2.5 V                                                                     |      | 0.42    | A       | (3)                       |
| $I_{CC33}$ Active (Power Supply) | PCI/PBI Current – 100 MHz/133 MHz at 3.3 V                                                         |      | 0.36    | A       | (3)                       |

**NOTES:**

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs with tri-state outputs.
2.  $I_{CC}$  Active (Thermal) value is provided for system thermal management. Typical  $I_{CC}$  is measured with  $V_{CC13} = 1.3 V$ ,  $V_{CC25} = 2.5 V$ ,  $V_{CC33} = 3.3 V$  and ambient temperature = 55°C.
3.  $I_{CC}$  Active (Power Supply) value is provided for selecting system power supply. It is measured using one of the worst case instruction mixes with  $V_{CC13} = 1.365 V$ ,  $V_{CC25} = 2.75 V$ ,  $V_{CC33} = 3.63 V$  and ambient temperature = 55°C.

## 4.4 Targeted AC Specifications

### 4.4.1 Clock Signal Timings

Table 20. Clock Timings

| Symbol                       | Parameter                                                       | PCI-X 133 |     | PCI-X 100 |     | PCI-X 66 |      | PCI 66 |      | PCI 33 |      | Units | Notes |
|------------------------------|-----------------------------------------------------------------|-----------|-----|-----------|-----|----------|------|--------|------|--------|------|-------|-------|
|                              |                                                                 | Min       | Max | Min       | Max | Min      | Max  | Min    | Max  | Min    | Max  |       |       |
| T <sub>F1</sub>              | PCI clock Frequency                                             | 100       | 133 | 66        | 100 | 50       | 66   | 33     | 66   | 16     | 33   | MHz   | 1     |
| T <sub>C1</sub>              | PCI clock Cycle Time                                            | 7.5       | 10  | 10        | 15  | 15       | 20   | 15     | 30   | 30     | 60   | ns    | 1, 3  |
| T <sub>CH1</sub>             | PCI clock High Time                                             | 3         |     | 3         |     | 6        |      | 6      |      | 11     |      | ns    |       |
| T <sub>CL1</sub>             | PCI clock Low Time                                              | 3         |     | 3         |     | 6        |      | 6      |      | 11     |      | ns    |       |
| T <sub>SR1</sub>             | PCI clock Slew Rate                                             | 1.5       | 4   | 1.5       | 4   | 1.5      | 4    | 1.5    | 4    | 1      | 4    | V/ns  | 2     |
| Spread Spectrum Requirements |                                                                 |           |     |           |     |          |      |        |      |        |      |       |       |
| f <sub>mod</sub>             | PCI clock modulation frequency                                  | 30        | 33  | 30        | 33  | 30       | 33   | 30     | 33   |        |      | KHz   |       |
| f <sub>spread</sub>          | PCI clock frequency spread                                      | -1        | 0   | -1        | 0   | -1       | 0    | -1     | 0    |        |      | %     |       |
| Symbol                       | Parameter                                                       |           |     |           |     |          |      | PC200  |      |        |      | Units | Notes |
|                              |                                                                 |           |     |           |     |          |      | Min    |      | Max    |      |       |       |
| T <sub>F2</sub>              | DDR SDRAM clock Frequency                                       |           |     |           |     |          |      |        |      | 100    |      | MHz   |       |
| T <sub>C2</sub>              | DDR SDRAM clock Cycle Time                                      |           |     |           |     |          |      | 10     |      |        |      | ns    |       |
| T <sub>CH2</sub>             | DDR SDRAM clock High Time                                       |           |     |           |     |          |      | 4.5    |      | 5.5    |      | ns    |       |
| T <sub>CL2</sub>             | DDR SDRAM clock Low Time                                        |           |     |           |     |          |      | 4.5    |      | 5.5    |      | ns    |       |
| T <sub>CS2</sub>             | DDR SDRAM clock Period Stability                                |           |     |           |     |          |      |        |      | ± 90   |      | ps    |       |
| T <sub>skew2</sub>           | DDR SDRAM clock skew for <b>M_CK[2:0]</b> and <b>M_CK[2:0]#</b> |           |     |           |     |          |      |        |      | 200    |      | ps    |       |
| Symbol                       | Parameter                                                       |           |     |           |     | PBI 100  |      | PBI 66 |      | PBI 33 |      | Units | Notes |
|                              |                                                                 |           |     |           |     | Min      | Max  | Min    | Max  | Min    | Max  |       |       |
| T <sub>F3</sub>              | PBI clock Frequency                                             |           |     |           |     |          | 100  |        | 66   |        | 33   | MHz   |       |
| T <sub>C3</sub>              | PBI clock Cycle Time                                            |           |     |           |     | 10       |      | 15     |      | 30     |      | ns    |       |
| T <sub>CH3</sub>             | PBI clock High Time                                             |           |     |           |     | 3        |      | 6      |      | 11     |      | ns    |       |
| T <sub>CL3</sub>             | PBI clock Low Time                                              |           |     |           |     | 3        |      | 6      |      | 11     |      | ns    |       |
| T <sub>CS3</sub>             | PBI clock Period Stability                                      |           |     |           |     |          | ± 90 |        | ± 90 |        | ± 90 | ps    |       |

**NOTES:**

1. The clock frequency may not change beyond the spread-spectrum limits except while P<sub>\_RST</sub># is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

## 4.4.2 PCI Interface Signal Timings

Table 21. PCI Signal Timings

| Symbol           | Parameter                                              | PCI-X 133<br>PCI-X 100 |     | PCI-X 66 |     | PCI 66 |     | PCI 33 |     | Units  | Notes   |
|------------------|--------------------------------------------------------|------------------------|-----|----------|-----|--------|-----|--------|-----|--------|---------|
|                  |                                                        | Min                    | Max | Min      | Max | Min    | Max | Min    | Max |        |         |
| T <sub>OV1</sub> | Clock to Output Valid Delay for bused signals          | 0.7                    | 3.8 | 0.7      | 3.8 | 1      | 6   | 2      | 11  | ns     | 1, 2, 3 |
| T <sub>OV2</sub> | Clock to Output Valid Delay for point to point signals | 0.7                    | 3.8 | 0.7      | 3.8 | 2      | 6   | 2      | 12  | ns     | 1, 2, 3 |
| T <sub>OF</sub>  | Clock to Output Float Delay                            |                        | 7   |          | 7   |        | 14  |        | 28  | ns     | 1, 7    |
| T <sub>IS1</sub> | Input Setup to clock for bused signals                 | 1.2                    |     | 1.7      |     | 3      |     | 7      |     | ns     | 3, 4, 8 |
| T <sub>IS2</sub> | Input Setup to clock for point to point signals        | 1.2                    |     | 1.7      |     | 5      |     | 10, 12 |     | ns     | 3, 4    |
| T <sub>IH1</sub> | Input Hold time from clock                             | 0.5                    |     | 0.5      |     | 0      |     | 0      |     | ns     | 4       |
| T <sub>RST</sub> | Reset Active Time                                      | 1                      |     | 1        |     | 1      |     | 1      |     | ms     |         |
| T <sub>RF</sub>  | Reset Active to output float delay                     |                        | 40  |          | 40  |        | 40  |        | 40  | ns     | 5, 6    |
| T <sub>IS3</sub> | REQ64# to Reset setup time                             | 10                     |     | 10       |     | 10     |     | 10     |     | clocks |         |
| T <sub>IH2</sub> | Reset to REQ64# hold time                              | 0                      | 50  | 0        | 50  | 0      | 50  | 0      | 50  | ns     |         |
| T <sub>IS4</sub> | PCI-X initialization pattern to Reset setup time       | 10                     |     | 10       |     |        |     |        |     | clocks |         |
| T <sub>IH3</sub> | Reset to PCI-X initialization pattern hold time        | 0                      | 50  | 0        | 50  |        |     |        |     | ns     |         |

**NOTES:**

1. See the timing measurement conditions in Figure 9 "Output Timing Measurement Waveforms" on page 51.
2. See Figure 15 "PCI/PCI-X TOV(max) Rising Edge AC Test Load" on page 55, Figure 16 "PCI/PCI-X TOV(max) Falling Edge AC Test Load" on page 55 and Figure 17 "PCI/PCI-X TOV(min) AC Test Load" on page 56.
3. Setup time for point-to-point signals applies to REQ# and GNT# only. All other signals are bused.
4. See the timing measurement conditions in Figure 10 "Input Timing Measurement Waveforms" on page 52.
5. RST# is asserted and deasserted asynchronously with respect to CLK.
6. All output drivers must be floated when RST# is active.
7. For purposes of Active/Float timing measurements, the HI-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

### 4.4.3 DDR SDRAM Interface Signal Timings

Table 22. DDR SDRAM Signal Timings

| Symbol           | Parameter                                             | Min | Max | Units | Notes |
|------------------|-------------------------------------------------------|-----|-----|-------|-------|
| T <sub>VB1</sub> | DQ, CB and DM output valid time before associated DQS | 1.3 |     | ns    | 4     |
| T <sub>VA1</sub> | DQ, CB and DM output valid time after associated DQS  | 1.3 |     | ns    | 4     |
| T <sub>VB2</sub> | DQS output valid time before M_CLK                    |     | 1.4 | ns    | 4     |
| T <sub>VA2</sub> | DQS output valid time after M_CLK                     |     | 1.0 | ns    | 4     |
| T <sub>VB3</sub> | Address and Control write output valid before M_CLK   | 4.2 |     | ns    | 4     |
| T <sub>VA3</sub> | Address and Control write output valid after M_CLK    | 3.3 |     | ns    | 4     |
| T <sub>VB4</sub> | DQS read input valid time before DQ                   |     | 1.6 | ns    | 5     |
| T <sub>VA4</sub> | DQS read input valid time after DQ                    |     | 1.6 | ns    | 5     |
| T <sub>VB5</sub> | RCVENO# output valid time before M_CLK                |     | 1.4 | ns    | 5     |
| T <sub>VA5</sub> | RCVENO# output valid time after M_CLK                 |     | 1.0 | ns    | 5     |
| T <sub>VB6</sub> | RCVENI# input valid time before DQS                   | 3.0 |     | ns    | 5     |
| T <sub>VA6</sub> | RCVENI# hold from DQS valid                           | 0.8 |     | ns    | 5     |

**NOTES:**

1. See Figure 9 "Output Timing Measurement Waveforms" on page 51.
2. See Figure 10 "Input Timing Measurement Waveforms" on page 52.
3. These output valid times are specified with a 0 pF loading.
4. See Figure 12 "DDR SDRAM Write Timings" on page 53.
5. See Figure 13 "DDR SDRAM Read Timings" on page 54.

### 4.4.4 Peripheral Bus Interface Signal Timings

Table 23. Peripheral Bus Signal Timings

| Sym              | Parameter                      | Min | Max | Units | Notes |
|------------------|--------------------------------|-----|-----|-------|-------|
| T <sub>OV1</sub> | Output Valid Delay from PB_CLK | 1   | 5.5 | ns    | 1, 3  |
| T <sub>OF</sub>  | Output Float Delay from PB_CLK | 1   | 5.5 | ns    | 1, 3  |
| T <sub>IS1</sub> | Input Setup to PB_CLK          | 4.9 |     | ns    | 2     |
| T <sub>IH1</sub> | Input Hold from PB_CLK         | 2   |     | ns    | 2     |

**NOTES:**

1. See Figure 9 "Output Timing Measurement Waveforms" on page 51.
2. See Figure 10 "Input Timing Measurement Waveforms" on page 52.
3. See Figure 14 "AC Test Load for all Signals Except PCI and DDR SDRAM" on page 55.



## 4.4.5 I<sup>2</sup>C Interface Signal Timings

Table 24. I<sup>2</sup>C Signal Timings

| Symbol             | Parameter                                      | Std. Mode |      | Fast Mode            |     | Units | Notes |
|--------------------|------------------------------------------------|-----------|------|----------------------|-----|-------|-------|
|                    |                                                | Min       | Max  | Min                  | Max |       |       |
| F <sub>SCL</sub>   | SCL Clock Frequency                            | 0         | 100  | 0                    | 400 | KHz   |       |
| T <sub>BUF</sub>   | Bus Free Time Between STOP and START Condition | 4.7       |      | 1.3                  |     | μs    | 1     |
| T <sub>HDSTA</sub> | Hold Time (repeated) START Condition           | 4         |      | 0.6                  |     | μs    | 1, 3  |
| T <sub>LOW</sub>   | SCL Clock Low Time                             | 4.7       |      | 1.3                  |     | μs    | 1, 2  |
| T <sub>HIGH</sub>  | SCL Clock High Time                            | 4         |      | 0.6                  |     | μs    | 1, 2  |
| T <sub>SUSTA</sub> | Setup Time for a Repeated START Condition      | 4.7       |      | 0.6                  |     | μs    | 1     |
| T <sub>HDDAT</sub> | Data Hold Time                                 | 0         | 3.45 | 0                    | 0.9 | μs    | 1     |
| T <sub>SUDAT</sub> | Data Setup Time                                | 250       |      | 100                  |     | ns    | 1     |
| T <sub>SR</sub>    | SCL and SDA Rise Time                          |           | 1000 | 20+0.1C <sub>b</sub> | 300 | ns    | 1, 4  |
| T <sub>SF</sub>    | SCL and SDA Fall Time                          |           | 300  | 20+0.1C <sub>b</sub> | 300 | ns    | 1, 4  |
| T <sub>SUSTO</sub> | Setup Time for STOP Condition                  | 4         |      | 0.6                  |     | μs    | 1     |

**NOTES:**

1. See Figure 11 "I<sup>2</sup>C Interface Signal Timings" on page 52.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C<sub>b</sub> = the total capacitance of one bus line, in pF.

## 4.4.6 Boundary Scan Test Signal Timings

Table 25. Boundary Scan Test Signal Timings

| Symbol             | Parameter                                                       | Min | Max | Units | Notes                 |
|--------------------|-----------------------------------------------------------------|-----|-----|-------|-----------------------|
| T <sub>BSF</sub>   | <b>TCK</b> Frequency                                            | 0   | 66  | MHz   |                       |
| T <sub>BSCH</sub>  | <b>TCK</b> High Time                                            | 7.5 |     | ns    | Measured at 1.5 V (1) |
| T <sub>BSCL</sub>  | <b>TCK</b> Low Time                                             | 7.5 |     | ns    | Measured at 1.5 V (1) |
| T <sub>BSCR</sub>  | <b>TCK</b> Rise Time                                            |     | 5   | ns    | 0.8 V to 2.0 V (1)    |
| T <sub>BSCF</sub>  | <b>TCK</b> Fall Time                                            |     | 5   | ns    | 2.0 V to 0.8 V (1)    |
| T <sub>BSIS1</sub> | Input Setup to <b>TCK</b>                                       | 3   |     | ns    | 4                     |
| T <sub>BSIH1</sub> | Input Hold from <b>TCK</b>                                      | 3   |     | ns    | 4                     |
| T <sub>BSOV1</sub> | <b>TDO</b> Output Valid Delay from falling edge of <b>TCK</b> . | 1   | 11  | ns    | 2, 3                  |
| T <sub>OF1</sub>   | <b>TDO</b> Output Float Delay from falling edge of <b>TCK</b> . | 1   | 11  | ns    | 2, 5                  |

**NOTES:**

1. Not tested.
2. Outputs precharged to V<sub>CC5</sub>.
3. See [Figure 9 “Output Timing Measurement Waveforms” on page 51.](#)
4. See [Figure 10 “Input Timing Measurement Waveforms” on page 52.](#)
5. A float condition occurs when the output current becomes less than I<sub>LO</sub>. Float delay is not tested. See [Figure 9 “Output Timing Measurement Waveforms” on page 51.](#)

## 4.5 AC Timing Waveforms

Figure 8. Clock Timing Measurement Waveforms

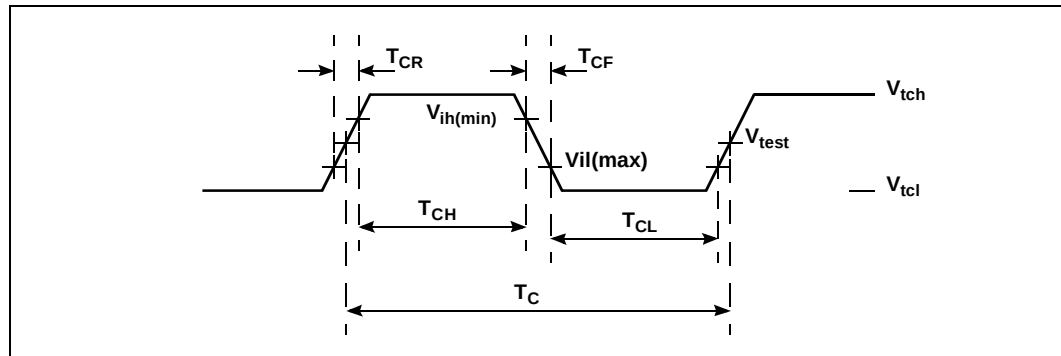


Figure 9. Output Timing Measurement Waveforms

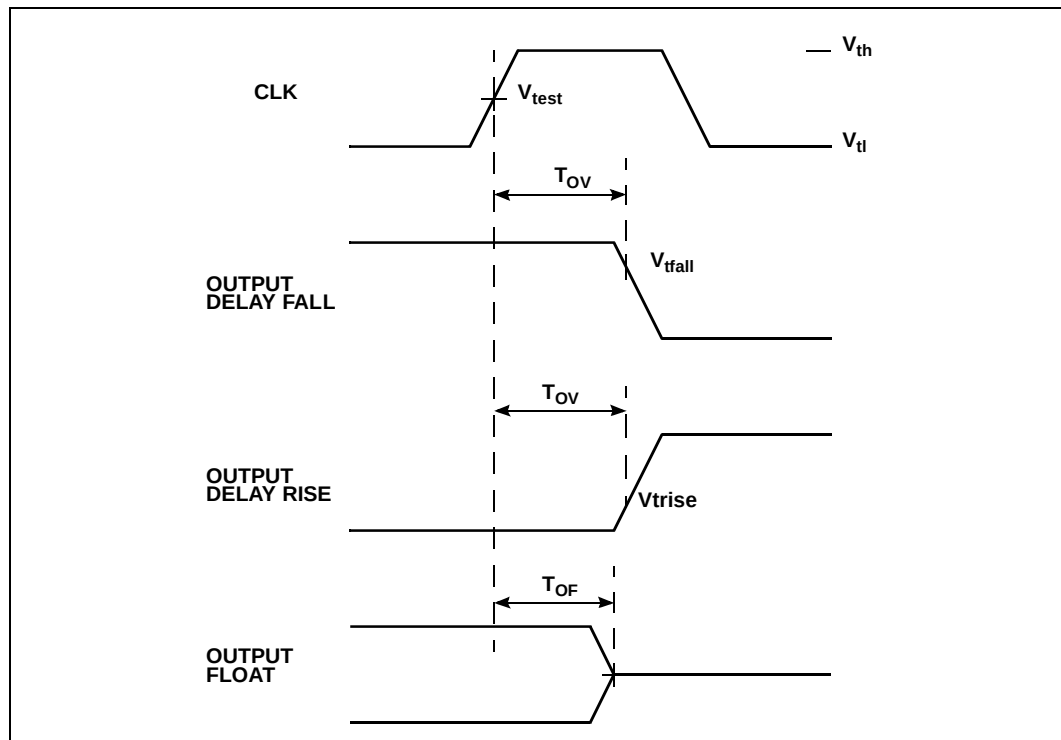


Figure 10. Input Timing Measurement Waveforms

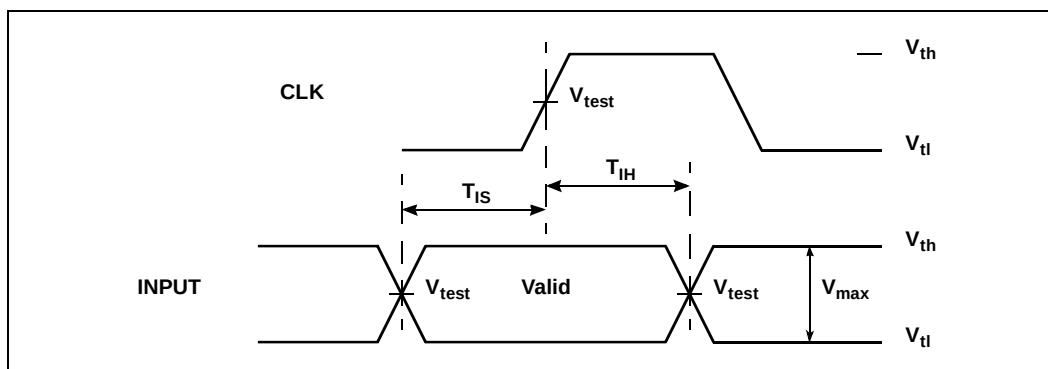


Figure 11. I<sup>2</sup>C Interface Signal Timings

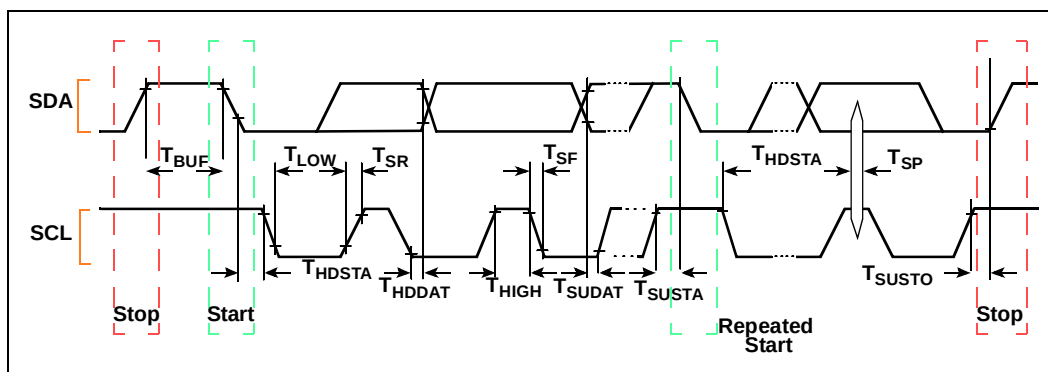
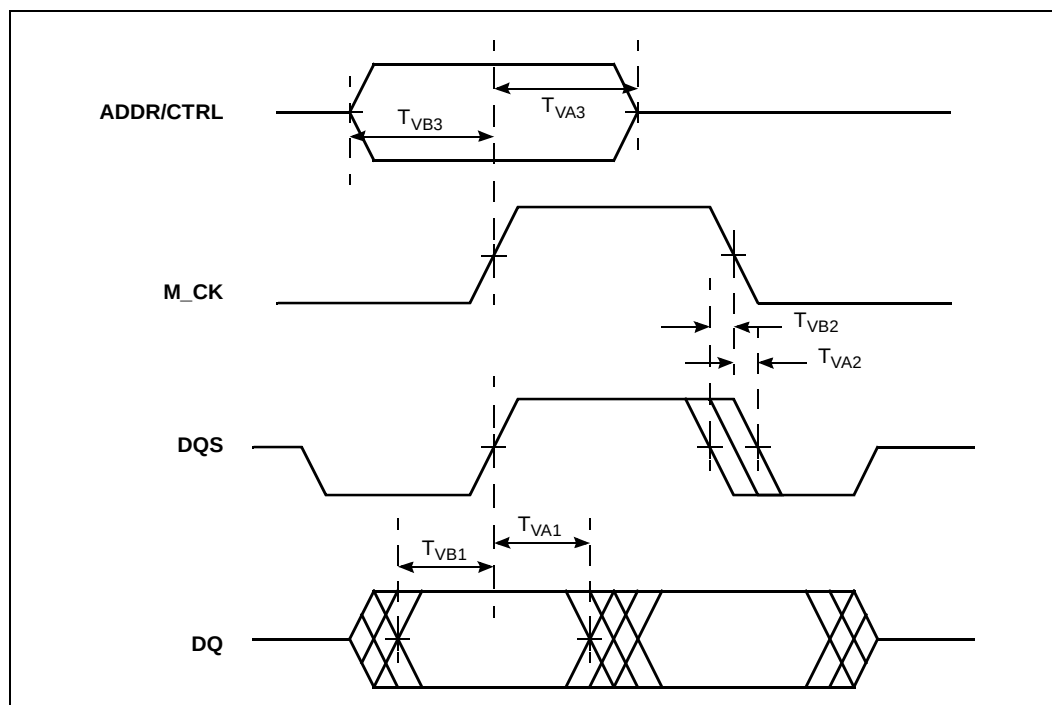
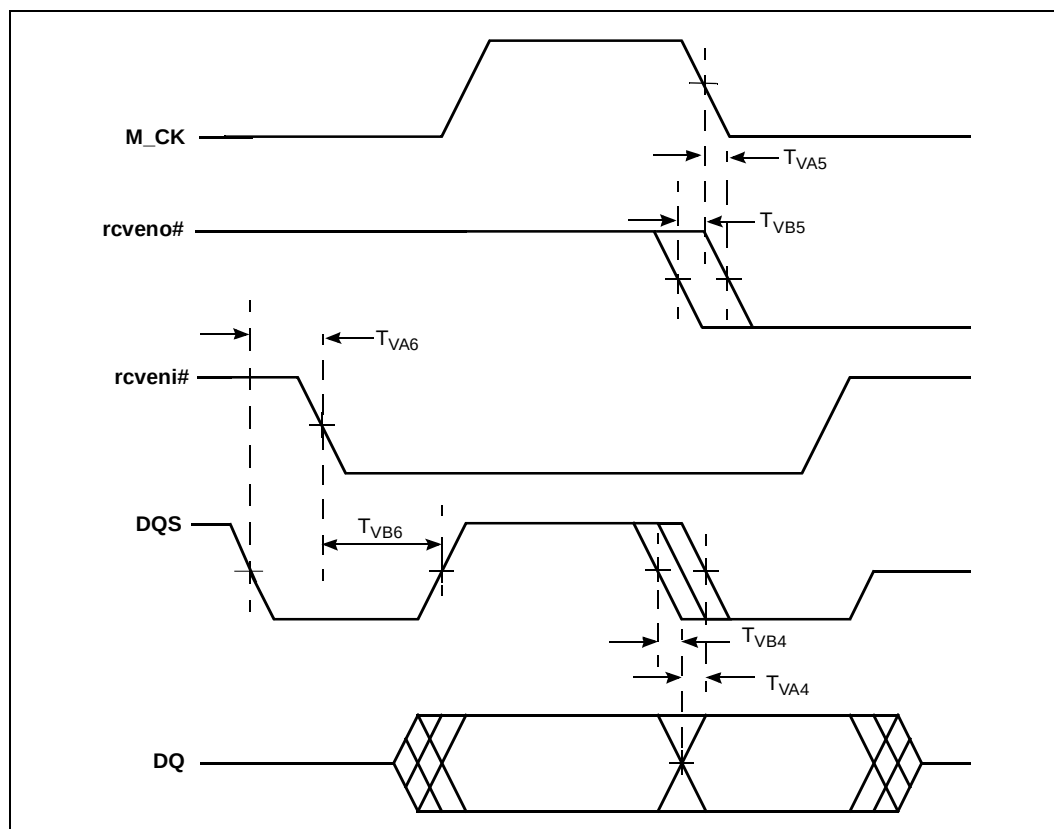


Figure 12. DDR SDRAM Write Timings



**Figure 13. DDR SDRAM Read Timings**



## 4.6 AC Test Conditions

Table 28. AC Measurement Conditions

| Symbol      | PCI-X            | PCI              | DDR  | PBI | Units | Notes |
|-------------|------------------|------------------|------|-----|-------|-------|
| $V_{tch}$   | $0.6 V_{CC33}$   | $0.6 V_{CC33}$   | -    | -   | V     |       |
| $V_{tcl}$   | $0.2 V_{CC33}$   | $0.2 V_{CC33}$   | -    | -   | V     |       |
| $V_{th}$    | $0.6 V_{CC33}$   | $0.6 V_{CC33}$   | 2.0  | 2.0 | V     |       |
| $V_{tl}$    | $0.25 V_{CC33}$  | $0.2 V_{CC33}$   | 0.5  | 0.8 | V     |       |
| $V_{test}$  | $0.4 V_{CC33}$   | $0.4 V_{CC33}$   | 1.25 | 1.5 | V     |       |
| $V_{trise}$ | $0.285 V_{CC33}$ | $0.285 V_{CC33}$ | 1.25 | 1.5 | V     |       |
| $V_{tfall}$ | $0.615 V_{CC33}$ | $0.615 V_{CC33}$ | 1.25 | 1.5 | V     |       |
| $V_{max}$   | $0.4 V_{CC33}$   | $0.4 V_{CC33}$   | 1.5  | 1.2 | V     |       |
| Slew Rate   | 1.5              | 1.5              | 1.5  | 1.5 | V/nS  | 1     |

1. Input signal slew rate is measured between  $V_{il}$  and  $V_{ih}$ .

Figure 14. AC Test Load for all Signals Except PCI and DDR SDRAM

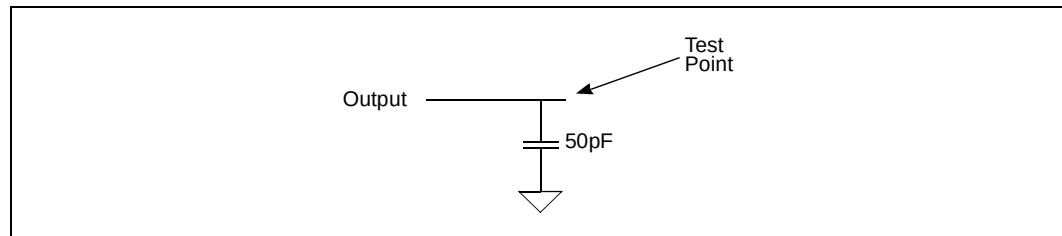


Figure 15. PCI/PCI-X  $T_{OV(max)}$  Rising Edge AC Test Load

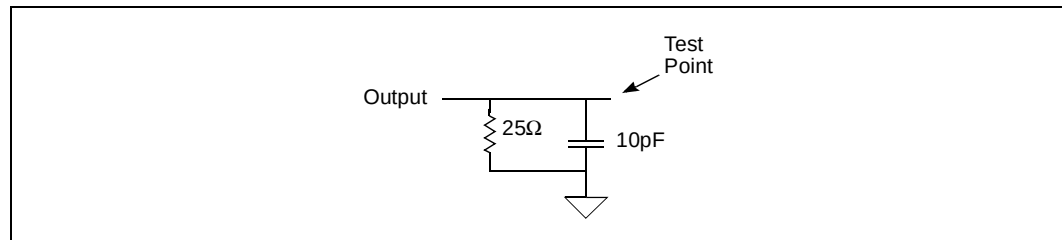


Figure 16. PCI/PCI-X  $T_{OV(max)}$  Falling Edge AC Test Load

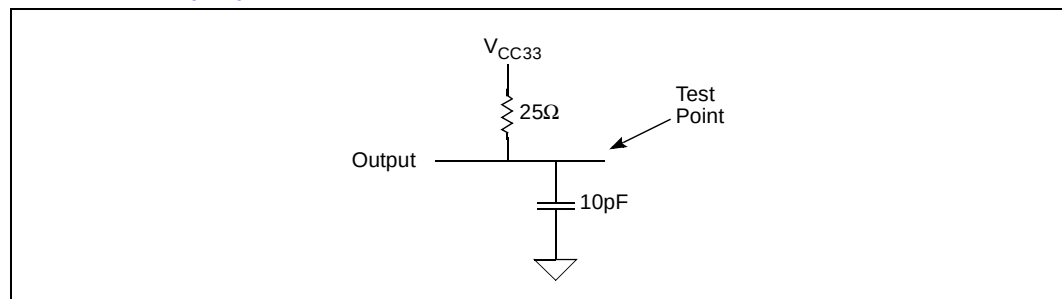




Figure 17. PCI/PCI-X  $T_{OV(min)}$  AC Test Load

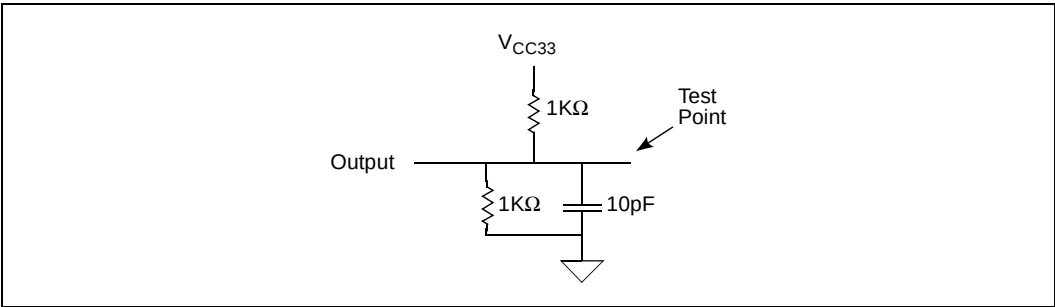


Figure 18. PCI\_RST# vs. PWRDELAY Timings During Power-Up

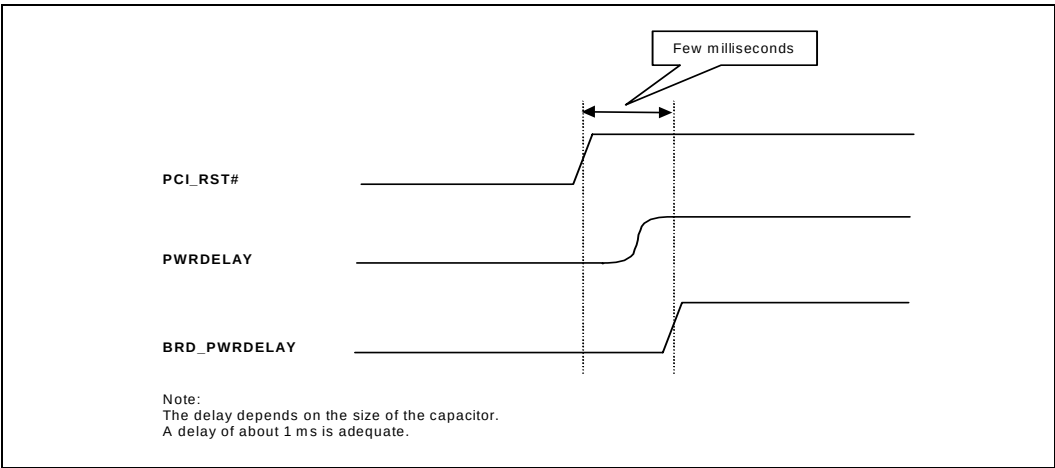


Figure 19. PCI\_RST# vs. PWRDELAY Timings During Power-Down

