General Description
The LM4681 is a fully integrated single supply, CLASS D audio power amplifier solution. The LM4681 utilizes a proprietary balanced pulse-width modulation technique that lowers output noise and THD and improves PSRR when compared to conventional pulse width modulators.

The LM4681 also features a stereo headphone amplifier that delivers 80mW into a 32Ω headset with less than 0.5% THD. The LM4681’s I2C/SPI (selectable) volume control has a +30dB to –48dB range when speakers are driven and a range of +13dB to –65dB when headphones are connected. All amplifiers are protected by thermal shutdown. Additionally, the high efficiency power amplifiers have output current limit.

With a 8Ω load, the IC’s efficiency for a 6W power level is 85%. The IC features click and pop reduction circuitry that minimizes audible popping during device turn-on and turn-off. The LM4681 is available in a 48-lead LLP package, ideal for portable and desktop computer applications.

Key Specifications
- $P_o$ at THD+N = 10%, $A_v = 30\, \text{dB}, V_{DD} = 14\, \text{V}$ 10W (typ)
- THD+N at 1kHz at 1W into 8Ω (Power Amp) 0.43% (typ)
- Efficiency at 7W into 8Ω 85% (min)
- Total quiescent power supply current 50mA (typ)
- THD+N 1kHz, 20mW, 32Ω (Headphone) 0.02% (typ)
- Single supply range 9.0V to 15.5V

Features
- Pulse-width modulator.
- I2C/SPI (selectable) volume control
- Stereo headphone amplifier.
- “Click and pop” suppression circuitry.
- Micropower shutdown mode.
- 48 lead LLP package (No heatsink required).

Applications
- Flat Panel Displays
- Televisions
- Multimedia Monitors

Block Diagram
Connection Diagram

OUT1_B_1
OUT1_B_2
OUT1_B_3
PV-DD_B_4
PGND_B_5
PGND_B_6
PGND_B_7
PV-DD_B_8
PV-DD_B_9
OUT2_B_10
OUT2_B_11
OUT2_B_12

OUT2_A_25
OUT2_A_26
OUT2_A_27
PV-DD_A_28
PV-DD_A_29
PGND_A_30
PGND_A_31
PGND_A_32
PV-DD_A_33
OUT1_A_34
OUT1_A_35
OUT1_A_36

Top View
Order Number LM4681SQ
See NS Package Number SQA048AA
(LLP Package)

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Figure 1. Typical Application
**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage: 16V
- Input Voltage: −0.3V to VDD +0.3V
- Power Dissipation (Note 3): Internally Limited
- ESD Susceptibility (Note 4): 2000V
- ESD Susceptibility (Note 5): 200V
- Junction Temperature (Note 6): 150˚C
- Storage Temperature: −65˚C ≤ TA ≤ 150˚C

**Operating Ratings** (Notes 1, 2)

- Temperature Range: TMIN ≤ TA ≤ TMAX −40˚C ≤ TA ≤ +85˚C
- Supply Voltage: 9V ≤ VDD ≤ 15.5V
- Thermal Resistance (LLP Package):
  - \( \theta_{JA} \): 28˚C/W
  - \( \theta_{JC} \): 20˚C/W

**Soldering Information**

**Electrical Characteristics** (Notes 1, 2, 7)

The following specifications apply for VDD = 12V, I^2CVDD = 5V, RL = 8Ω, LC filter values as shown in Figure 1, unless otherwise specified. Limits apply for TA = 25˚C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>LM4681</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Operating Supply Voltage Range</td>
<td></td>
<td>Typical</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9</td>
</tr>
<tr>
<td>IS</td>
<td>Quiescent Power Supply Current, Class D Mode</td>
<td>( V_{IN} = 0V_{RMS}, V_{HPSEL} = 0V )</td>
<td>50</td>
</tr>
<tr>
<td>IS</td>
<td>Quiescent Power Supply Current, Headphone Mode</td>
<td>( V_{IN} = 0V_{RMS}, V_{HPSEL} = V_{DD} )</td>
<td>22</td>
</tr>
<tr>
<td>ISD</td>
<td>Quiescent Power Supply Current, Shutdown Mode</td>
<td>( V_{SD} = 5V )</td>
<td>0.1</td>
</tr>
<tr>
<td>RIN</td>
<td>Input Resistance in Both Modes</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>I^2CVDD</td>
<td>I^2C / SPI Logic Supply Voltage</td>
<td></td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V (min)</td>
</tr>
<tr>
<td>VIL</td>
<td>Minimum High Level Input Voltage</td>
<td>( I^2C/SPI ) Interface pins</td>
<td>0.7 x I^2CVDD</td>
</tr>
<tr>
<td>VIL</td>
<td>Maximum Low Level Input Voltage</td>
<td>( I^2C/SPI ) Interface pins</td>
<td>0.3 x I^2CVDD</td>
</tr>
<tr>
<td>VHPH</td>
<td>HP Sense High Input Voltage</td>
<td></td>
<td>VDD − 1</td>
</tr>
<tr>
<td>VHPL</td>
<td>HP Sense Low Input Voltage</td>
<td></td>
<td>VDD/2</td>
</tr>
</tbody>
</table>

**Power Amplifiers**

- PO: Maximum Output Power, Per Channel
  - THD+N ≤ 1%, \( f_{IN} = 1kHz \) | 6.0 | 5.3 | W (min) |
  - THD+N ≤ 10%, \( V_{DD} = 14V, f_{IN} = 1kHz \) | 10 | W |
- PDI | Power Dissipation | \( P_{O} = 6W/Chan, f_{IN} = 1kHz \) | 1.17 | W |
- EFF1 | Efficiency | \( P_{O} = 6W/Chan, f_{IN} = 1kHz \) | 85 | % |
| THD+N | Harmonic Distortion + Noise | \( P_{O} = 1W/Chan, f_{IN} = 1kHz \) | 0.11 | % |
| VNOISE | Output Noise Voltage | \( R_{SOURCE} = 50Ω, C_{IN} = 1μF, BW = 8Hz to 22kHz, A-weighted, input referred \) | 10 | µV |
### Electrical Characteristics (Notes 1, 2, 7) (Continued)

The following specifications apply for $V_{DD} = 12V$, $I_{CVDD} = 5V$, $R_L = 8\, \Omega$, LC filter values as shown in Figure 1, unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LM4681</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_{RIPPLE} = 200mV_{P-P}$, $C_{BYPASS} = 10\mu F$, input referred</td>
<td>Typical</td>
<td>Limit</td>
</tr>
<tr>
<td></td>
<td>PSRR</td>
<td>$f = 50Hz$</td>
<td>82</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 60Hz$</td>
<td>84</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 100Hz$</td>
<td>92</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 120Hz$</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 1kHz$</td>
<td>95</td>
<td></td>
</tr>
</tbody>
</table>

#### Headphone Amplifiers

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LM4681</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_O$</td>
<td>Maximum Power Output Per Channel</td>
<td>$THD+N \leq 1%, R_L = 32\Omega$, $f_{IN} = 1kHz$</td>
<td>94</td>
<td>70 mW (min)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$THD+N$</td>
<td>Distortion + Noise</td>
<td>$P_O = 20mW$, $R_L = 32\Omega$, $f_{IN} = 1kHz$</td>
<td>0.02</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{NOISE}$</td>
<td>Output Noise Voltage, RMS</td>
<td>$R_{IN} = 50\Omega$, $C_{IN} = 1\mu F$, $BW = 20Hz$ to 20kHz, $R_L = 32\Omega$ A-weighted, Input referred</td>
<td>22</td>
<td>$\mu V$</td>
</tr>
<tr>
<td></td>
<td>PSRR</td>
<td>Power Supply Rejection Ratio (Referred to Input)</td>
<td>$200mV$, $1kHz$, $V_{IN} = 0$, $R_L = 32\Omega$</td>
<td>77</td>
</tr>
</tbody>
</table>

### Electrical Characteristics for Volume Control (Notes 1, 2)

The following specifications apply for $V_{DD} = 12V$. Limits apply for $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LM4681</th>
<th>Units (Limits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{RANGE}$</td>
<td>Gain Range</td>
<td>Digital Code = Full Scale, No Load Power Amplifier</td>
<td>30</td>
<td>29 dB (min)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Headphone Amplifier</td>
<td>13</td>
<td>12 dB (min)</td>
</tr>
<tr>
<td></td>
<td>Digital Code = +1LSB, No Load Power Amplifier</td>
<td>$-48$</td>
<td>$-46$ dB (min)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Headphone Amplifier</td>
<td>$-65$</td>
<td>$-63$ dB (min)</td>
<td></td>
</tr>
<tr>
<td>$A_M$</td>
<td>Mute Gain</td>
<td>Digital Code = 0, No Load Power Amplifier</td>
<td>$-76$</td>
<td>$-74$ dB (max)</td>
</tr>
<tr>
<td></td>
<td>Headphone Amplifier</td>
<td>$-76$</td>
<td>$-74$ dB (max)</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. “Operating Ratings” indicate conditions for which the device is functional, but do not guarantee specific performance limits. “Electrical Characteristics” state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 3:** For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JA} = 80^\circ C/W$ (junction to ambient).

**Note 4:** Human body model, 100pF discharged through a 1.5k$\Omega$ resistor.

**Note 5:** Machine Model 220pF − 240pF discharged through all pins.

**Note 6:** The operating junction temperature maximum is 150°C.

**Note 7:** Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

**Note 8:** Typicals are measured at 25°C and represent the parametric norm.
### I²C/SPI Interface Controls

<table>
<thead>
<tr>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>I²C Address</th>
<th>Mode Control Register</th>
<th>Volume Control Register (See Table 4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ADR</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

#### Headphone Control

<table>
<thead>
<tr>
<th>HP Sense Pin (HPSEL, pin 22)</th>
<th>Output Stage Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Class D Amps Active</td>
</tr>
<tr>
<td>1 (VDD)</td>
<td>Class D Amps inactive</td>
</tr>
</tbody>
</table>

#### Logic Controls

<table>
<thead>
<tr>
<th>Logic Level (SEL, pin 21)</th>
<th>I²C/SPI Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>I²C mode</td>
</tr>
<tr>
<td>1</td>
<td>SPI mode</td>
</tr>
</tbody>
</table>
Typical Performance Characteristics
(Volume control at maximum, unless otherwise stated.)

Class D Amplifier THD+N vs Frequency
$V_{DD} = 9V$, $R_L = 8\Omega$, $P_O = 1W$

Class D Amplifier THD+N vs Frequency
$V_{DD} = 12V$, $R_L = 8\Omega$, $P_O = 1W$

Class D Amplifier THD+N vs Frequency
$V_{DD} = 15.5V$, $R_L = 8\Omega$, $P_O = 1W$

Class AB Headphone Amplifier THD+N vs Frequency
$V_{DD} = 9V$, $R_L = 32\Omega$, $P_O = 20mW$

Class AB Headphone Amplifier THD+N vs Frequency
$V_{DD} = 12V$, $R_L = 32\Omega$, $P_O = 20mW$

Class AB Headphone Amplifier THD+N vs Frequency
$V_{DD} = 15.5V$, $R_L = 32\Omega$, $P_O = 20mW$
Typical Performance Characteristics (Continued)

Class D Amplifier Output Power vs Supply Voltage

Class AB Headphone Amplifier Output Power vs Supply Voltage

Class D Amplifier Magnitude vs Frequency

- $V_{DD} = 9V$, $R_L = 8\Omega$, $P_O = 1W$
- $V_{DD} = 12V$, $R_L = 8\Omega$, $P_O = 1W$
- $V_{DD} = 15.5V$, $R_L = 8\Omega$, $P_O = 1W$

Class AB Headphone Amplifier Magnitude vs Frequency

- $V_{DD} = 9V$, $R_L = 32\Omega$, $P_O = 20mW$
Typical Performance Characteristics (Continued)

Class AB Headphone Amplifier Magnitude vs Frequency

- $V_{DD} = 12V$, $R_L = 32\Omega$, $P_O = 20mW$

- $V_{DD} = 15.5V$, $R_L = 32\Omega$, $P_O = 20mW$

PSRR vs Frequency

- $V_{DD} = 9V$
- $V_{DD} = 12V$
- $V_{DD} = 15.5V$

Class D Amplifier Dissipation vs Load Dissipation

- $V_{DD} = 9V$, $R_L = 8\Omega$
- Both channels driven and measured

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Typical Performance Characteristics (Continued)

Class D Amplifier Dissipation vs Load Dissipation

- **V_{DD} = 12V, R_L = 8\Omega**
- Both channels driven and measured

Class D Amplifier Dissipation vs Load Dissipation

- **V_{DD} = 15.5V, R_L = 8\Omega**
- Both channels driven and measured

Class D Amplifier Efficiency vs Total Output Power

- **V_{DD} = 9V, R_L = 8\Omega**
- Both channels driven and measured

Class D Amplifier Efficiency vs Total Output Power

- **V_{DD} = 12V, R_L = 8\Omega**
- Both channels driven and measured

Class D Amplifier Efficiency vs Total Output Power

- **V_{DD} = 15.5V, R_L = 8\Omega**
- Both channels driven and measured

Output Power vs Load Resistance

- **V_{DD} = 9V**
- Upper curve = 10% THD+N, Lower curve = 1% THD+N
Typical Performance Characteristics (Continued)

Output Power vs Load Resistance
$V_{DD} = 12V$
Upper curve = 10% THD+N, Lower curve = 1% THD+N

Output Power vs Load Resistance
$V_{DD} = 15.5V$
Upper curve = 10% THD+N, Lower curve = 1% THD+N

Power Supply Current vs Power Supply Voltage
General Features

SYSTEM FUNCTIONAL INFORMATION

Modulation Technique
Unlike typical Class D amplifiers that use single-ended comparators to generate a pulse-width modulated switching waveform and RC timing circuits to set the switching frequency, the LM4681 uses a balanced differential floating modulator. Oscillation is a result of injecting complimentary currents onto the respective plates of a floating, on-die capacitor. The value of the floating capacitor and value of the components in the modulator’s feedback network set the nominal switching frequency at 450kHz. Modulation results from imbalances in the injected currents. The amount of current imbalance is directly proportional to the applied input signal’s magnitude and frequency.

Using a balanced, floating modulator produces a Class D amplifier that is immune to common mode noise sources such as substrate noise. This noise occurs because of the high frequency, high current switching in the amplifier’s output stage. The LM4681 is immune to this type of noise because the modulator, the components that set its switching frequency, and even the load all float with respect to ground.

The balanced modulator’s pulse width modulated output drives the gates of the LM4681’s H-bridge configured output power MOSFETs. The pulse-train present at the power MOSFETs’ output is applied to an LC low pass filter that removes the 450kHz energy component. The filter’s output signal, which is applied to the driven load, is an amplified replica of the audio input signal.

Shutdown Function
The LM4681’s digitally controlled shutdown function allows the user to place the amplifier in a shutdown mode while the system power supply remains active. Activating shutdown deactivates the output switching waveform and minimizes the quiescent current. Through the SPI/I2C digital interface, the Mode control register’s Bit 0 is used to control the LM4681’s shutdown function. A logic “0” activates shutdown, whereas a logic “1” returns the amplifier to its operational quiescent state. When the power supply voltage is first applied, the LM4681 is immune to this type of noise because the modulator, the components that set its switching frequency, and even the load all float with respect to ground.

The balanced modulator’s pulse width modulated output drives the gates of the LM4681’s H-bridge configured output power MOSFETs. The pulse-train present at the power MOSFETs’ output is applied to an LC low pass filter that removes the 450kHz energy component. The filter’s output signal, which is applied to the driven load, is an amplified replica of the audio input signal.

Mute Function
The LM4681’s digitally-controlled mute function allows the user to place the amplifier outputs in a muted mode while the amplifier’s analog input signals remain active. Activating mute internally removes the analog input signal from the Class D and headphone amplifier inputs. While muted, the amplifier inputs and outputs retain their VDD/2 operational bias. Through the SPI/I2C digital interface, the Mode control register’s Bit 1 is used to control the LM4681’s audio mute function. A logic “0” activates mute, whereas a logic “1” deactivates mute. When the power supply voltage is first applied, the LM4681’s headphone and Class D amplifier outputs are muted. More information on the digital interface is found in the section titled “SPI/I2C Serial Digital Interface.”

Stereo Headphone Amplifier
The LM4681’s stereo headphone amplifier operates continuously, even while the Class D amplifiers are active. When using headphones to listen to program material, it is usually desirable to stop driving external speakers. This is easily achieved by using the active low HPSEL input. As shown in typical application schematic in Figure 1, with no headphones connected to the headphone jack the input voltage applied to the HPSEL pin is a logic low. In this state, the Class D amplifiers are active and able to drive external speakers. When headphones are plugged into the headphone jack, the switch internal to the jack is opened. This changes the voltage applied to the HPSEL pin to a logic high, shutting off the LM4681’s Class D amplifiers.

Under Voltage Protection
The under voltage protection disables the output driver section of the LM4681 while the supply voltage is below 8V. This condition may occur as power is first applied or during low line conditions, changes in load resistance, or when power supply sag occurs. The under voltage protection ensures that all of the LM4681’s power MOSFETs are off. This action eliminates shoot-through current and minimizes output transients during turn-on and turn-off. The under voltage protection gives the digital logic time to stabilize into known states, further minimizing turn output transients.

Power Supply Sequencing
To ensure best performance, please observe the following power-up sequence. The I2CVDD supply voltage should be applied first. Do not send any data to the LM4681’s internal registers until the VDD is applied. This takes advantage of the LM4681’s power-on reset, which activates the amplifier’s shutdown and mute. Once I2CVDD is applied, apply the VDD supply voltage. Prior to removing the two supply voltages, activate shutdown and mute.

Turn-On Time
The LM4681 has an internal timer that determines the amplifier’s turn-on time. After power is first applied or the part returns from shutdown, the nominal turn-on time is 600ms. This delay allows all externally applied capacitors to charge to a final value of VDD/2. Further, during turn-on, the outputs are muted. This minimizes output transients that may occur while the part settles into is quiescent operating mode.

Output Stage Current Limit and Fault Detection Protection
The output stage MOSFETs are protected against output conditions that could otherwise compromise their operational status. The first stage of protection is output current limiting. When conditions that require high currents to drive a load, the LM4681’s current limit circuitry clamps the output current at a nominal value of 2.5A. The output waveform is present, but may be clipped or its amplitude reduced. The same 2.5A nominal current limit also occurs if the amplifier outputs are shorted together or either output is shorted to VDD or GND.

The second stage of protection is an onboard fault detection circuit that continuously monitors the signal on each output MOSFET’s gate and compares it against the respective drain voltage. When a condition is detected that violates a MOSFET’s Safe Operating Area (SOA), the drive signal is disconnected from the output MOSFETs’ gates. The fault detect circuit maintains this protective condition for approximately 600ms, at which time the drive signal is reconnected. If the fault condition is no longer present, normal operation resumes. If the fault condition remains, however, the drive signal is again disconnected.
General Features (Continued)

Thermal Protection
The LM4681 has thermal shutdown circuitry that monitors the die temperature. Once the LM4681 die temperature reaches 170˚C, the LM4681 disables the output switching waveform and remains disabled until the die temperature falls below 140˚C (typ).

Over-Modulation Protection
The LM4681’s over-modulation protection is a result of the preamplifier’s (AMP1 and AMP2, Figure 1) inability to produce signal magnitudes that equal the power supply voltages. Since the preamplifier’s output magnitude will always be less than the supply voltage, the duty cycle of the amplifier’s switching output will never reach zero. Peak modulation is limited to a nominal 95%.

I²C Compatible Interface
The LM4681 uses a serial bus, which conforms to the I²C protocol, to control the chip’s functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4681.

The I²C address for the LM4681 is determined using the ADR pin. The LM4681’s two possible I²C chip addresses are of the form 110110X10 (binary), where X1 = 0, if ADR is logic low, and X1 = 1, if ADR is a logic high. If the I²C interface is used to address a number of chips in a system, the LM4681’s chip address can be changed to avoid possible address conflicts.

The bus format for the I²C interface is shown in Figure 5. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master releases the data line high (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4681 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not held low during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4681.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable.

After the data byte is sent, the master must check for another acknowledge to see if the LM4681 received the data.

If the master has more data bytes to send to the LM4681, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

SPI Interface
The LM4681’s serial control interface is compatible with SPI signals and protocols. When using SPI signals, the ADR pin is the input for the SPI ENABLE signal, the SDA pin is the input for the SPI CLOCK signal, and the SDA pin is the SPI DATA input.

I²C/SPI Interface Power Supply Pin (I²C VDD)
The LM4681’s I²C/SPI interface is powered up through the I²C/SPI VDD pin. The LM4681’s I²C/SPI interface operates at a voltage level set by the I²C/SPI VDD pin which can be set independent to that of the main power supply pin VDD. This is ideal whenever logic levels for the I²C/SPI interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.
SPI Operational Requirements

1. The maximum clock rate is 5MHz for the CLK pin.
2. CLK must remain logic-high for at least 100ns ($t_{CH}$) after the rising edge of CLK, and CLK must remain logic-low for at least 100ns ($t_{CL}$) after the falling edge of CLK.
3. Data bits are written to the DATA pin with the most significant bit (MSB) first.
4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 50ns ($t_{DS}$) before the rising edge of CLK. Also, any transition on DATA must occur at least 50ns ($t_{DH}$) after the rising edge of CLK and stabilize before the next rising edge of CLK.
5. ENABLE should be logic-low only during serial data transmission.
6. ENABLE must be logic-low at least 50ns ($t_{ES}$) before the first rising edge of CLK, and ENABLE has to remain logic-low at least 50ns ($t_{EH}$) after the eighth rising edge of CLK.
7. If ENABLE remains logic-high for more than 50ns before all 8 bits are transmitted then the data latch will be aborted.
8. If ENABLE is logic-low for more than 8 CLK pulses then only the first 8 data bits will be latched and activated at rising edge of eighth CLK.

9. ENABLE must remain logic-high for at least 50ns (t_{EL}).

10. Coincidental rising or falling edges of CLK and ENABLE are not allowed. If CLK is to be held logic-high after the data transmission, the falling edge of CLK must occur at least 50ns (t_{CS}) before ENABLE transitions to logic-low for the next set of data.

**Volume Control**

The internal Stereo Volume Control is set by changing bits 0 through 4 in the SPI interface, as shown in table 3 below.

<table>
<thead>
<tr>
<th>Gain (dB)</th>
<th>HP Outputs</th>
<th>Class D Outputs</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
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Application Hints

SUPPLY BYPASSING

Correct power supply bypassing has two important goals. The first is to reduce noise on the power supply lines and minimize deleterious effects that the noise may cause to the amplifier’s operation. The second is to help stabilize an unregulated power supply and to improve the supply’s transient response under heavy current demands. These two goals require different capacitor value ranges. Therefore, various types and values are recommended for supply bypassing. For noise de-coupling, generally small ceramic capacitors (0.01µF to 0.1µF) are recommended. Larger value (1µF to 10µF) tantalum capacitors are needed for the transient current demands. These two capacitors in parallel will do an adequate job of removing most noise from the supply rails and providing the necessary transient current. These capacitors should be placed as close as possible to each IC’s supply pin(s) using leads as short as possible.

The LM4681 has two different set of \( V_{DD} \) pins: a set for power \( V_{DD} \) (PVDD) and a set for signal \( V_{DD} \) (SVDD). The parallel combination of the low value ceramic (0.1µF) and high value tantalum (10µF) should be used to bypass the PVDD pin. A small value (0.1µF) ceramic or tantalum can be used to bypass the SVDD pin.

OUTPUT STAGE FILTERING

The LM4681 requires a low pass filter connected between the amplifier’s bridge output and the load. Figure 1 shows the recommended LC filter. A minimum value of 27µH is recommended. As shown in Figure 1, using the values of the components connected between the amplifier BTL outputs and the load achieves a 2nd-order lowpass filter response with a -3dB cutoff frequency of 25kHz.

THD+N MEASUREMENTS AND OUT OF AUDIO BAND NOISE

THD+N (Total Harmonic Distortion plus Noise) is a very important parameter by which all audio amplifiers are measured. Often it is shown as a graph where either the output power or frequency is changed over the operating range. A very important variable in the measurement of THD+N is the bandwidth-limiting filter at the input of the test equipment. Class D amplifiers, by design, switch their output power devices at a much higher frequency than the accepted audio range (20Hz - 20kHz). Alternately switching the output voltage between \( V_{DD} \) and GND allows the LM4681 to operate at much higher efficiency than that achieved by traditional Class AB amplifiers. Switching the outputs at high frequency also increases the out-of-band noise. Under normal circumstances the output lowpass filter significantly reduces this out-of-band noise. If the low pass filter is not optimized for a given switching frequency, there can be significant increase in out-of-band noise. THD+N measurements can be significantly affected by out-of-band noise, resulting in a higher than expected THD+N measurement. To achieve a more accurate measurement of THD, the test equipment’s input bandwidth of the must be limited. Some common upper filter points are 22kHz, 30kHz, and 80kHz. The input filter limits the noise component of the THD+N measurement to a smaller bandwidth resulting in a more real-world THD+N value.
<table>
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<tr>
<th>Rev</th>
<th>Date</th>
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<td>Initial release.</td>
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Physical Dimensions  inches (millimeters) unless otherwise noted

Order Number LM4681SQ
NS Package Number SQA048AA

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