**Description**

Silicon Laboratories’ family of SONET/SDH clock multipliers/jitter attenuators provides the industry’s best performance while requiring the least amount of board space. Offering jitter generation of less than 0.3ps_RMS (OC-192), these devices outperform discrete implementations and hybrid clock solutions while integrating features like selectable forward error correction (FEC), frequency scaling, pin selectable loop filter bandwidths, and Stratum compliant hitless switching. Based on Silicon Laboratories’ DSPLL™ technology, these clock ICs provide a fully integrated PLL eliminating the need for sensitive external loop filter components and costly VCXO s. A complete family of clocking solutions is available including single input/output devices as well as multiple input/output devices with hitless switching.

**System Benefits**

- Small size saves board space
- Frequency agility reduces bill-of-materials
- DSPLL technology reduces external component count
- Enhanced functionality simplifies design and saves cost

**Applications**

- Optical port cards/line cards
- Optical routers switches
- Add/drop multiplexers
- Metro and edge equipment

**Key Products**

**Si5364 Port Card Clock IC**
- Stratum compliant hitless switching among three 19.44 MHz clock inputs
- Jitter generation less than 0.3 ps_RMS (OC-192)
- Jitter attenuation with programmable PLL bandwidths
- Four programmable clock outputs at 19, 155 or 622 MHz
- Automatic or manual clock switching
- FEC scaling (255/238)
- Small size: 11 x 11 mm BGA package

**Si5321 Clock Multiplier**
- Jitter generation less than 0.3 ps_RMS (OC-192)
- Clock input/output centered at 19, 38, 77, 155, 311, 622, 1244 or 2488 MHz
- Forward and reverse FEC clock scaling (255/238, 255/237, 66/64)
- Selectable loop filter bandwidths of 800 to 12800 Hz
- Low power: 445 mW (3.3 V operation)
- Small size: 9 x 9 mm BGA package

**Si5320 Clock Multiplier**
- Jitter generation less than 0.3 ps_RMS (OC-192)
- Clock input/output centered at 19, 155, 622 MHz
- Forward and reverse FEC clock scaling (255/238)
- Selectable loop filter bandwidths of 800 to 12800 Hz
- Low power: 445 mW (3.3 V operation)
- Small size: 9 x 9 mm BGA package
**Jitter Attenuation**

Silicon Laboratories' family of precision clock multipliers/jitter attenuators provides selectable loop filter bandwidths to minimize system clock jitter. Available loop bandwidth settings are 800, 1600, 3200, 6400 and 12800 Hz.

**FEC Scaling**

These clock ICs provide the appropriate clock scaling to translate between standard SONET/SDH reference clock frequencies and forward error correction (FEC) frequencies. The maximum clock output includes 693 MHz and 2.77 GHz (Si5321) for 10 GbE FEC support.

**Hitless Switching**

The Si5364 provides reference monitoring and clock switching that support Stratum 2/3/3E and SMC requirements. Clock switching can be automatic or manually controlled.

**Small Size**

These devices provide 5x to 20x space savings compared to traditional solutions using discretely implemented PLLs or clock modules.

**Proprietary DSPLL Technology**

The PLL within these devices utilizes digital signal processing to provide superior jitter performance while keeping all VCO and loop filter circuitry internal to the device. This level of integration makes the PLL less susceptible to board level noise, improving jitter performance.