TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVX374F,TC74LVX374FW,TC74LVX374FT

Octal D-Type Flip-Flop with 3-State Output

The TC74LVX374F/FW/FT is a high-speed CMOS octal D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

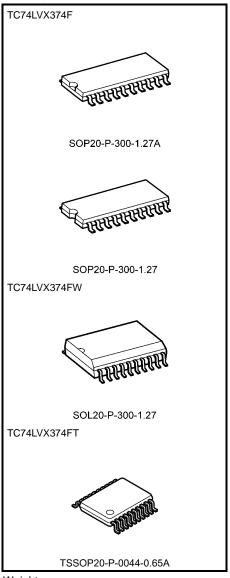
This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input (\overline{OE}). When the \overline{OE} input is high, the eight outputs are in a high-impedance state.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High-speed: $f_{max} = 160 \text{ MHz}$ (typ.) (VCC = 3.3 V)
- Low power dissipation: $I_{CC} = 4 \mu A \text{ (max) (Ta} = 25 ^{\circ}\text{C)}$
- Input voltage level: VIL = 0.8 V (max) (VCC = 3 V) VIH = 2.0 V (min) (VCC = 3 V)
- Power-down protection is provided on all inputs
- Balanced propagation delays: t_pLH ≃ t_pHL
- Low noise: VOLP = 0.8 V (max)
- Pin and function compatible with 74HC374

Note: xxxFW (JEDEC SOP) is not available in Japan.



Weight

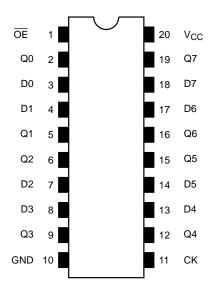
 SOP20-P-300-1.27A
 : 0.22 g (typ.)

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 : 0.22 g (typ.)

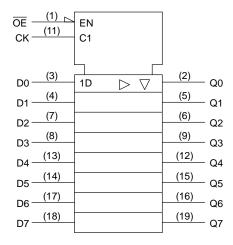
 SOL20-P-300-1.27
 : 0.46 g (typ.)

 TSSOP20-P-0044-0.65A
 : 0.08 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

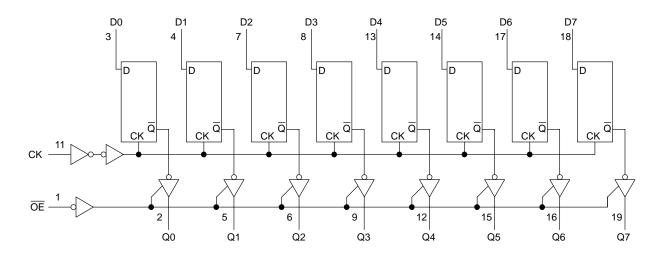
	Outpute		
ŌĒ	CK	Outputs	
Н	Х	X	Z
L	—	Х	Qn
L		L	L
L		Н	Н

X: Don't care

Z: High impedance

Qn: No change

System Diagram





Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	lout	±25	mA
DC V _{CC} /ground current	Icc	±75	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 3.6	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.



Electrical Characteristics

DC Characteristics

Characteristics		Symbol	ol Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit									
					V _{CC} (V)	Min	Тур.	Max	Min	Max										
					2.0	1.5	_	_	1.5	_										
	H-level	V _{IH}		_	3.0	2.0	_	_	2.0	_										
Input voltage					3.6	2.4	_	_	2.4	_	V									
Input voltage	voltage			2.0	_	_	0.5	_	0.5	v										
	L-level	el V _{IL}	_		_	_	0.8	_	0.8	,										
						_	_	0.8	_	0.8										
		H-level V _{OH}	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -50 \mu A$	2.0	1.9	2.0	_	1.9	_	V									
	H-level			$I_{OH} = -50 \mu A$	3.0	2.9	3.0	_	2.9	_										
Output voltage				$I_{OH} = -4 \text{ mA}$	3.0	2.58	_	_	2.48	_										
Output voltage				$I_{OL} = 50 \mu A$	2.0	_	0	0.1	_	0.1	v									
	L-level	V _{OL}	$V_{IN} = V_{IH}$	V _{IN} = V _{IH}	V _{IN} = V _{IH}	$V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{II}	$V_{IN} = V_{IH}$ or V_{II}	$V_{IN} = V_{IH}$ or V_{II}	V _{IN} = V _{IH}	$V_{IN} = V_{IH}$ or V_{II}	$V_{IN} = V_{IH}$	$I_{OL} = 50 \mu A$	3.0		0	0.1		0.1	
				$I_{OL} = 4 \text{ mA}$	3.0		ı	0.36		0.44										
3-state output Off-state current		loz	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		3.6	_	_	±0.25	_	±2.5	μА									
Input leakage cur	rent	I _{IN}	V _{IN} = 5.5 V or GND		3.6	_	_	±0.1	_	±1.0	μΑ									
Quiescent supply	current	Icc	V _{IN} = V _{CC} or GND		3.6			4.0		40.0	μА									

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	nbol Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit	
	, , , ,		V _{CC} (V)	Limit	Limit		
Minimum pulse width	t _{W (H)}		2.7	7.5	8.0	ns	
(CK)	t _{W (L)}	_	3.3 ± 0.3	5.0	5.5	113	
Minimum set-up time	t _S		2.7	6.5	6.5	ns	
		_	3.3 ± 0.3	4.5	4.5	115	
Minimum hold time	th		2.7	2.0	2.0	ns	
			3.3 ± 0.3	2.0	2.0	115	

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AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	st Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
	Í		V _{CC} (V)	C _L (pF)	Min	Тур.	Max	Min	Max	
	t		2.7	15	1	8.5	16.3	1.0	19.5	ns
Propagation delay time	t _{pLH}			50		11.0	19.8	1.0	23.0	
(CK-Q)	tarn	_	3.3 ± 0.3	15		6.7	10.6	1.0	12.5	113
	tpHL		3.3 ± 0.5	50		9.2	14.1	1.0	16.0	
	t=1		2.7	15		7.6	14.5	1.0	17.5	
Outside as able time	t _{pZL}	$R_L = 1 \text{ k}\Omega$	2.1	50		10.1	18.0	1.0	21.0	ns ns
Output enable time	t _{pZH}		3.3 ± 0.3	15		5.9	9.3	1.0	11.0	
				50		8.4	12.8	1.0	14.5	
Output disable time	t _{pLZ}	$R_L = 1 \text{ k}\Omega$	2.7	50	_	11.5	18.5	1.0	22.0	
Output disable time	t _{pHZ}		3.3 ± 0.3	50		9.6	13.2	1.0	15.0	
			2.7	15	60	115	_	50	_	- MHz
Maximum clock frequency				50	45	60	_	40	_	
Maximum clock frequency	f _{max}	_	3.3 ± 0.3	15	100	160	_	85	_	
				50	60	95	_	55	_	
Output to output skew	t _{osLH}	(Note 1)	2.7	50			1.5	_	1.5	ns
Output to output skew	t _{osHL}	(Note 1)	3.3 ± 0.3	50			1.5	_	1.5	113
Input capacitance	C _{IN}			(Note 2)		4	10	_	10	pF
Output capacitance	C _{OUT}		_			6			_	pF
Power dissipation capacitance	C _{PD}			(Note 3)	_	32	_	_	_	pF

Note 1: Parameter guaranteed by design.

 $(t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)$

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 (per F/F)$

And the total CPD when n pcs. of Flip Flop operate can be gained by the following equation:

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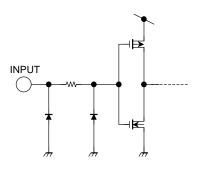
 C_{PD} (total) = 20 + 12 · n



Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Limit	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	_	3.3	0.5	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	_	3.3	-0.5	-0.8	V
Minimum high level dynamic input voltage V _{IH}	V_{IHD}	_	3.3	_	2.0	٧
Maximum low level dynamic input voltage V _{IL}	V _{ILD}	ı	3.3	_	0.8	٧

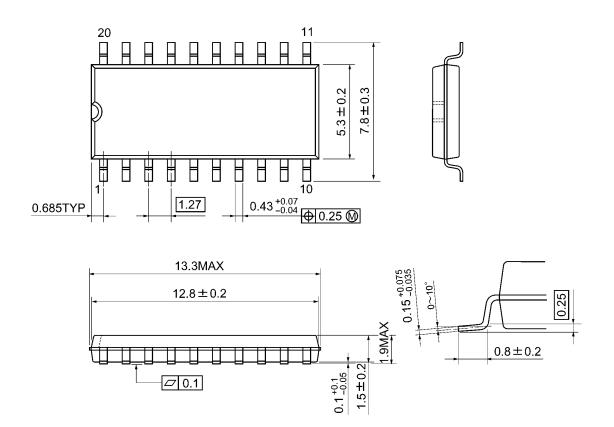
Input Equivalent Circuit



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Package Dimensions

SOP20-P-300-1.27A Unit: mm



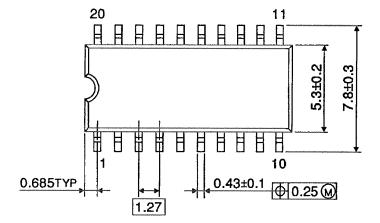
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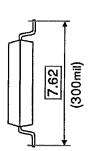
Weight: 0.22 g (typ.)

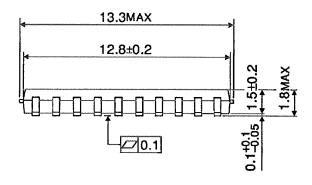
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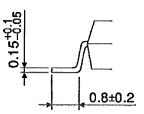
Package Dimensions

SOP20-P-300-1.27







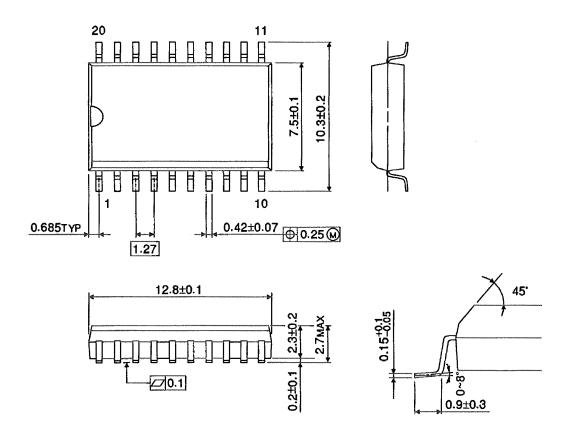


Weight: 0.22 g (typ.)

Package Dimensions (Note)

SOL20-P-300-1.27

Unit: mm



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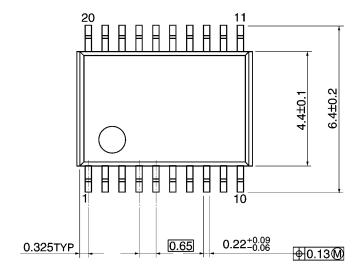
Note: This package is not available in Japan.

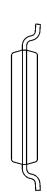
Weight: 0.46 g (typ.)

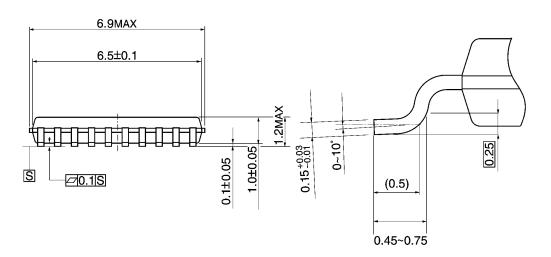
Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm







Weight: 0.08 g (typ.)

Note: Lead (Pb)-Free Packages

SOP20-P-300-1.27A TSSOP20-P-0044-0.65A

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