

CMOS 32-bit Micro-controller

**TMP92FD54AI****1. Outline and Device Characteristics**

TMP92FD54AI is high-speed advanced 32-bit micro-controller developed for controlling equipment which processes mass data.

TMP92FD54AI is a micro-controller which has a high-performance CPU (900/H1 CPU) and various built-in I/Os. TMP92FD54AI is housed in a 100-pin mini flat package.

Device characteristics are as follows:

## (1) CPU : 32-bit CPU(900/H1 CPU)

Compatible with TLCS-900,900/L,900/L1,900/H,900/H2's instruction code

16Mbytes of linear address space

General-purpose register and register banks

Micro DMA : 8channels (250ns / 4bytes at fc = 20MHz, best case)

Minimum instruction execution time : 50ns(at 20MHz)

Internal data bus : 32-bit

## (2) Internal memory

Internal RAM : 32K-byte

Internal ROM : 512K-byte Flash E2PROM

3K-byte Mask ROM (for Flash boot mode)

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- (3) External memory expansion
  - 16M-byte linear address space (memory mapped I/O)
  - External data bus : 8bit(for external I/O expansion)
  - \* Can't use upper address bus when built-in I/Os are selected
- (4) Memory controller (MEMC)
  - Chip select output : 1 channel
- (5) 8-bit timer : 8 channels
  - 8-bit interval timer mode (8 channels)
  - 16-bit interval timer mode (4 channels)
  - 8-bit programmable pulse generation (PPG) output mode (4 channels)
  - 8-bit pulse width modulation (PWM) output mode (4 channels)
- (6) 16-bit timer : 2 channels
  - 16-bit interval timer mode
  - 16-bit event counter mode
  - 16-bit programmable pulse generation (PPG) output mode
  - Frequency measurement mode
  - Pulse width measurement mode
  - Time differential measurement mode
- (7) Serial interface (SIO) : 2 channels
  - I/O interface mode
  - Universal asynchronous receiver transmitter (UART) mode
- (8) Serial expansion interface (SEI) : 1 channel
  - Baud rate 4/2/0.5Mbps at fc=20MHz.
- (9) Serial bus interface (SBI) : 3 channels
  - Clocked-synchronous 8-bit serial interface mode
  - I<sup>2</sup>C bus mode
- (10) CAN controller : 1channel
  - Supports CAN version 2.0B.
  - 16 mailboxes
- (11) 10-bit A/D converter (ADC) : 12 channels
  - A/D conversion time 8μsec @fc=20MHz.
  - Total tolerance +/- 3LSB (excluding quantization error)
  - Scan mode for all 12channels
- (12) Watch dog timer (WDT)
- (13) Timer for real-time clock (RTC)
  - Can operate with only low frequency oscillator.
- (14) Interrupt controller (INTC) : 60 interrupt sources
  - 9 interrupts from CPU
  - 42 internal interrupt vectors
  - 9 external interrupt vectors
- (15) I/O Port : 68pins
- (16) Standby mode
  - Four modes : IDLE3, IDLE2, IDLE1 and STOP
  - STOP mode can be released by 9 external inputs.
- (17) Internal voltage detection flag (RAMSTB)

(18) Power supply voltage

VCC5 = 4.5V to 5.25V

VCC3 = 3.3V (VCC3 Connect to REGOUT; built-in voltage regulator.)

(19) Operating temperature : -40 to 85 degree C

(20) Package : P-LQFP100-1414-0.50C

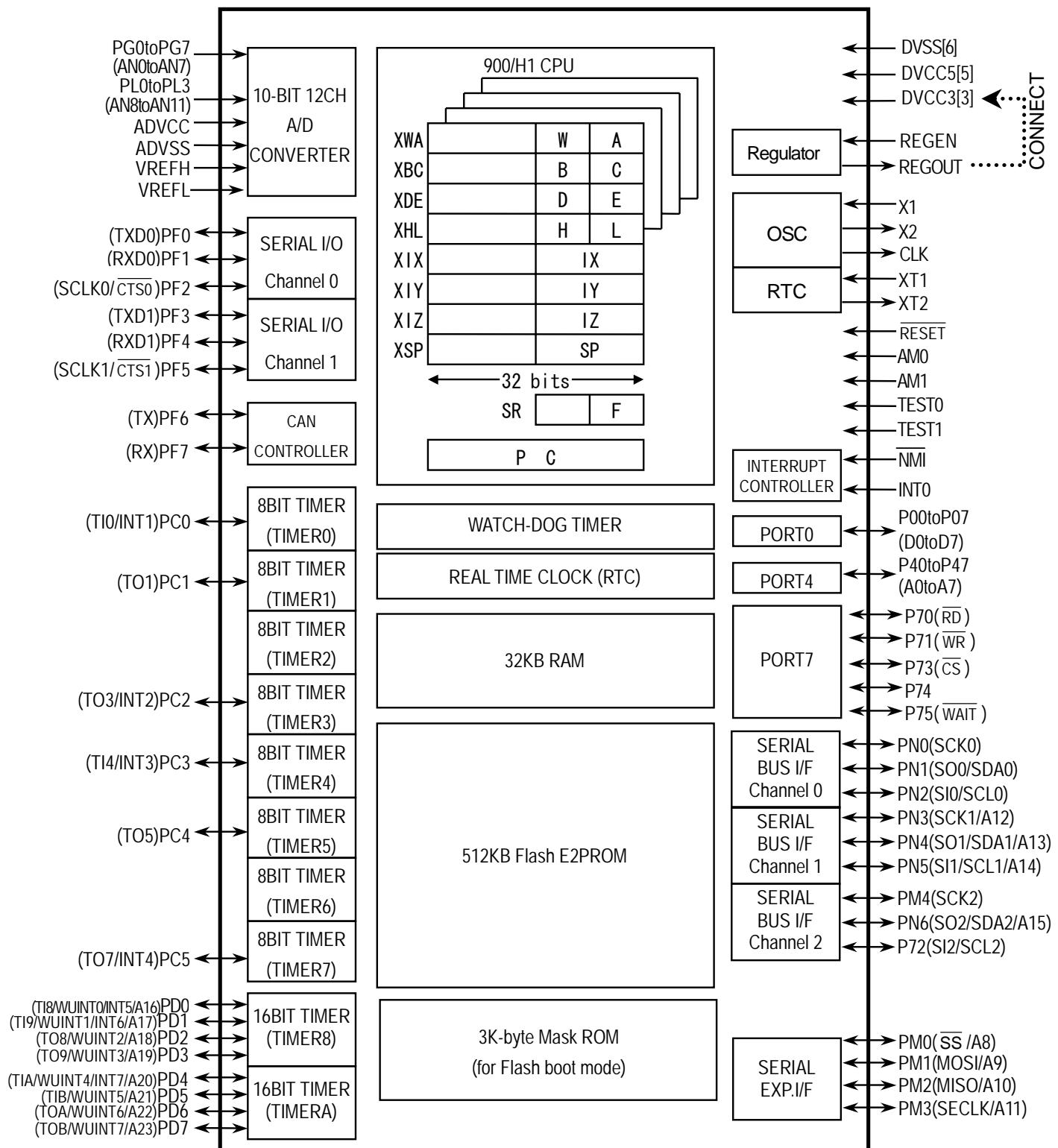
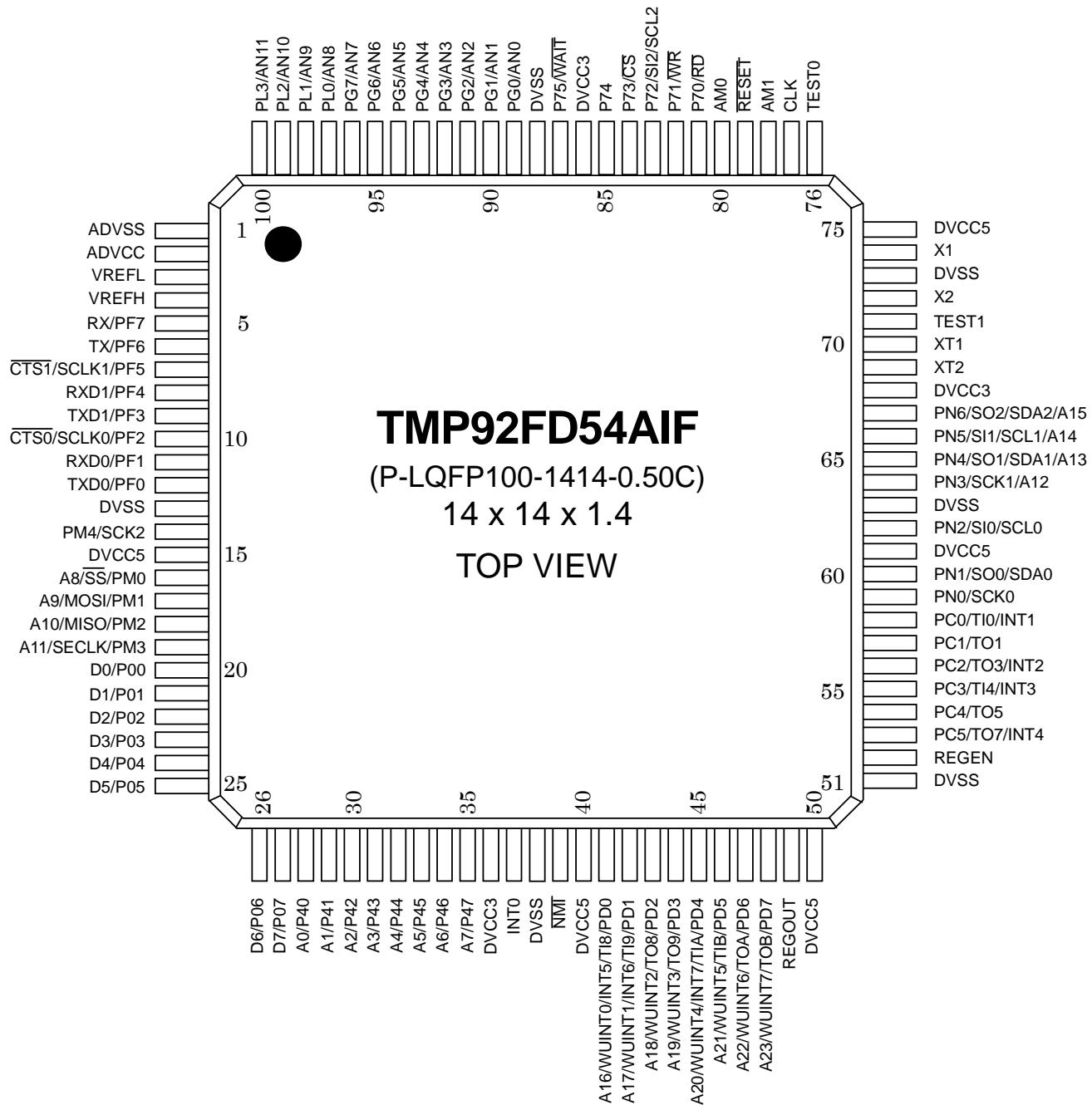


Figure 1 TMP92FD54AI block diagram

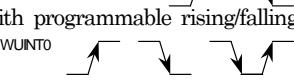
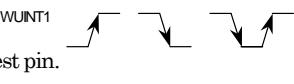
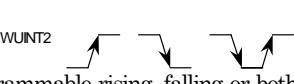
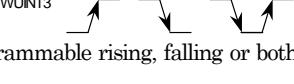
## 2. Pin Assignment and Functions

### 2.1 Pin Assignment



## 2.2 Pin names and functions

The following table shows the names and functions of the input/output pins.

Pin name	Pin number	Number of pins	In/Out	Function
P00..P07 D0..D7	20 <sup>th</sup> ...27 <sup>th</sup>	8 <small>(CMOS) (TTL)</small>	in/out in/out	Port 0: I/O port. Input or output specifiable in units of bits. Data: Data bus 0 to 7.
P40..P47 A0..A7	28 <sup>th</sup> ...35 <sup>th</sup>	8	in/out out	Port4: I/O port. Input or output specifiable in units of bits. Address: Address bus 0 to 7.
P70 RD	81 <sup>st</sup>	1	in/out out	Port70: I/O port. Read: Outputs strobe signal to read external memory.
P71 WR	82 <sup>nd</sup>	1	in/out out	Port 71: I/O port. Write: Output strobe signal to write external memory.
P72 SI2 SCL2	83 <sup>rd</sup>	1	in/out	Port 72: I/O port. SBI channel 2: Input data at SIO mode SBI channel 2: Clock input/output at I <sup>C</sup> mode
P73 CS	84 <sup>th</sup>	1	in/out out	Port 73: I/O port. Chip select: Outputs "low" if address is within specified address area.
P74	85 <sup>th</sup>	1	in/out	Port 74: I/O port.
P75 WAIT	87 <sup>th</sup>	1	in/out in	Port 75: I/O port. Wait: Signal used to request CPU bus wait.
PC0 TI0 INT1	58 <sup>th</sup>	1	in/out in in	Port C0: I/O port. Timer input 0: Input pin for timer 0. Interrupt request pin 1: Rising-edge interrupt request pin. 
PC1 TO1	57 <sup>th</sup>	1	in/out out	Port C1: I/O port. Timer output 1: Output pin for timer 1.
PC2 TO3 INT2	56 <sup>th</sup>	1	in/out out in	Port C2: I/O port. Timer output 3: Output pin for timer 3. Interrupt request pin 2: Rising-edge interrupt request pin. 
PC3 TI4 INT3	55 <sup>th</sup>	1	in/out in in	Port C3: I/O port. Timer input 4: Input pin for timer 4. Interrupt request pin 3: Rising-edge interrupt request pin. 
PC4 TO5	54 <sup>th</sup>	1	in/out out	Port C4: I/O port. Timer output 5: Output pin for timer 5.
PC5 TO7 INT4	53 <sup>rd</sup>	1	in/out out in	Port C5: I/O port. Timer output 7: Output pin for timer 7. Interrupt request pin 4: Rising-edge interrupt request pin. 
PD0 TI8 INT5 A16 WUINT0	41 <sup>st</sup>	1	in/out in in out in	Port D0: I/O port. Timer input 8: Input pin for timer 8. Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge. Address: Address bus 16. Wake up input 0: Wake up request pin with programmable rising, falling or both falling and rising edge. 
PD1 TI9 INT6 A17 WUINT1	42 <sup>nd</sup>	1	in/out in in out in	Port D1: I/O port. Timer input 9: Input pin for timer 9. Interrupt request pin 6: Rising-edge interrupt request pin. Address: Address bus 17. Wake up input 1: Wake up request pin with programmable rising, falling or both falling and rising edge. 
PD2 TO8 A18 WUINT2	43 <sup>rd</sup>	1	in/out out out in	Port D2: I/O port. Timer output 8: Output pin for timer 8 Address: Address bus 18. Wake up input 2: Wake up request pin with programmable rising, falling or both falling and rising edge. 
PD3 TO9 A19 WUINT3	44 <sup>th</sup>	1	in/out out out in	Port D3: I/O port. Timer output 9: Output pin for timer 9 Address: Address bus 19. Wake up input 3: Wake up request pin with programmable rising, falling or both falling and rising edge. 

Pin name	Pin number	Number of pins	In/Out	Function
PD4 TIA INT7 A20 WUINT4	45 <sup>th</sup>	1	in/out in in out in	Port D4: I/O port. Timer input A: Input pin for timer A Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge. Address: Address bus 20. Wake up input 4: Wake up request pin with programmable rising, falling or both falling and rising edge.
PD5 TIB A21 WUINT5	46 <sup>th</sup>	1	in/out in out in	Port D5: I/O port. Timer input B: Input pin for timer B. Address: Address bus 21. Wake up input 5: Wake up request pin with programmable rising, falling or both falling and rising edge.
PD6 TOA A22 WUINT6	47 <sup>th</sup>	1	in/out out out in	Port D6: I/O port. Timer output A: Output pin for timer A. Address: Address bus 22. Wake up input 6: Wake up request pin with programmable rising, falling or both falling and rising edge.
PD7 TOB A23 WUINT7	48 <sup>th</sup>	1	in/out out out in	Port D7: I/O port. Timer output B: Output pin for timer B. Address: Address bus 23. Wake up input 7: Wake up request pin with programmable rising, falling or both falling and rising edge.
PF0 TXD0	12 <sup>th</sup>	1	in/out out	Port F0: I/O port. Serial interface channel 0: Transmission data.
PF1 RXD0	11 <sup>th</sup>	1	in/out in	Port F1: I/O port. Serial interface channel 0: Receive data.
PF2 SCLK0 CTS0	10 <sup>th</sup>	1	in/out in/out in	Port F2: I/O port. Serial interface channel 0: Clock input/output. Serial interface channel 0: Data ready to send. (Clear-to-send)
PF3 TXD1	9 <sup>th</sup>	1	in/out out	Port F3: I/O port. Serial interface channel 1: Transmission data.
PF4 RXD1	8 <sup>th</sup>	1	in/out in	Port F4: I/O port. Serial interface channel 1: Receive data.
PF5 SCLK1 CTS1	7 <sup>th</sup>	1	in/out in/out in	Port F5: I/O port. Serial interface channel 1: Clock input/output. Serial interface channel 1: Data ready to send. (Clear-to-send)
PF6 TX	6 <sup>th</sup>	1	in/out out	Port F6: I/O port. CAN: Transmission data.
PF7 RX	5 <sup>th</sup>	1	in/out in	Port F7: I/O port. CAN: Receive data.
PG0..PG7 AN0..AN7	89 <sup>th</sup> ...96 <sup>th</sup>	8	in in	Port G: Input-only port. Analog input 0 to 7: AD converter input pins.
PL0..PL3 AN8..AN1 1	97 <sup>th</sup> ...100 <sup>th</sup>	4	in in	Port L0 to L3: Input-only port. Analog input 8 to 11: AD converter input pins.
PM0 <u>SS</u> A8	16 <sup>th</sup>	1	in/out in out	Port M0: I/O port. SEI: Slave select input. Address: Address bus 8.
PM1 MOSI A9	17 <sup>th</sup>	1	in/out in/out out	Port M1: I/O port. SEI: Master output, slave input. Address: Address bus 9.
PM2 MISO A10	18 <sup>th</sup>	1	in/out in/out out	Port M2: I/O port. SEI: Master input, slave output. Address: Address bus 10.
PM3 SECLK A11	19 <sup>th</sup>	1	in/out in/out out	Port M3: I/O port. SEI: Clock input/output. Address: Address bus 11.
PM4 SCK2	14 <sup>th</sup>	1	in/out in/out	Port M4: I/O port. SBI channel 2: Clock input/output at SIO mode.
PN0 SCK0	59 <sup>th</sup>	1	in/out in/out	Port N0: I/O port. SBI channel 0: Clock input/output at SIO mode.

Pin name	Pin number	Number of pins	In/Out	Function
PN1 SO0 SDA0	60 <sup>th</sup>	1	in/out out in/out	Port N1: I/O port. SBI channel 0: Output data input/output at SIO mode SBI channel 0: Data input/output at I <sup>2</sup> C mode
PN2 SIO SCL0	62 <sup>nd</sup>	1	in/out in in/out	Port N2: I/O port. SBI channel 0: Input data at SIO mode SBI channel 0: Clock input/output at I <sup>2</sup> C mode
PN3 SCK1 A12	64 <sup>th</sup>	1	in/out in/out out	Port N3: I/O port. SBI channel 1: Clock input/output at SIO mode Address: Address bus 12.
PN4 SO1 SDA1 A13	65 <sup>th</sup>	1	in/out out in/out out	Port N4: I/O port. SBI channel 1: Output data at SIO mode SBI channel 1: Data input/output at I <sup>2</sup> C mode Address: Address bus 13.
PN5 SI1 SCL1 A14	66 <sup>th</sup>	1	in/out in in/out out	Port N5: I/O port. SBI channel 1: Input data at SIO mode SBI channel 1: Clock input/output at I <sup>2</sup> C mode Address: Address bus 14
PN6 SO2 SDA2 A15	67 <sup>th</sup>	1	in/out out	Port N6: I/O port. SBI channel 2: Output data at SIO mode SBI channel 2: data input output at I <sup>2</sup> C mode Address: Address bus 15.
<u>NMI</u>	39 <sup>th</sup>	1	in	Non-maskable interrupt: Interrupt request pin with programmable falling or both falling and rising edge.
INT0	37 <sup>th</sup>	1	in	Interrupt request pin 0: Interrupt request pin with programmable level or rising-edge.
AM0,1	80 <sup>th</sup> , 78 <sup>th</sup>	2	in	Address mode pins: These pins are set as following, (Single-Chip mode) AM0 = L, AM1 = H (Single-Boot mode) AM0 = H, AM1 = H
TEST0,1	76 <sup>th</sup> , 71 <sup>st</sup>	2	in	Test mode pins: These pins are set as following, (Single Chip & Single Boot mode) TEST0 = L, TEST1 = L
CLK	77 <sup>th</sup>	1	out	Programmable clock output (with pull-up register).
X1/X2	74 <sup>th</sup> , 72 <sup>nd</sup>	2	in/out	Oscillator connecting pins
XT1/XT2	70 <sup>th</sup> , 69 <sup>th</sup>	2	in/out	Low frequency oscillator connecting pins. Crystal or ceramic resonator is connected. RC oscillation is also possible depending on MASK option.
RESET	79 <sup>th</sup>	1	in	Reset: Initializes LSI (with pull-up register).
VREFH	4 <sup>th</sup>	1	in	AD reference voltage high
VREFL	3 <sup>rd</sup>	1	in	AD reference voltage low
ADVCC	2 <sup>nd</sup>	1	-	Power supply pin for AD converter (+5V): Connect ADVCC pin to 5V power supply.
ADVSS	1 <sup>st</sup>	1	-	GND pin for AD converter: Connect ADVSS pin to GND (0V).
DVCC5	15 <sup>th</sup> , 40 <sup>th</sup> , 50 <sup>th</sup> , 61 <sup>st</sup> , 75 <sup>th</sup>	5	-	Power supply pins (+5V): Connect all DVCC5 pins to 5V power supply.
DVCC3	36 <sup>th</sup> , 63 <sup>th</sup> , 86 <sup>th</sup>	3	-	Power supply pins (+3.3V): Connect all DVCC3 pins to REGOUT pin.
DVSS	13 <sup>th</sup> , 38 <sup>th</sup> , 51 <sup>st</sup> , 63 <sup>rd</sup> , 73 <sup>rd</sup> , 88 <sup>th</sup>	6	-	GND: Connect all DVSS pins to GND (0V).
REGOUT	49 <sup>th</sup>	1	out	Regulator output 3.3V: Connect capacitor to stabilize the regulator output.
REGEN	52 <sup>nd</sup>	1	in	Regulator enable pin: Should be set to H or OPEN (with pull-up register).

### 3. OPERATION

This section describes the basic components, functions and operation of TMP92FD54AI.

#### 3.1 CPU

TMP92FD54AI contains an advanced high-speed 32-bit CPU (900/H1 CPU)

##### 3.1.1 CPU Outline

900/H1 CPU is high-speed and high-performance CPU based on 900/H CPU. 900/H1 CPU has expanded 32-bit internal data bus to process Instructions more quickly.

Outline of 900/H1 CPU are as follows:

900/H1 CPU		
Width of CPU Address Bus	24-bit	
Width of CPU Data Bus	32-bit	
Internal Operating Frequency	16 to 20MHz (@fosc=8 to 10MHz)	
Minimum Bus Cycle (Internal RAM)	1-clock access (50ns@fosc=10MHz)	
Internal RAM	32-bit 1-clock access	
Internal ROM	32-bit interleave 2-1-1-1-clock access	
Internal I/O	8/16-bit 2-clock access	PORT, INTC, MEMC
	8/16-bit 5 to 6-clock access	SEI, SIO, WDT, 8-bit Timer, 16-bit Timer, RTC, 10-bit ADC, SBI, CAN
External Device	8-bit 2-clock access (can insert some waits)	
Minimum Instruction Execution Cycle	1-clock(50ns@fosc=10MHz)	
Conditional Jump	2-clock(100ns@fosc=10MHz)	
Instruction Queue Buffer	12-byte	
Instruction Set	Compatible with TLCS-900, 900/H, 900/L, 900/L1 and 900/H2 (NORMAL, MIN, MAX and LDX instruction is deleted)	
Micro DMA	8-channels	

## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V <sub>CC5</sub>	-0.5 to 6.0	V
Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>CC5</sub> +0.5	V
Output Current(total)	ΣI <sub>OL</sub>	100	mA
Output Current(total)	ΣI <sub>OH</sub>	-100	mA
Power Dissipation(Ta=85degree C)	P <sub>D</sub>	600	mW
Soldering Temperature(10s)	T <sub>SOLDER</sub>	260	degree C
Storage Temperature	T <sub>STG</sub>	-65 to 150	degree C
Operation Temperature	T <sub>OPR</sub>	-40 to 85	degree C
Operation Temperature (Flash Program / Erase)		0 to 70	
The number of write erase cycles	N <sub>EW</sub>	100	Cycle

Note: The absolute maximum ratings are rated values that must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products that include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 5.2 DC Electrical Characteristics

Vcc5 = 4.5V to 5.25V / fc = 16 to 20MHz / Ta = -40 to 85 degree C

Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V <sub>CC5</sub>		4.5	5.25	V
Input Low Voltage P00 to P07(D0 to 7) PG0 to PG7 PL0 to PL3	V <sub>IL0</sub>		-0.3	0.8	V
Input Low Voltage P00 to P07(PORT) P40 to P47	V <sub>IL1</sub>		-0.3	0.3*VCC5	V
Input Low Voltage INT0 NMI RESET P70,P71,P73 to P75 PC0 to PC5 PD0 to PD7 PF0 to PF7 PM0 to PM4	V <sub>IL2</sub>		-0.3	0.25*VCC5	V
P72, PN0 to PN6	V <sub>IL6</sub>		-0.3	0.3*VCC5	V
Input Low Voltage AM0 to AM1 TEST0 to TEST1	V <sub>IL3</sub>		-0.3	0.3	V
Input Low Voltage X1, XT1 (Crystal)	V <sub>IL4</sub>	* Vcc3 = 3.3V	-0.3	0.2*VCC3	V
Input Low Voltage XT1 (CR)	V <sub>IL5</sub>	* Vcc3 = 3.3V	-0.3	0.2*VCC3	V
Input High Voltage P00 to P07(D0 to 7) PG0 to PG7 PL0 to PL3	V <sub>IH0</sub>		2.2	VCC5+0.3	V
Input High Voltage P00 to P07 P40 to P47	V <sub>IH1</sub>		0.7*VCC5	VCC5+0.3	V
Input High Voltage INT0 NMI RESET P70,P71,P73 to P75 PC0 to PC5 PD0 to PD7 PF0 to PF7 PM0 to PM4	V <sub>IH2</sub>		0.75*VCC5	VCC5+0.3	V
P72, PN0 to PN6	V <sub>IH6</sub>		0.7*VCC5	VCC5+0.3	V
Input High Voltage AM0 to AM1 TEST0 to TEST1	V <sub>IH3</sub>		VCC5-0.3	VCC5+0.3	V
Input High Voltage X1, XT1 (Crystal)	V <sub>IH4</sub>	* Vcc3 = 3.3V	0.8*VCC3	VCC3+0.3	V
Input High Voltage XT1 (CR)	V <sub>IH5</sub>	* Vcc3 = 3.3V	0.7*VCC3	VCC3+0.3	V

Parameter	Symbol	Condition		Min	Max	Unit
Output Low Voltage	$V_{OL}$	$I_{OL} = 3.0\text{mA}$			0.4	V
Output High Voltage	$V_{OH0}$	$I_{OH} = -400\mu\text{A}$	2.4			V
	$V_{OH1}$	$I_{OH} = -100\mu\text{A}$	0.75*VCC5			
	$V_{OH2}$	$I_{OH} = -20\mu\text{A}$	0.9*VCC5			
	$V_{OHn}$	$I_{OH} = -200\mu\text{A}$ , PF6(TX) pin	0.82*VCC5			
Input Leakage Current	$I_{LI}$	$0.0 \leq V_{in} \leq V_{CC5}$		0.02(typ.)	$\pm 5$	uA
Output Leakage Current	$I_{LO}$	$0.2 \leq V_{in} \leq V_{CC5}-0.2$		0.05(typ.)	$\pm 10$	uA
Operating Current (Single Chip)*	$I_{CC5}$	$V_{CC5}=5.25\text{V}$ , $X1=10\text{MHz}$ (Internal 20MHz)		80(typ)	100	mA
Operating Current (Stand-by)	$I_{CC5IDLE2}$	IDLE2 Mode	$V_{CC5}=5.25\text{V}$ , $X1=10\text{MHz}$ (Internal 20MHz)		90	mA
	$I_{CC5IDLE1}$	IDLE1 Mode	$V_{CC5}=5.25\text{V}$ , $X1=10\text{MHz}$ (Internal 20MHz)		30	
	$I_{CC5IDLE3}$	IDLE3 Mode	$V_{CC5}=5.25\text{V}$ , $T_a = -40$ to $85$ degree C $V_{CC5}=5.25\text{V}$ , $T_a = -10$ to $55$ degree C		220 140	uA
	$I_{CC5STOP}$	STOP Mode	$V_{CC5}=5.25\text{V}$ , $T_a = -40$ to $85$ degree C $V_{CC5}=5.25\text{V}$ , $T_a = -10$ to $55$ degree C		200 120	uA
Stand-by Voltage	$V_{STB5}$	$V_{CC3} < V_{CC5}$ , $V_{IH1} < V_{CC5}$ , $V_{IH2} < V_{CC5}$ , $V_{IH3} < V_{CC5}$		3.0	5.25	V
Pull-up Resistor	$R_{RST}$	RESET		60	220	K ohm
	$R_{CLK}$	CLK				
Schmitt Width	$V_{TH}$	INT0, NMI, RESET, P70 to P75, PC0 to PC5, PD0 to PD7, PF0 to PF7, PM0 to PM4, PN0 to PN6		0.4	1.0(typ.)	V

\*: On condition that external bus don't operate

V<sub>CC5</sub> = 4.5V to 5.25V / f<sub>C</sub> = 16 to 20MHz / T<sub>A</sub> = -40 to 85 degree C  
 (T<sub>A</sub>=0 to 70 degree C during programming or erasing of flash memory)

Parameter	Symbol	Condition	Min	Max	Unit
Mean operating current (during reading)	I <sub>DDO1</sub>	f <sub>C</sub> = 20 MHz	80	100	mA
Mean operating current (during programming)	I <sub>DDO2</sub>		—	100	mA
Mean operating current (during erasing)	I <sub>DDO3</sub>		—	110	mA
Standby current	I <sub>DDS</sub>	V <sub>CC5</sub> =5.25V, T <sub>A</sub> = -40 to 85 degree C V <sub>CC5</sub> =5.25V, T <sub>A</sub> = -10 to 55 degree C	—	200 120	uA

Note: Precautions when programming/erasing flash memory

- 1) In On-Board Programming Mode (Single-Boot Mode or User Boot Mode), inhibit all interrupts including NMI to allow the highest priority for program/erase operations.
- 2) To rewrite data in already programmed addresses, execute an Auto Erase before executing Auto Program.

## 5.3 AC Characteristics

## Read cycle

VCC5=4.5 to 5.25V±5%, TA=-40 to 85 degree C							
No.	Parameter	Symbol	Min	Max	@20MHz	@16MHz	Unit
1	OSC period (X1/X2)	$t_{osc}$	100	125	100	125	ns
2	System Clock period (=T)	$t_{cyc}$	50	62.5	50	62.5	ns
3	CLK Low Width	$t_{cl}$	$0.5 \times T-15$		10	16	ns
4	CLK High Width	$t_{ch}$	$0.5 \times T-15$		10	16	ns
5-1	A0 to A23 Valid → D0 to D7 Input @0WAIT	$t_{ad}$		$2.0 \times T-50$	50	75	ns
5-2	A0 to A23 Valid → D0 to D7 Input @1WAIT	$t_{ad3}$		$3.0 \times T-50$	100	138	ns
6-1	$\overline{RD}$ Fall → D0 to D7 Input @0WAIT	$t_{rd}$		$1.5 \times T-45$	30	49	ns
6-2	$\overline{RD}$ Fall → D0 to D7 Input @1WAIT	$t_{rd3}$		$2.5 \times T-45$	80	111	ns
7-1	$\overline{RD}$ Low Width @0WAIT	$t_{rr}$	$1.5 \times T-20$		55	74	ns
7-2	$\overline{RD}$ Low Width @1WAIT	$t_{rr3}$	$2.5 \times T-20$		105	136	ns
8	A0 to A23 Valid → $\overline{RD}$ Fall	$t_{ar}$	$0.5 \times T-20$		5	11	ns
9	RD Fall → CLK Fall	$t_{rk}$	$0.5 \times T-20$		5	11	ns
10	A0 to A23 Valid → D0 to D7 Hold	$t_{ah}$	0		0	0	ns
11	RD Rise → D0 to D7 Hold	$t_{hr}$	0		0	0	ns
12	A0 to A23 Valid → PORT Input	$t_{apr}$		$2.0 \times T-120$	-20	5	ns
13	A0 to A23 Valid → PORT Hold	$t_{aph}$	$2.0 \times T$		100	125	ns
14	WAIT Set-up Time	$t_{tk}$	15		15	15	ns
15	WAIT Hold Time	$t_{kt}$	5		5	5	ns

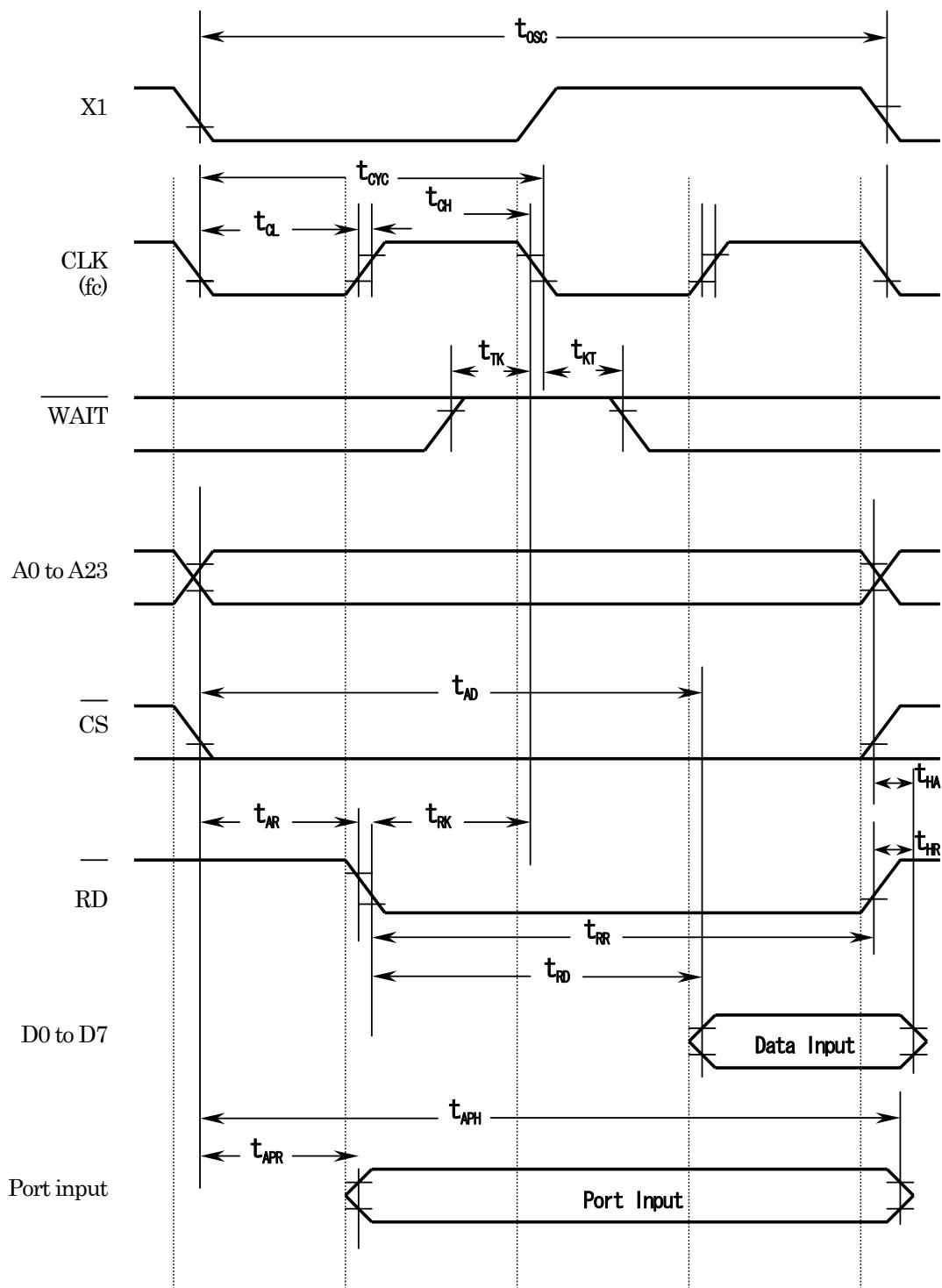
## Write cycle

VCC5=5.0V±5%, TA=-40 to 85 degree C							
No.	Parameter	Symbol	Min	Max	@20MHz	@16MHz	Unit
1	OSC period (X1/X2)	$t_{osc}$	100	125	100	125	ns
2	System Clock period (=T)	$t_{cyc}$	50	62.5	50	62.5	ns
3	CLK Low Width	$t_{cl}$	$0.5 \times T-15$		10	16	ns
4	CLK High Width	$t_{ch}$	$0.5 \times T-15$		10	16	ns
5-1	D0 to D7 Valid → $\overline{WR}$ Rise @0WAIT	$t_{dw}$	$1.25 \times T-35$		28	43	ns
5-2	D0 to D7 Valid → $\overline{WR}$ Rise @1WAIT	$t_{dw3}$	$2.25 \times T-35$		78	106	ns
6-1	$\overline{WR}$ Low Width @0WAIT	$t_{ww}$	$1.25 \times T-30$		33	48	ns
6-2	$\overline{WR}$ Low Width @1WAIT	$t_{ww3}$	$2.25 \times T-30$		83	111	ns
7	A0 to A23 Valid → $\overline{WR}$ Fall	$t_{aw}$	$0.5 \times T-20$		5	11	ns
8	$\overline{WR}$ Fall → CLK Fall	$t_{wk}$	$0.5 \times T-20$		5	11	ns
9	$\overline{WR}$ Fall → A0 to A23 Hold	$t_{wa}$	$0.25 \times T-5$		8	11	ns
10	$\overline{WR}$ Fall → D0 to D7 Hold	$t_{wd}$	$0.25 \times T-5$		8	11	ns
11	A0 to A23 Valid → PORT Output	$t_{apw}$		$2.0 \times T+70$	170	195	ns
12	WAIT Set-up Time	$t_{tk}$	15		15	15	ns
13	WAIT Hold Time	$t_{kt}$	5		5	5	ns
14	RD Rise → D0 to D7 Output	$t_{rdo}$	$1.25 \times T-35$		20	26	ns

## AC Condition

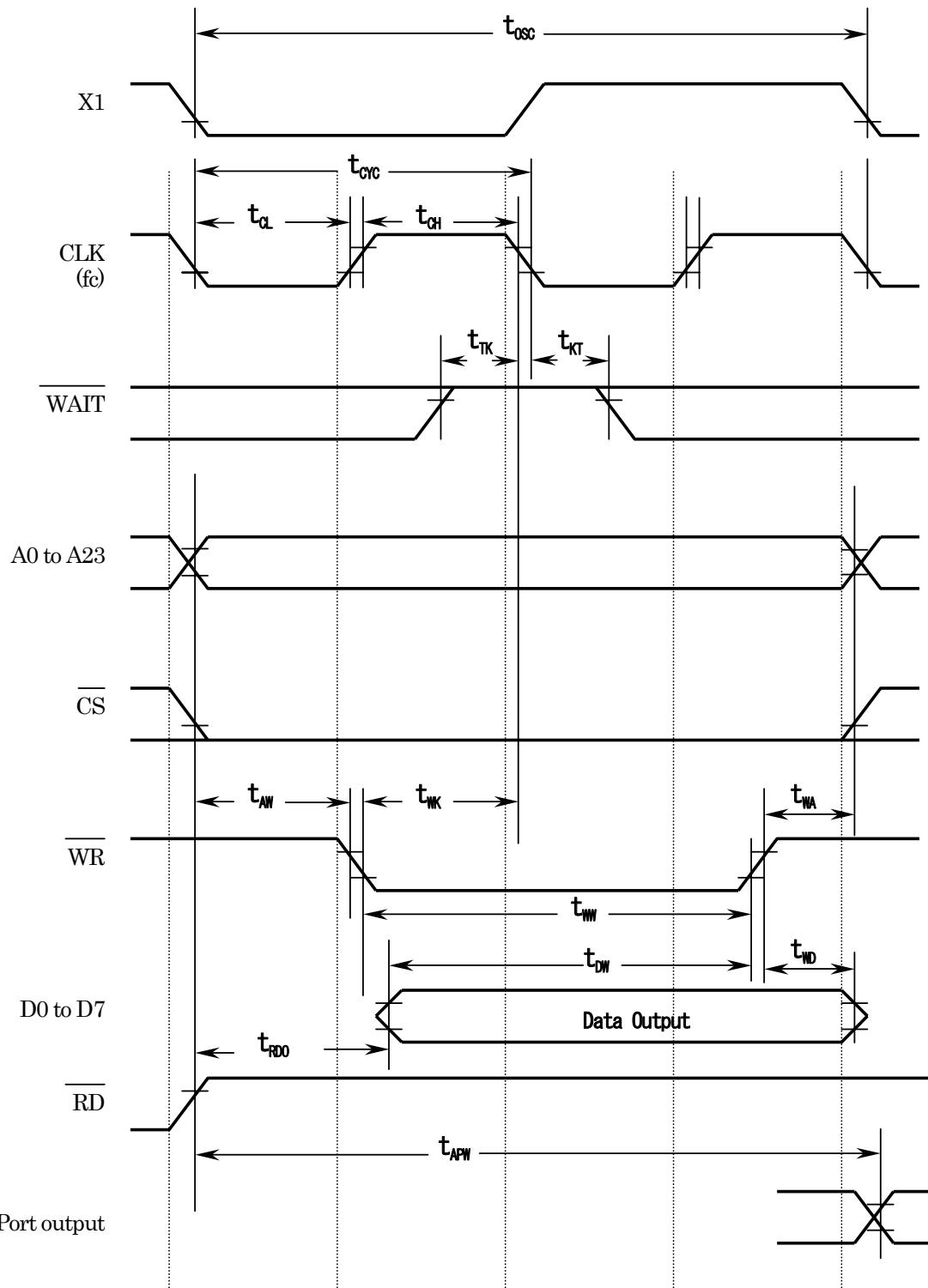
- Output : D0 to D7, A0 to A7, A8 to A15, A16 to A23,  $\overline{RD}$ ,  $\overline{WR}$   
High 2.0V, Low 0.8V, CL=50pF  
Others High 2.0V, Low 0.8V, CL=50pF
- Input : D0 to D7  
High 2.4V, Low 0.45V, CL=50pF  
Others High 0.8×VCC5, Low 0.2×VCC5

## (1) Read cycle (0 wait)



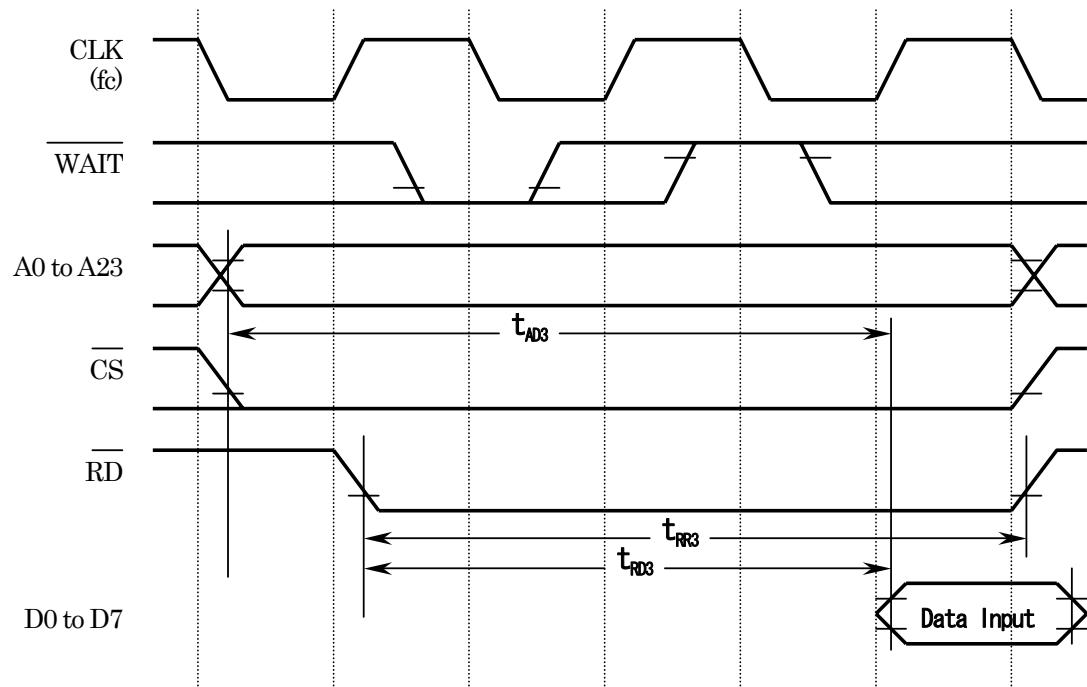
Note : The phase relation between X1 input signal and the other signals is unsettled.  
The timing chart above is an example.

(2) Write cycle (0 wait)

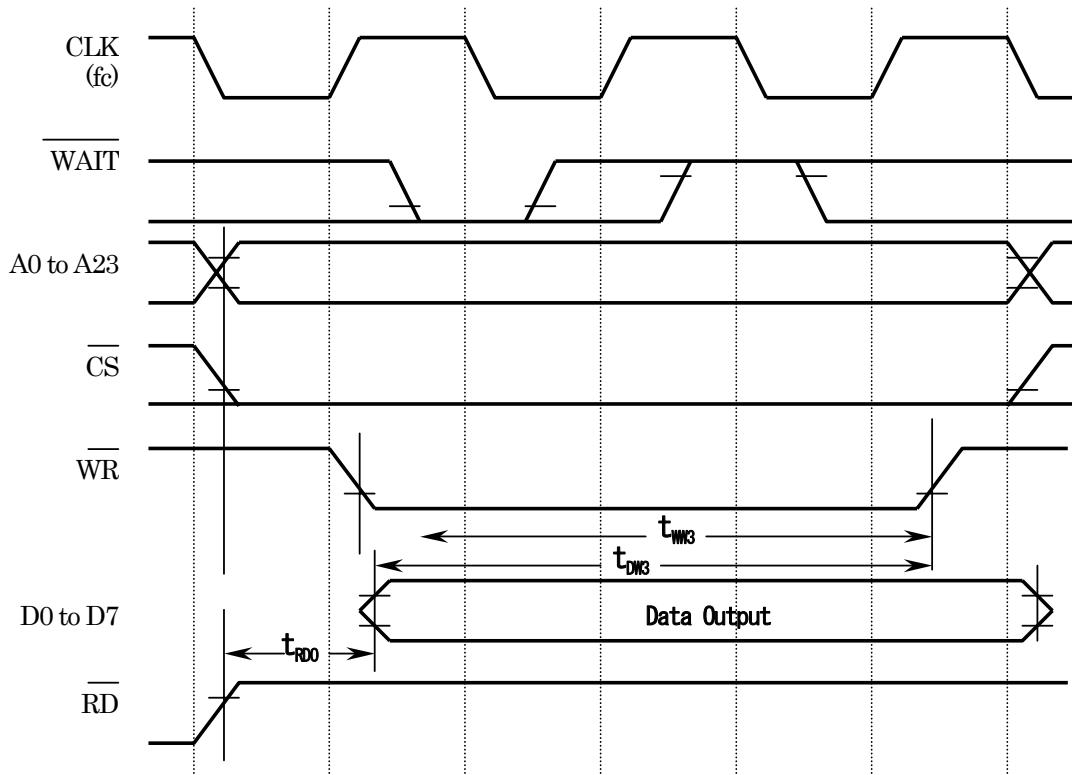


Note : The phase relation between X1 input signal and the other signals is unsettled.  
The timing chart above is an example.

## (3) Read cycle (1 wait)



## (4) Write cycle (1 wait)



## 5.4 AD Conversion Characteristics

Symbol	Parameter	Min	Typ	MAX	Unit
VREFH	Analog reference voltage(+)	VCC5-0.2	VCC5	VCC5	V
VREFL	Analog reference voltage(-)	VSS5	VSS5	VSS5	
AVCC	AD Converter Power Supply Voltage	VCC5-0.2	VCC5	VCC5	
AVSS	AD Converter Ground	VSS5	VSS5	VSS5	
AVIN	Analog Input Voltage	VREFL		VREFH	
IREF	Analog Current for analog reference voltage <VREFON>=1		0.8	1.2	mA
	<VREFON>=0		0.02	5	uA
ET	Total error (excluding quantize error)			±3.0	LSB

Note) "LSB" is the UNIT which means the resolution of AD CONVERTER. ( $\pm 3 \text{ LSB} = 3 * \text{VCC}/1024 = \pm 15 \text{mV}$ )

## 5.5 Event Counter (TI0, TI4, TI8, TI9, TIA, TIB)

Parameter	Symbol	Variable		20MHz		16MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	tVCK	8T+100		500		600		ns
Clock Low Width	tVCKL	4T+40		240		290		ns
Clock High Width	tVCKH	4T+40		240		290		ns

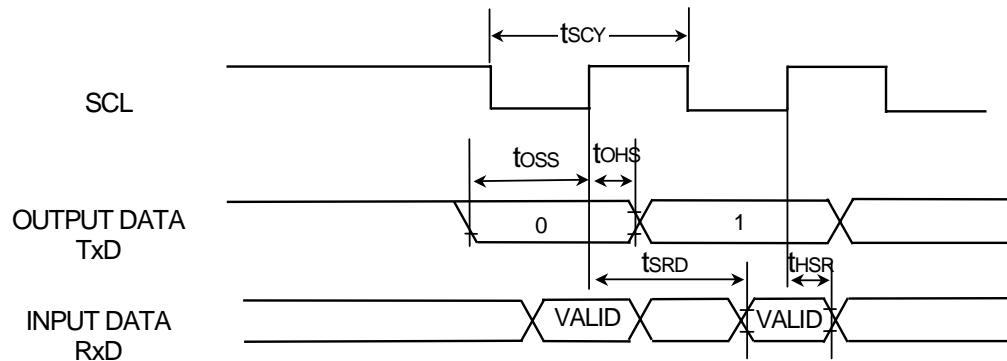
## 5.6 Serial Channel Timing

### (1) SCLK Input mode (I/O Interface mode)

Parameter	Symbol	Variable		20MHz		16MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle	tSCY	16T		0.8		1.0		us
Output Data → SCLK Rise	toss	tSCY/2-4T -110		90		140		ns
SCLK Rise → Output Data Hold	tOHS	tSCY/2+2T		500		625		
SCLK Rise → Input Data Hold	tHSR	3T+10		160		197.5		
SCLK Rise → Input Data Valid	tSRD		tSCY		800		1000	

### (2) SCLK Output mode (I/O Interface mode)

Parameter	Symbol	Variable		20MHz		16MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle (programmable)	tSCY	16T	8192T	0.8	409.6	1.0	512	us
Output Data → SCLK Rise	toss	tSCY/2-40		360		460		ns
SCLK Rise → Output Data Hold	tOHS	tSCY/2-40		360		460		
SCLK Rise → Input Data Hold	tHSR	0		0		0		
SCLK Rise → Input Data Valid	tSRD		tSCY/2-T -180		570		757.5	



## (3) SCLK Input mode (UART mode) (Preliminary)

Parameter	Symbol	Variable		20MHz		16MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle	$T_{SCY}$	4T + 20		220		270		ns
SCLK Low level Pulse width	$T_{SCYL}$	2T + 5		105		130		
SCLK High level Pulse width	$T_{SCYH}$	2T + 5		105		130		

## 5.7 Interrupt Operation

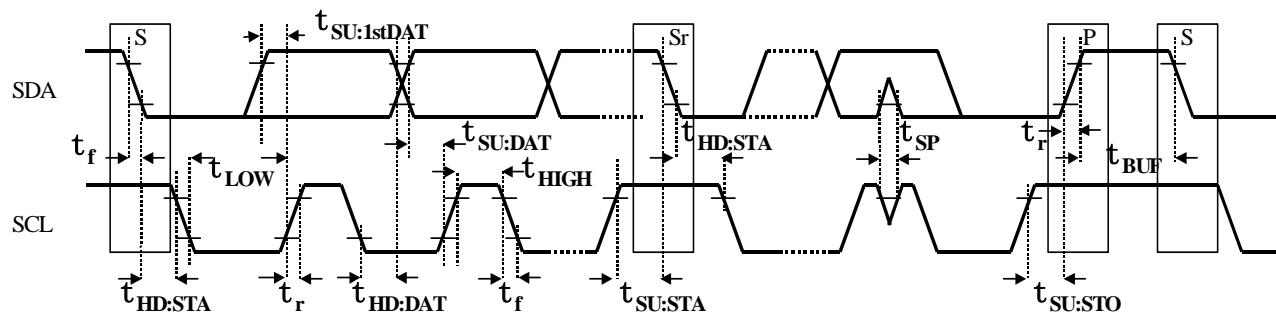
Parameter	Symbol	Variable		20MHz		16MHz		Unit
		Min	Max	Min	Max	Min	Max	
NMI,INT0 Low Width	$T_{INTAL}$	4T		200		250		ns
NMI,INT0 High Width	$T_{INTAH}$	4T		200		250		
WUINT0 to WUINT7, INT1 to INT7 Low Width	$T_{INTBL}$	8T+100		500		600		
WUINT0 to WUINT7, INT1 to INT7 High Width	$T_{INTBH}$	8T+100		500		600		

## 5.8 Serial bus interface

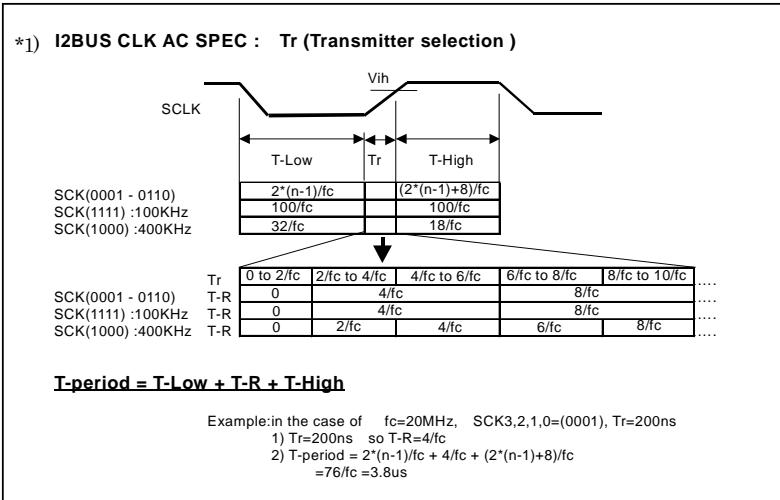
## I2CBUS-AC-SPEC TABLE

No	PARAMETER	(fc=20MHz)				(fc=System clock)	
		SYMBOL	UNIT	400KHz		100KHz	
				MIN	MAX	MIN	MAX
1	SCL clock frequency	$f_{\text{scl}}$	KHz	0	400	0	100
	Hold time (repeated) START condition.						
2	After this period, the first clock pulse is generated.	$t_{\text{HD:STA}}$	ns	650	-	4500	-
3	LOW period of the SCL clock	$t_{\text{LOW}}$	ns	1300	-	4700	-
4	HIGH period of the SCL clock	$t_{\text{HIGH}}$	ns	600	-	4000	-
5	Set-up time for a repeated START condition	$t_{\text{SU:STA}}$	ns	by software		by software	
6	Data hold time: for CBUS compatible masters for I2C-bus devices	$t_{\text{HD:DAT}}$	ns	0	900	0	3450
7	Data set-up time	$t_{\text{SU:DAT}}$	ns	100	-	250	$(2^{n-1}/fc)$
7'	Data set-up time (The case in the first bit after transfer )	$t_{\text{SU:1stDAT}}$	↑	↑	↑	↑	$(2^{n-1}-12)/fc$
8	Rise time of both SDA and ACL signals (*1)	$t_r$	ns	-	300 (receive)	- (receive)	-
9	Fall time of both SDA and ACL signals	$t_f$	ns	-	300	300	-
10	Set-up time for STOP condition	$t_{\text{SU:STO}}$	ns	950	-	4200	$(2^{n-1}+12)/fc$
11	Bus free time between a STOP and START condition	$t_{\text{BUF}}$	ns	by software		by software	
12	Capacitive load for each bus line	$C_b$	pF		400	400	400
13	Noise margin at the LOW level for each connected device (including hysteresis)	$V_{NL}$	v	0.2V <sub>DD5</sub>	-	0.2V <sub>DD5</sub>	-
14	Noise margin at the HIGH level for each connected device (including hysteresis)	$V_{NH}$	v	0.2V <sub>DD5</sub>	-	0.2V <sub>DD5</sub>	-
15	Pulse width of spikes which must be suppressed by the input filter	$t_{\text{sp}}$	ns	0	50	n/a	n/a

Note

1 All values referred to  $V_{IL\text{min}}$  and  $V_{IL\text{max}}$  levels.

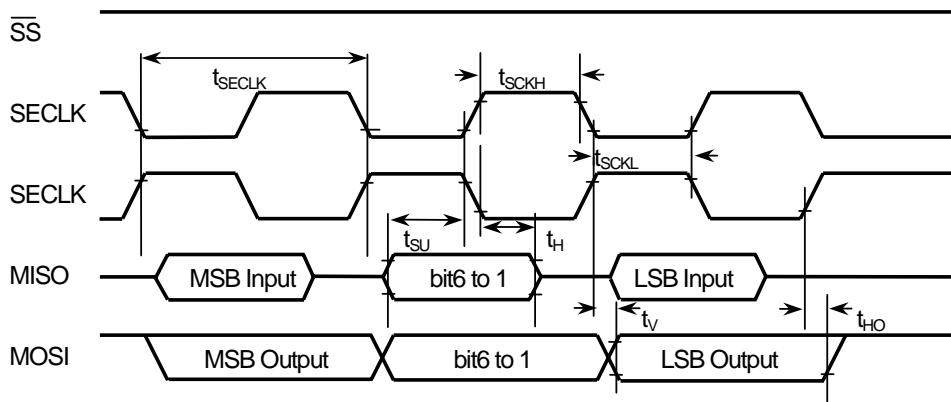
S : Start P :Stop Sr : ReStart



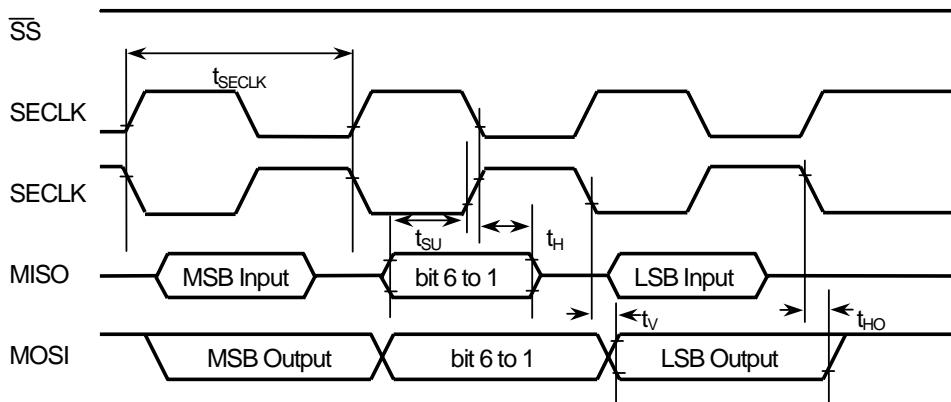
## 5.9 Serial Expansion Interface

Symbol	Parameter	Variable		20MHz		Unit
		Min	Max	Min	Max	
$t_{SECLK}$	SECLK Cycle	5T	40T	250	2000	ns
$t_{LEAD}$	SS fall $\rightarrow$ SECLK	4T		200		ns
$t_{LAG}$	SECLK $\rightarrow$ SS rise	4T		200		ns
$t_{SCKH}$	SECLK High Pulse Width	$t_{SECLK}/2\text{-}9$		116		ns
$t_{SCKL}$	SECLK Low Pulse Width	$t_{SECLK}/2\text{-}9$		116		ns
$t_{SU}$	Input Data Set-up	$t_{SECLK}/4\text{-}10$		52		ns
$t_H$	Input Data Hold	$t_{SECLK}/4$		62		ns
$t_v$	Output Data Valid		$t_{SECLK}/4$		62	ns
$t_{HO}$	Output Data Hold	0		0		ns

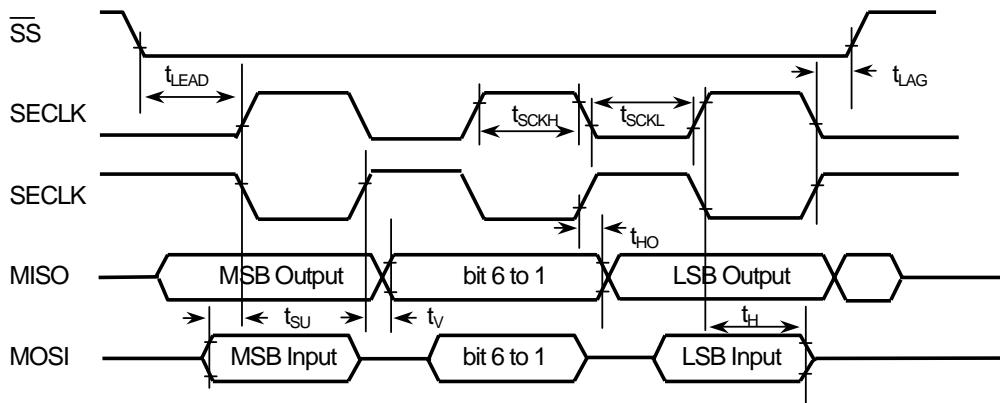
a) SEI Master (CPHA=0)



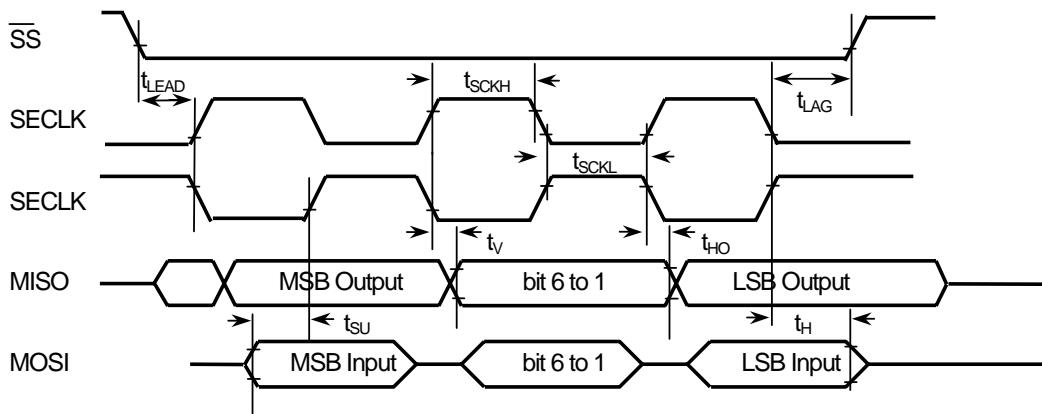
b) SEI Master (CPHA=1)



c) SEI Slave (CPHA=0)

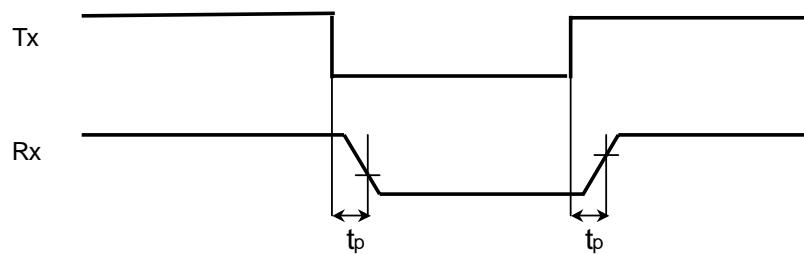


d) SEI Slave (CPHA=1)



## 5.10 Controller Area Network (CAN)

Symbol	Parameter	Variable		20MHz		Unit
		Min	Max	Min	Max	
$t_{clk}$	CAN Clock period	2T		100		ns
$t_p$	Tx edge → Rx Input			2tcclk-20	180	ns



## 5.11 Voltage regulator

## Voltage Regulator

Vcc5 = 4.5V to 5.25V / fc = 16 to 20MHz / Ta = -40 to 85 degree C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.
Output Voltage	REGOUT		3.0	—	3.6	V
Output Current	Iro	Vin-REGOUT=1.0V	0	—	150	mA
Quiescent Current	Iq	Iro≤10 uA	30	50	100	μ A
	Iq1	10 uA < Iro < 100mA (Ta=25°C)	15	250	800	μ A
	Iop	Iro=150mA	6	8	10	mA
Standby Current	Is	REGEN=0 (Regulator Only)	—	0.1	0.2	μ A

0.5[Ohm] ≤ ESR ≤ 5.0[Ohm]

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.
Stabilization capacitor	Cs	Cb=10uF, ESR=4.7Ω	0.1	—	10	μ F
Bypass capacitor	Cb	Cs=10uF, ESR=4.7Ω (Cs>=Cb)	0.1	—	10	μ F
Input capacitor	Cin (Note)	Cs=10uF, ESR=4.7Ω	4.7	—	22	μ F
Equivalent Series Resistor	ESR	Cs=10uF Cb=0.1uF	0.5	—	5	Ω

0.5[Ohm] ≤ ESR ≤ 50[Ohm]

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.
Stabilization capacitor	Cs	Cb=0.6uF, ESR=47Ω	0.1	—	10	μ F
Bypass capacitor	Cb	Cs=10uF, ESR=47Ω (Cs>=Cb)	0.6	—	10	μ F
Input capacitor	Cin (Note)	Cs=10uF, ESR=47Ω	4.7	—	22	μ F
Equivalent Series Resistor	ESR	Cs=10uF Cb=0.6uF	0.5	—	50	Ω

0.5[Ohm] ≤ ESR ≤ 100[Ohm]

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.
Stabilization capacitor	Cs	Cb=1.0uF, ESR=100Ω	0.1	—	10	μ F
Bypass capacitor	Cb	Cs=10uF, ESR=100Ω (Cs>=Cb)	1.0	—	10	μ F
Input capacitor	Cin (Note)	Cs=10uF, ESR=100Ω	4.7	—	22	μ F
Equivalent Series Resistor	ESR	Cs=10uF Cb=1.0uF	0.5	—	100	Ω

Note: Recommend Tantalum Capacitor.

