Advanced Product / Process Change Notice

PCN No.: Z200-PCN-DM201301-01-A Date : Jan. 7, 2013

Change Title : **W25Q64FW "F-Series" (58nm) to replace W25Q64DW "D-Series" (90nm) 64Mb 1.8V SpiFlash® Memories**

Change Classification: ☑ **Major** ☐Minor
Change item: ☑ **Design** ☐ Raw Material ☐ Wafer FAB ☐ Package Assembly ☐ Testing ☐ Others : _____.

Affected Product(s): 90nm 64Mb "D-Series" SpiFlash memories:
W25Q64DWSSIG , W25Q64DWSFIG, W25Q64DWSTIG, W25Q64DWSTIM, W25Q64DWZPIG, W25Q64DWZEIG, W25Q64DWWC

Description of Change(s) :

The W25Q64FW 64Mb SpiFlash® Memories use Winbond's 58nm Flash technology. It is function-compatible to W25Q64DW 90nm devices offering improved performance, features and availability.

Reason for Change(s):

1) Technology Migration from 90nm to 58nm on 12" wafer
2) Improved Features (see below)

Features

- Advanced 58nm SpiFlash Technology
- Command compatible with W25Q64DW (same JEDEC Device ID, Superset Instruction Set)
- Individual Block Write Protection in addition to the existing protection schemes
- Additional configurable hardware /RESET pin
- Programmable Output Driver Strength

Benefits

- 58nm Technology allows for improved availability and best possible future pricing
- Faster Read performance

Impact of Change(s) : (positive & negative)

Form: No Change

Fit: No Change

Function: No System Change*

Reliability: No concern (Attachment I 58nm SPI Serial Flash Reliability Report is attached as reference)

Hazardous Substances: No concern (see Appendix I)

* No system change is needed unless new features (QPI, Software Reset) will be used.

Qualification Plan/ Results :

Based on Winbond W25Q64FW Serial Flash Reliability report, the new product meets our criteria and no quality concern (refers to Attachment I in details).

Implementation Plan :

Please refer to Attachment for details

☐ Date Code : _____ onward ☐ Lot No.: _____ onward ☑ Implemented date: (See Attachment) .

Originator:(QA Sec. Manager)	Y.H Chang	***Responsible: (QA Dept. Manager)***	Y.H Chang	***Approval:(QRA Director)***	Yu-Sung, Cheng

Contact for Questions & Concerns	Name: Hannah Cheng TEL:886-3-5678168 (ext.6553) FAX: 886-3-5796124 Address : # 539, Sec. 2, Wenxing Rd., Jhubei City, Hsinchu County 302, Taiwan E-mail: yhcheng2@winbond.com

Customer Comments:

Note: Please sign this notice, and return to Winbond contact within 30 days. If no response is received within 30 days, this Change Request will be assumed to meet your approval.

☐ Approval ☐ Disapproval ☐ Conditional Approval : _____.

Date: _____

Dept. name:_____

Person in charge:_____.

Table 1 The impact product list: Primary Winbond replacement part numbers for 90nm W25Q64DW D-Series products are listed below. These devices offer the best future availability. Availability of W25Q64DW Automotive Grade products are not affected by this notice.

Winbond Current PN (90nm D-Series)	Winbond Primary Replacement PN (58nm F-Series)
W25Q64DWSSIG	W25Q64FWSSIG
W25Q64DWSFIG	W25Q64FWSFIG
W25Q64DWSTIG	W25Q64FWSTIG
W25Q64DWSTIM	W25Q64FWSTIM
W25Q64DWZPIG	W25Q64FWZPIG
W25Q64DWZEIG	W25Q64FWZEIG
W25Q64DWWC	W25Q64FWWC

PRIMARILY RELIABILITY REPORT

W25Q64FW

PART NO. : W25Q64FW

FUNCTION : 1.8V 64M FLASH MEMORY

PROCESS : 58nm CMOS (DPTM)

RA ENGINEER: W R. Chang

RA MANAGER: K F. Chuang

~SUMMARY~

W25Q64FW for 8-VSOP 208 mil passed the reliability items as follows:

- **High Temp. Operating : 0/231 pcs**
- **Data Retention : 0/231 pcs**
- **Endurance Cycling with Data Retention : 0/231 pcs**
- **Pre-Condition Test : 0/924 pcs**
- **High Temp. Storage Life Test : 0/231 pcs**
- **Pressure Cooker Test : 0/231 pcs**
- **Temperature Cycle Test : 0/231 pcs**
- **Highly Accelerated Stress Test : 0/231 pcs**
- **ESD-HBM : 0/36 pcs**
- **ESD-MM : 0/36 pcs**
- **ESD-CDM : 0/9 pcs**
- **Latch -Up Test : 0/18 pcs**

---CONTENTS---

Ⅲ. ENVIRONMENTAL TEST

A. Introduction

1. Pre-Condition Test
2. High Temp. Storage Life Test (HTSL)
3. Pressure Cooker Test (PCT)
4. Highly Accelerated Stress Testing (HAST)
5. Temperature Cycle Test (TCT)

B. Test Results

1. Pre-Condition Test
2. High Temp. Storage Life Test (HTSL)
3. Pressure Cooker Test (PCT)
4. Highly Accelerated Stress Testing (HAST)
5. Temperature Cycle Test (TCT)

Ⅳ. ESD & LATCH-UP

A. Introduction

1. ESD
2. LATCH-UP

B. Test Results

1. ESD
2. LATCH-UP

I. PRODUCT DESCRIPTION

A. Introduction

The W25Q64FW (64M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The devices operate on a single 1.65V to 1.95V power supply with current consumption as low as 4mA active and 1μA for power-down. All devices are offered in space-saving packages.

The W25Q64FW array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q64FW has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The W25Q64FW supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad peripheral interface(QPI): Serial Clock, Chip Select, Serial Data I/O0(DI),I/O1(DO),I/O2(/WP), and I/O3(/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHZ x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

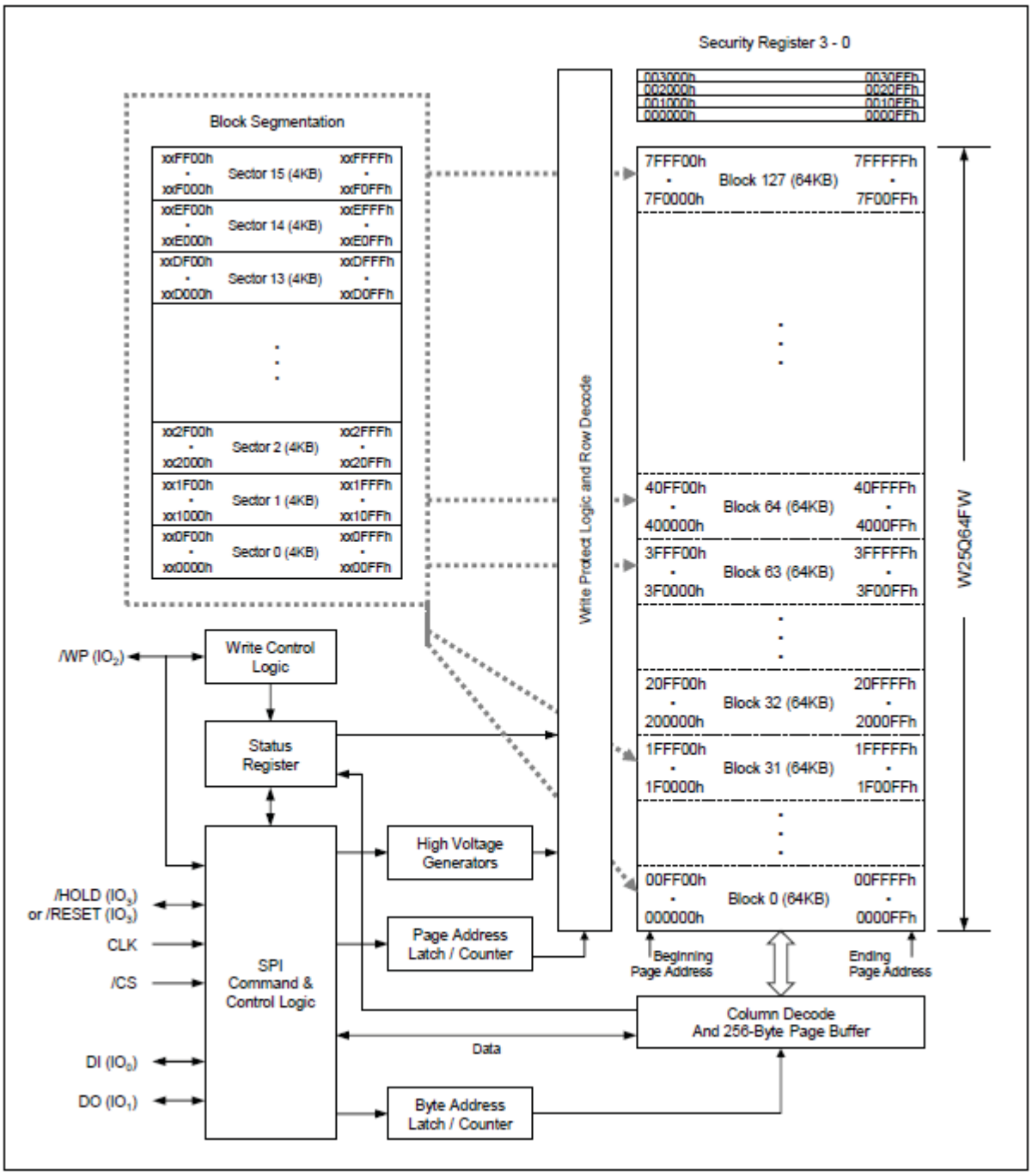
A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provides further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

B. Features

- New Family of SpiFlash Memories
  - W25Q64FW: 64M-bit / 8M -byte
  - Standard SPI: CLK,/CS,DI,DO,/WP,/Hold
  - Dual SPI: CLK,/CS,IO0,IO1,/WP,/Hold
  - Quad SPI: CLK,/CS,IO0,IO1,IO2,IO3
  - QPI: CLK, /CS,IO0,IO1,IO2,IO3
  - Software & Hardware Reset
- Highest Performance Serial Flash
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate.
  - More than 100,000 erase/write cycles
  - More than 20-year data retention
- Efficient “Continuous Read Mode”and QPI Mode
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Quad Peripheral interface (QPI) reduces instruction overhead
  - Allows true XIP(excute in place) operation
  - Outperforms X16 Parallel Flash
- Low Power, Wide Temperature Range
  - Single 1.65 to 1.95V supply
  - 4mA active current, <1μA Power-down (typ.)
  - -40° C to +85°C operating range
- Flexible Architecture with 4KB sectors
  - Uniform Sector/Block Erase (4K/32K/64K -Byte)
  - Program 1 to 256 bytes per programable page

  - Erase/Program Suspend & Resume
- Advanced Security Features
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for eatch device
  - 4X 256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- Space Efficient Packaging
  - 8-pin SOIC/VSOP 208-mil
  - 8-pad WSON 6x5-mm/ 8x6-mm
  - 16pin SOIC 300mil (additional/RESET pin)
  - 24-ball TFBGA 8x6mm
  - Contact Winbond for KGD and other options

C. Function Block



II. LIFE TEST

A. Introduction

1. High-Temperature Operating Life Test (HTOL)

1.1 SCOPE

HTOL test is performed to accelerate failure mechanisms which are thermally activated. This can be achieved by stressing the devices with bias at high temperature.

1.2 TEST CONDITION

Temp ambient = 125°C, Vdd = 1.95V, dynamic stressing, Td = 1000 hrs. (JESD22-A108)

2. Data Retention Test (DR)

2.1 SCOPE

DR test is to determine the stability of data stored in the device under high temperature environment.

2.2 TEST CONDITION

Temp = 150°C, Td = 1000 hrs. (JESD22-A117)

3. Non-Volatile Memory Cycling Endurance (NVCE)

3.1 SCOPE

Test product's capability to the number of Program and Erase.

3.2 TEST CONDITION

JEDEC-STD-JESD 47

Room Temp cycling test:

TD (Duration) = 1K, 10K, 100K cycles on 100:10:1 memory size.

Vcc = 1.95V

Pattern = 00, FF, CHKBD, CHKBD\

Low temp data retention (LTDR):

Dynamic operation life test at room temp.

TD (Duration) = 500 hrs

Vcc = 1.95V

Apply dynamic pattern.

85℃ cycling test:

TD (Duration) = 1K, 10K, 100K cycles on 100:10:1 memory size.

Vcc = 1.95V

Pattern = 00, FF, CHKBD, CHKBD\

High temp data retention (HTDR):

Bake at 125°C

TD (Duration) = 10 hrs for 100K cycling,

100 hrs for 10K and 1K cycling.

B. Test Results

1. High-Temperature Operating Life Test (HTOL)

1.1 SUMMARY TABLE

RUN	Lot No	500 Hrs	1000 Hrs	Remark
#1	6217AJ700	0/77	0/77	
#2	6217AC000	0/77	0/77	
#3	6217AL9AZ	0/77	0/77	

*Criteria : Acc/Rej = 0/1

1.2 FAILURE RATE CALCULATION

$$F.R.(T) = \frac{X^2(1-CL, 2N+2)}{2EDH}$$

WHERE X^2: CHI-SQUARE Function CL: Confidence Level

N : No of Failures EDH: Equivalent Device Hour

Test Item	Dev. Hours at Tj=125.6°C	Equiv. Dev. Hours at Tj=55°C	No. of Failure	Failure Rate at 55°C
HTOL	231000	227695602	0	4.02 FIT

Based on CL = 60% and Activation Energy = 1.1 eV

$Tj = Ta + Pd \bullet \theta ja$

Where: Tj= junction temp, Ta=125℃ (ambient temp)

Pd=8.19mW (power dissipated on the device)

Θja=77.8℃/W (thermal resistance from junction to ambient)

2. Data Retention Test (DR)

RUN	Lot No	500 Hrs	1000 Hrs	Remark
#1	6217AJ700	0/77	0/77	
#2	6217AC000	0/77	0/77	
#3	6217AL9AZ	0/77	0/77	

*Criteria : Acc/Rej = 0/1.

3. Non-Volatile Memory Cycling Endurance (NVCE)

3.1 Room temp 1k~100k cycling with Data Retention

RUN	Lot No	RT cycling: 1K~100K	LTDR-500 HRs	Remark
#1	6217AJ700	0/38	0/38	
#2	6217AC000	0/38	0/38	
#3	6217AL9AZ	0/38	0/38	

*Criteria: Acc/Rej = 0/1.

3.2 85℃ 1k~100k cycling with Data Retention

RUN	Lot No	85°C cycling: 1K~100K	HTDR-10 HRs	HTDR-100 HRs	Remark
#1	6217AJ700	0/39	0/39	0/39	
#2	6217AC000	0/39	0/39	0/39	
#3	6217AL9AZ	0/39	0/39	0/39	

*Criteria: Acc/Rej = 0/1.

III. ENVIRONMENTAL TESTS

A. Introduction

1. Pre-condition Test

1.1 SCOPE

Pre-condition Test is to measure the resistance of SMD (Surface Mount Devices) to the storage environment at the customer site and to thermal stress created by IR reflow.

1.2 TEST CONDITION

Step 1: TCT (-65°C/150°C, 5 cycles)

Step 2: Bake (125°C, 20 hours)

Step 3: Soak (30°C/60%RH, 192 hours)

Step 4: IR, 3 passes (JEDEC 020 D).

2. High Temperature Storage Life Test (HTSL)

2.1 SCOPE

HTSL test is to determine the stability of the device in high temperature environment.

2.2 TEST CONDITION

Temp = 150°C, Td = 1000 hrs. (JESD22-A103)

3. Pressure Cooker Test (PCT)

3.1 SCOPE

PCT is to evaluate the device resistance to moisture penetration.

3.2 TEST CONDITION

Ta = 121°C, RH = 100%, P = 2 atm, Td = 168 Hrs. (JESD22-A102-A)

4. Highly Accelerated Stress Testing (HAST)

4.1 SCOPE

HAST is to evaluate the reliability of non hermetic packaged solid-state device in humid environments.

4.2 TEST CONDITION

Ta = 130°C, Vdd=1.95V, RH% = 85%, P = 2 atm, Td = 168 Hrs.
(JESD22-A110)

5. Temperature Cycle Test (TCT)

5.1 SCOPE

TCT is to evaluate the resistance of device to environmental temperature change.

5.2 TEST CONDITION

-65°C / 15min, transfer time 1min, +150 °C/15min, 500 cycles.
(JESD22-A104)

B. Test Result

1. Pre-condition Test

Run	Lot No	Result	Remark
#1	6217AJ700	0/308	
#2	6217AC000	0/308	
#3	6217AL9AZ	0/308	

*Criteria : Acc/Rej = 0/1.

2. High Temperature Storage Life Test (HTSL)

RUN	Lot No	500 Hrs	1000 Hrs	Remark
#1	6217AJ700	0/77	0/77	
#2	6217AC000	0/77	0/77	
#3	6217AL9AZ	0/77	0/77	

*Criteria : Acc/Rej = 0/1

3. Pressure Cooker Test (PCT)

Run	Lot No	168 Hrs	Remark
#1	6217AJ700	0/77	
#2	6217AC000	0/77	
#3	6217AL9AZ	0/77	

*Criteria : Acc/Rej = 0/1.

4. Highly Accelerated Stress Testing (HAST)

Run	Lot No	168 Hrs	Remark
#1	6217AJ700	0/77	
#2	6217AC000	0/77	
#3	6217AL9AZ	0/77	

*Criteria : Acc/Rej = 0/1.

5. Temperature Cycle Test (TCT)

Run	Lot No	500 Cycles	Remark
#1	6217AJ700	0/77	
#2	6217AC000	0/77	
#3	6217AL9AZ	0/77	

*Criteria : Acc/Rej = 0/1.

IV. ESD AND LATCH-UP

A. Introduction

1. ESD

1.1 SCOPE

ESD test is to evaluate the immunity of device to electrostatic discharge.

1.2 TEST CONDITION

Human Body Model (HBM): JESD22-A114C.01
Machine Model (MM): EIA/JESD22-A115-A.
Charge Device Model (CDM): JESD22-C101-C.

2. Latch-Up

2.1 SCOPE

Latch-Up test is to evaluate the immunity of the devices to latch-up.

2.2 TEST CONDITION

JEDEC STD 78, Temp = 25 °C, VDD = Max. Operating Voltage

B. Test Results

1. ESD

1.1 Human Body Model

Run	LOT#	POSITIVE	NEGATIVE	Remark
#1	6217AJ700	0/6	0/6	
#2	6217AC000	0/6	0/6	
#3	6217AL9AZ	0/6	0/6	

*Criteria : Acc/Rej = 0/1.

*| SPEC | : >2KV

1.2. Machine Model

Run	LOT#	POSITIVE	NEGATIVE	Remark
#1	6217AJ700	0/6	0/6	
#2	6217AC000	0/6	0/6	
#3	6217AL9AZ	0/6	0/6	

*Criteria : Acc/Rej = 0/1.

*| SPEC | : >200 V

1.3. Charge Device Model

Run	LOT#	POSITIVE / NEGATIVE	Remark
#1	6217AJ700	0/3	
#2	6217AC000	0/3	
#3	6217AL9AZ	0/3	

*Criteria : Acc/Rej = 0/1.

*| SPEC | : >750V

2. Latch-Up

Run	LOT#	POSITIVE	NEGATIVE	Remark
#1	6217AJ700	0/3	0/3	
#2	6217AC000	0/3	0/3	
#3	6217AL9AZ	0/3	0/3	

*Criteria : Acc/Rej = 0/1.

*| SPEC. | : I-Test > 200mA

Vsupply over voltage Test>1.5x max supply voltage

Headquarters Taiwan

Winbond Electronics Corp.

No. 8, Keya Rd. I, Central Taiwan Science Park,
Taichung County, 428, Taiwan, R.O.C.
Tel: 886-4-25218168

USA

Winbond Electronics Corporation America

2727 N. First Street,
San Jose, CA 95134, U.S.A.
Tel: 408-943-6666

Hong Kong

Winbond Electronics (H.K.) Ltd.

Unit 9-11, 22/F, Millennium City 2,
378 Kwun Tong Road, Kowloon,
Hong Kong, P.R. China
Tel: 852-27513126

Japan

Winbond Electronics Corporation Japan

NO.2 Ueno-Bldg.,7-18,3-chome,
Shinyokohama Kohoku-ku,
Yokohama, 222-0033, Japan
Tel: 81-45-478-1881

Winbond Electronics Corporation
No.539, Sec.2 Wenxing Rd.
Jhubei City, Hsinchu, Taiwan, R.O.C.

Product Obsolescence Notice

W25Q64DW SpiFlash Memories

Notification Date: December 14, 2012

Dear Valued Customer,

This letter is to notification of Winbond's intention to terminate production of the W25Q64DW SpiFlash memory and replace it with the W25Q64FW. Current part numbers affected and corresponding replacement part numbers are listed below. Availability of W25Q64DW Automotive Grade products are not affected by this notice.

Winbond Current PN (90nm D-Series)	Winbond Primary Replacement PN (58nm F-Series)
W25Q64DWSSIG	W25Q64FWSSIG
W25Q64DWSFIG	W25Q64FWSFIG
W25Q64DWSTIG	W25Q64FWSTIG
W25Q64DWSTIM	W25Q64FWSTIM
W25Q64DWZPIG	W25Q64FWZPIG
W25Q64DWZEIG	W25Q64FWZEIG
W25Q64DWWC	W25Q64FWWC

W25Q64FW Features
a) Advanced 58nm SpiFlash Technology
b) Command compatible with W25Q64DW (same JEDEC Device ID, Superset Instruction Set)
c) Individual Block Write Protection in addition to the existing protection schemes
d) Additional configurable hardware /RESET pin
e) Programmable Output Driver Strength

W25Q64FW Benefits
a) 58nm Technology allows for improved availability and best possible future pricing
b) Faster Read performance

Please refer to the table below for the product last time order date and Winbond last shipment date. Winbond Electronics reserves the right to limit last time buy □uantities based on capacity and material availability. Please notify Winbond as soon as possible if there are any concerns with this schedule.

90nm Part Number	Notification Date	90nm □ast Order Date	90nm □ast Ship Date	58nm Part Number	58nm Reliability Report	58nm Mass Production
W25Q64DW	Dec. 14th 2012	June 14th 2013	Dec. 14th 2013	W25Q64FW	Dec. 5th 2012	Dec. 5th 2012

Robin Jigour

Vice President of Flash Marketing