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## SOT23-5 and 4-pin QFN Co-layout Designs For SiTime MHz Devices

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### 1 Introduction

SiTime offers a family of single-chip, one-output clock generators with embedded MEMS resonators that eliminate the need for external crystals (XTAL) or other clock references. These clock generators have the same electrical specifications and features as SiTime's 4-pin oscillators, but come in a small SOT23-5 (5-pin, 2.9 x 2.8 x 1.27 mm) package (refer to Figure 1).

The SOT23-5 package is a commonly used semiconductor package that provides several benefits compared to the standard 4-pin oscillator SMD packages:

- Most cost effective
- Lower test cost through use of an optical scope for solder joint inspection
- Better board level solder joint reliability
- Easier re-work capability (typical of any leaded package)



Figure 1: 3-D view of SOT23-5 package

This document provides layout guidelines that enable system designers to support both SOT23-5 and standard oscillator footprints on the same PCB board, therefore ensuring maximum flexibility in sourcing these types of clock components.

Refer to Section 5 for a high-level spec summary of the one-output clock generator family and their 4-pin oscillator counterparts.

**Note that SiTime also offers a family of 32 kHz oscillators in 2012, CSP and SOT23 packages. This appnote does not apply to the 32 kHz family.**

### 2 SOT23-5 and 4-pin SMD Oscillator Co-layout Methodology

There are two general approaches to design co-layout for SOT23-5 and 4-pin oscillator SMD package, the co-planar design and the stacked design.

In the co-planar design, the SOT23-5 and the SMD land patterns are placed side by side on the same PCB layer. This is the simpler approach, but this layout requires more PCB area than the stacked design. The stacked design reduces area usage by placing the SOT-23 and the SMD land patterns opposite to each other, symmetrically, with one pattern on top layer and the other pattern on the bottom layer.

Sections 3 and 4 provide details of both methodology, along with co-layout guidelines for SOT23-5 and five standard QFN oscillator packages available from SiTime (2.0 x 1.6 mm, 2.5 x 2.0 mm, 3.2 x 2.5 mm, 5.0 x 3.2 mm, 7.0 x 5.0 mm). The same guidelines are applicable to quartz-based oscillators as long as the land patterns for these oscillators are compatible to the SiTime oscillator land patterns.

### 3 Co-planar Designs

This section shows examples of co-planar designs. The main advantage of this approach is the ability to place SiTime parts in either the SOT23-5 package or one of the QFN package types on the same layer without additional via for the output pin.

#### 3.1 QFN 2016 and SOT23-5 Co-planar Design

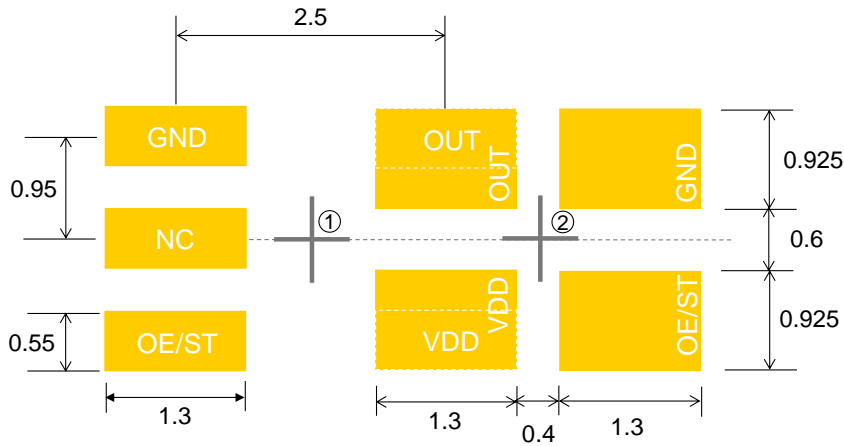


Figure 2: QFN 2016 and SOT23-5 co-planar design land pattern

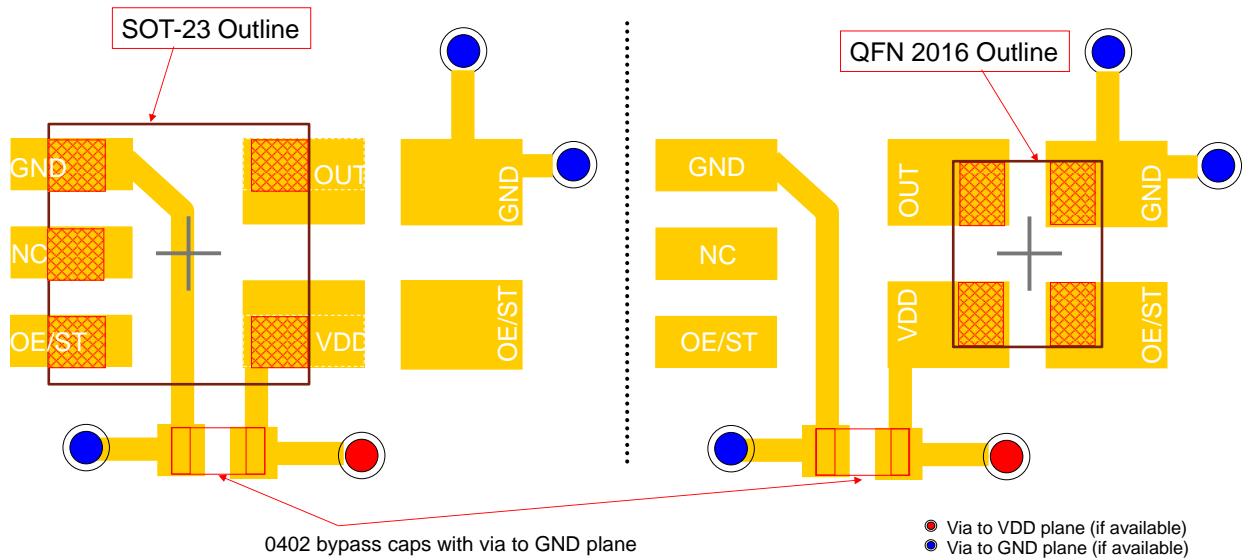


Figure 3: QFN 2016 and SOT23-5 co-planar design layout example showing placement of both QFN 2016 and SOT23-5 devices

## 3.2 QFN 2520 and SOT23-5 Co-planar Design

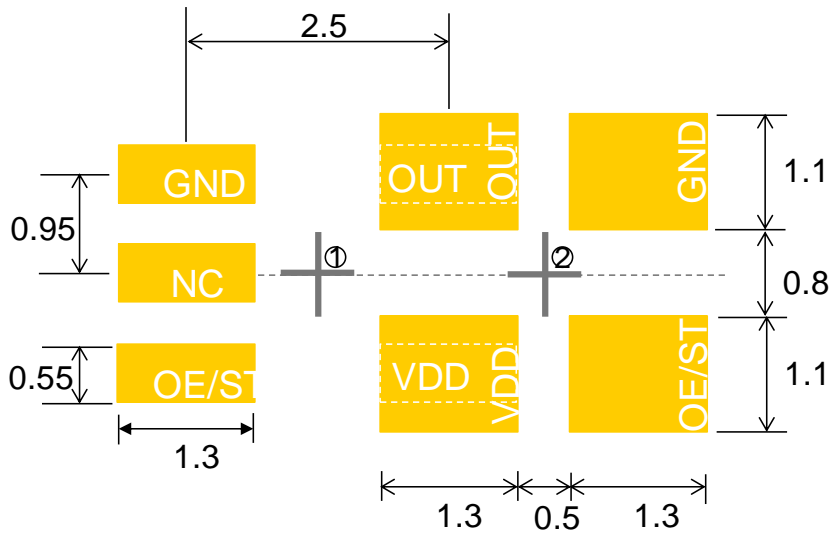


Figure 4: QFN 2520 and SOT23-5 co-planar design land pattern

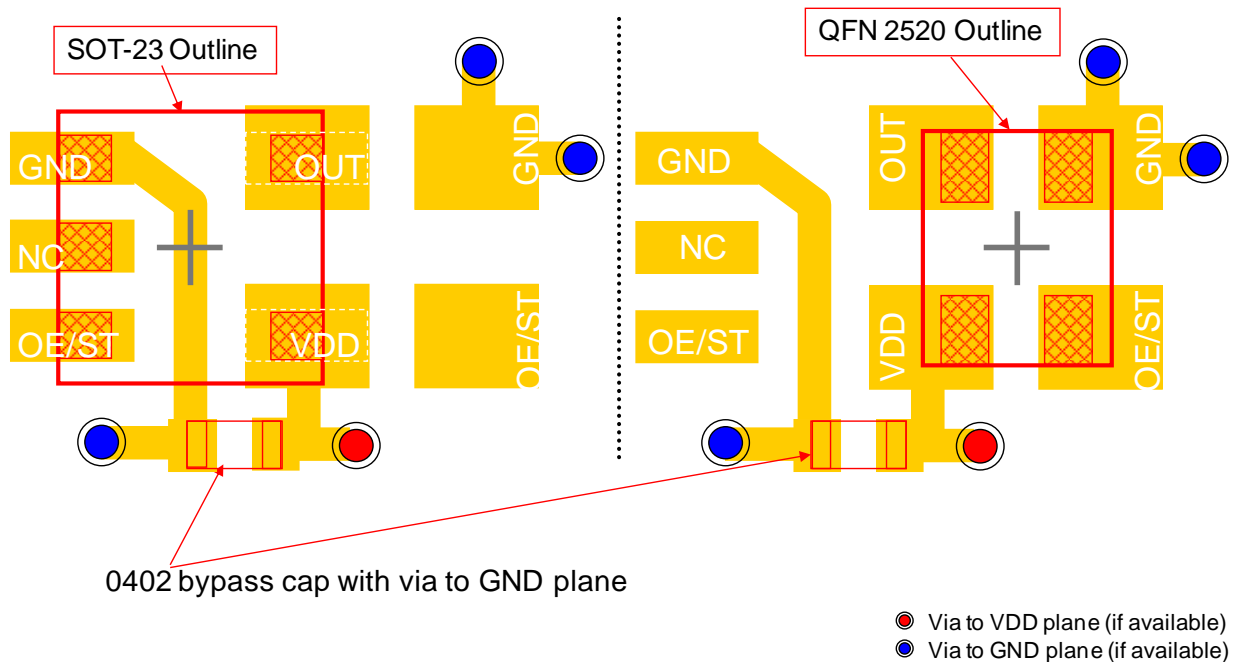


Figure 5: QFN 2520 and SOT23-5 co-planar design layout example showing placement of both QFN 2520 and SOT23-5 devices

### 3.3 QFN 3225 and SOT23-5 Co-planar Design

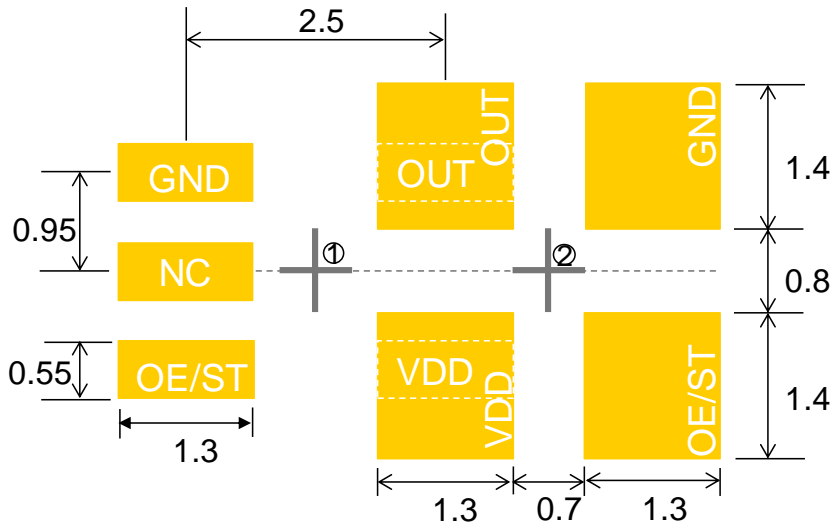


Figure 6: QFN 3225 and SOT23-5 co-planar design land pattern

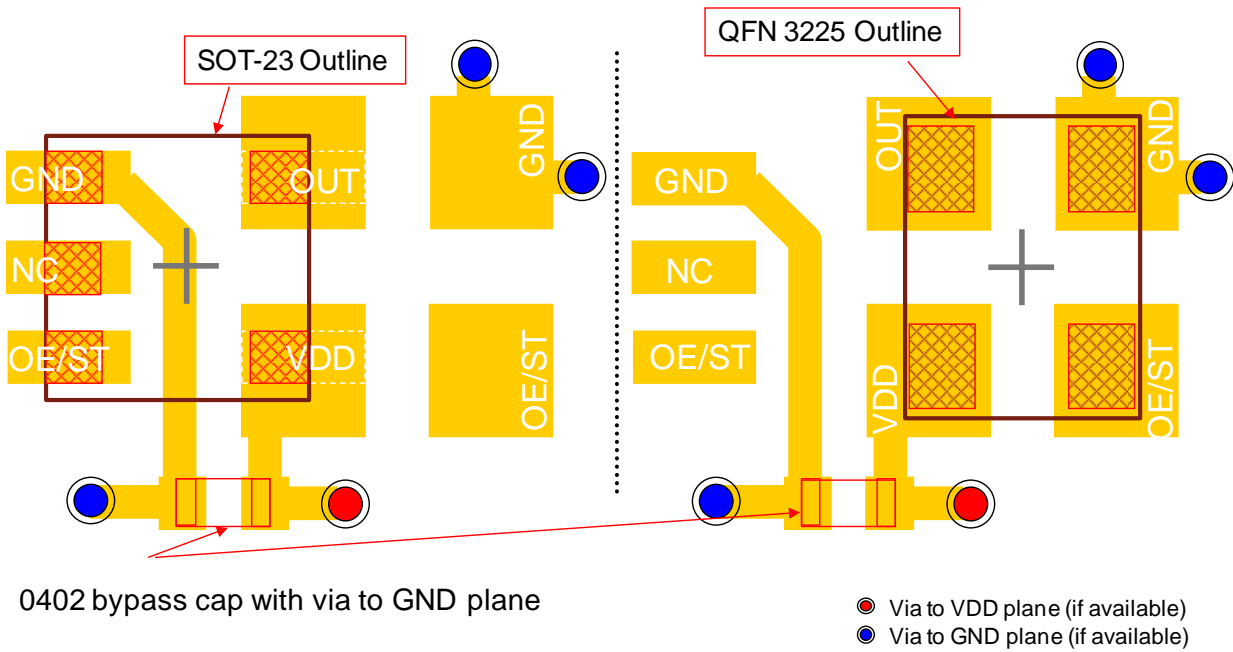


Figure 7: QFN 3225 and SOT23-5 co-planar design layout example showing placement of both QFN 3225 and SOT23-5 devices

## 3.4 QFN 5032 and SOT23-5 Co-planar Design

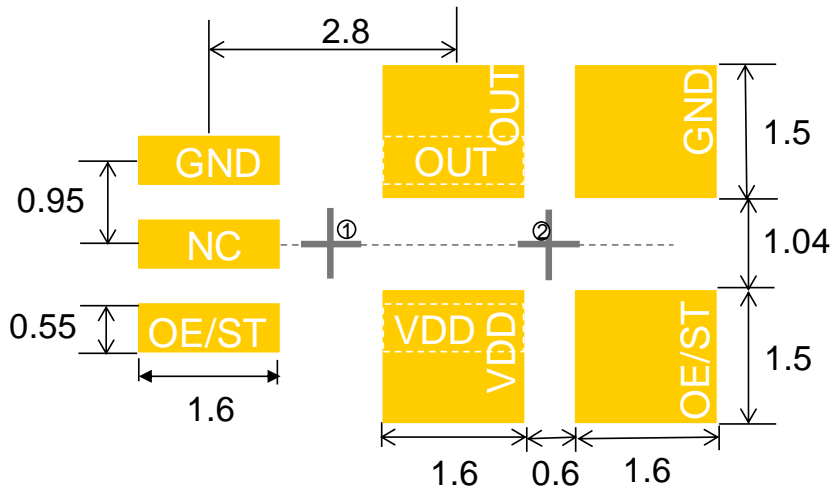


Figure 8: QFN 5032 and SOT23-5 co-planar design land pattern

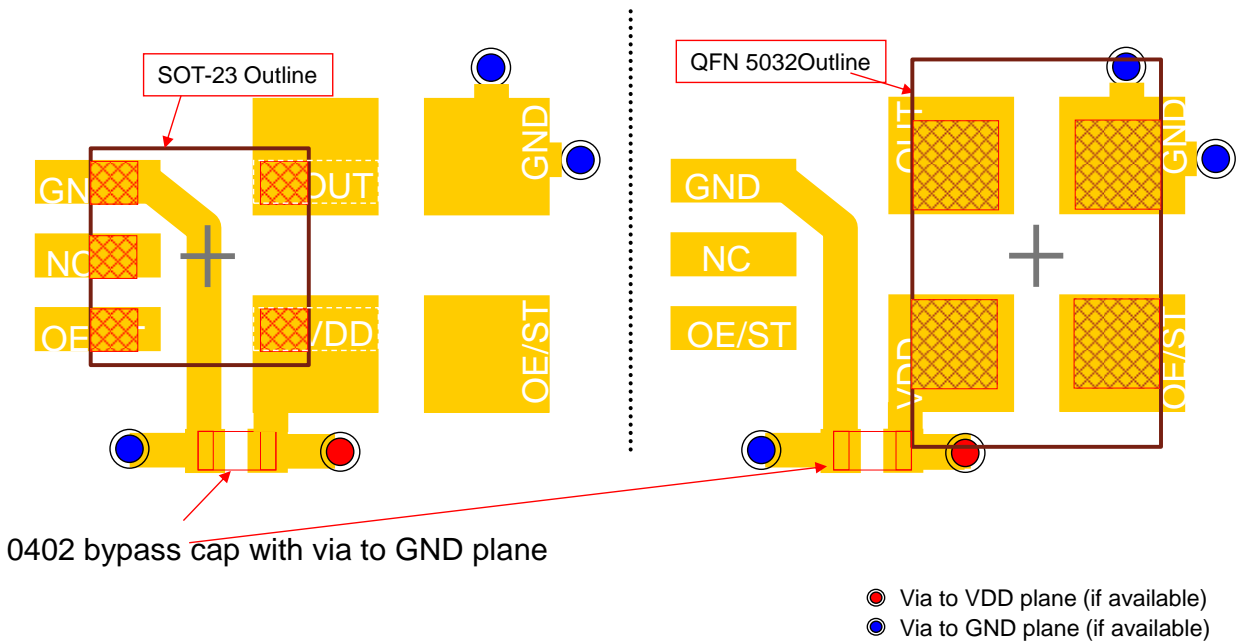


Figure 9: QFN 5032 and SOT23-5 co-planar design layout example showing placement of both QFN 5032 and SOT23-5 devices

## 3.5 QFN 7050 and SOT23-5 Co-planar Design

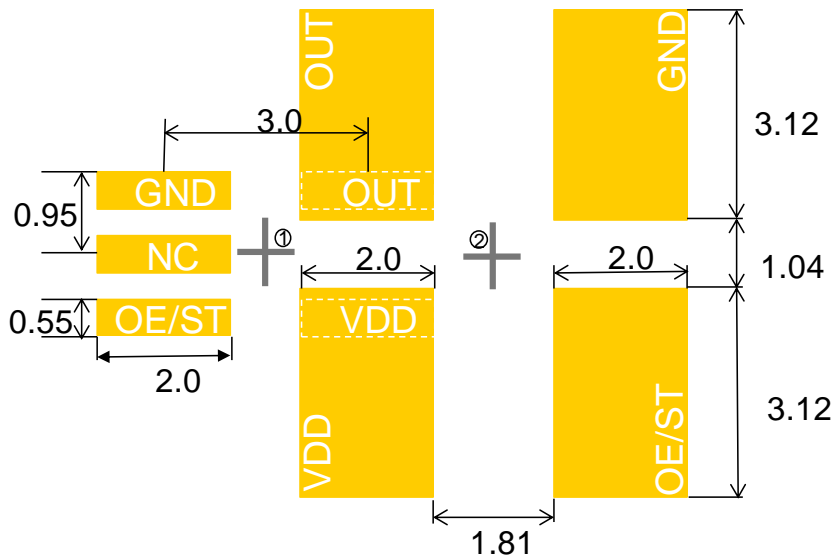


Figure 10: QFN 7050 and SOT23-5 co-planar design land pattern

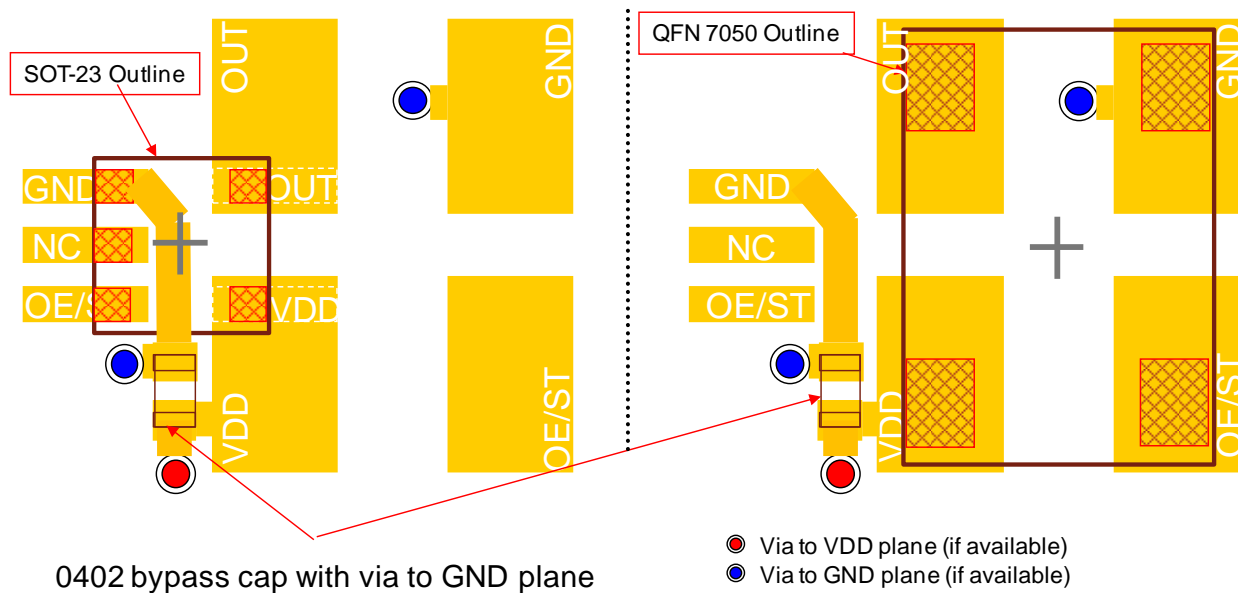


Figure 11: QFN 7050 and SOT23-5 co-planar design layout example showing placement of both QFN 7050 and SOT23-5 devices

## 4 Stacked Designs

This section shows examples of stacked designs. This approach lends itself to a more compact layout but it requires additional via for connecting the pads of the output clock pins. The center of the footprints on the top and bottom layers should be aligned in stacked designs.

### 4.1 QFN 2016 and SOT23-5 Stacked Design

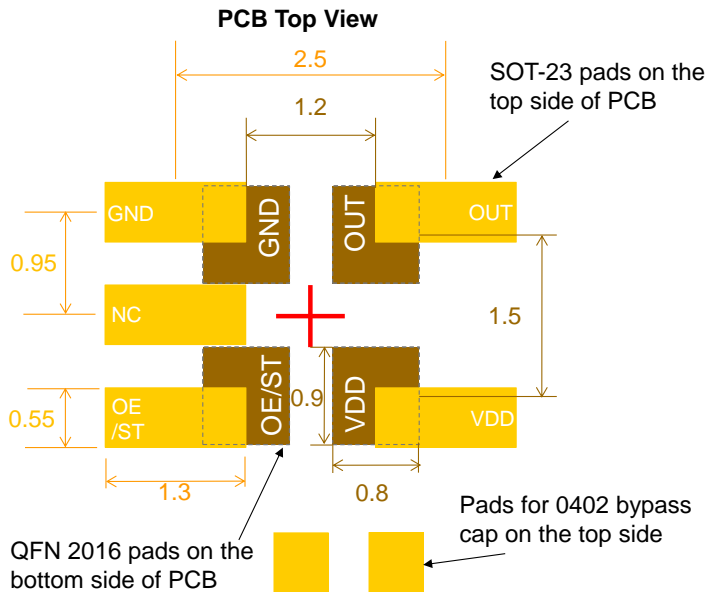


Figure 12: QFN 2016 and SOT23-5 stacked design land pattern

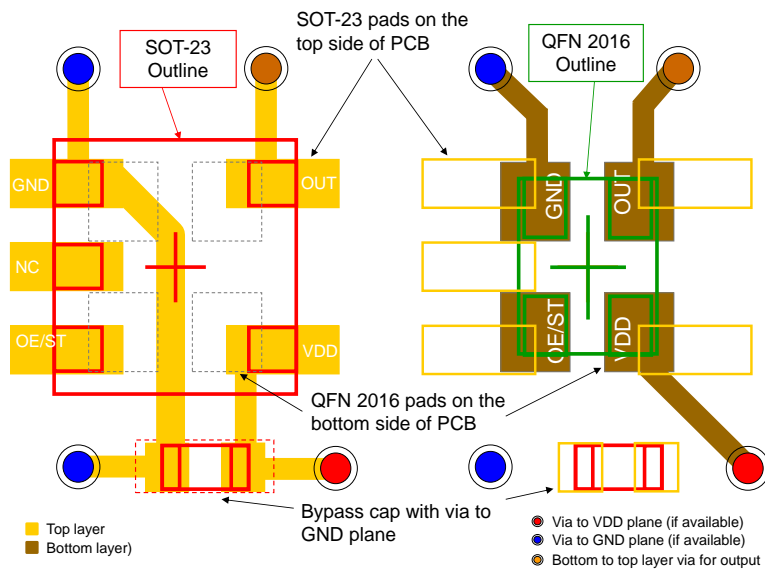
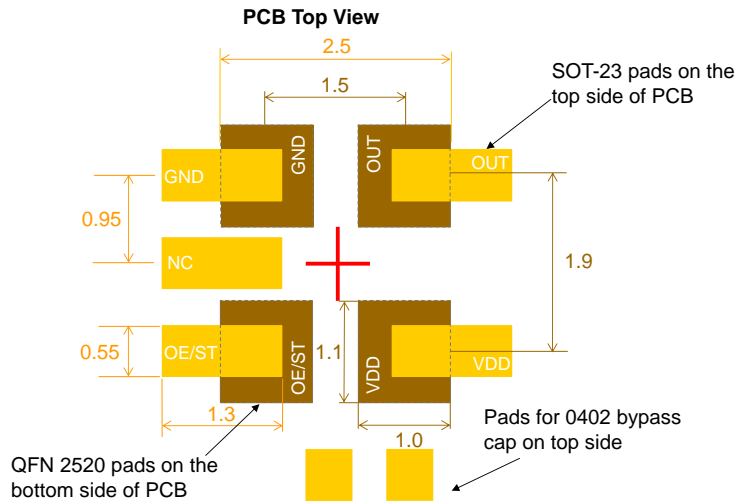


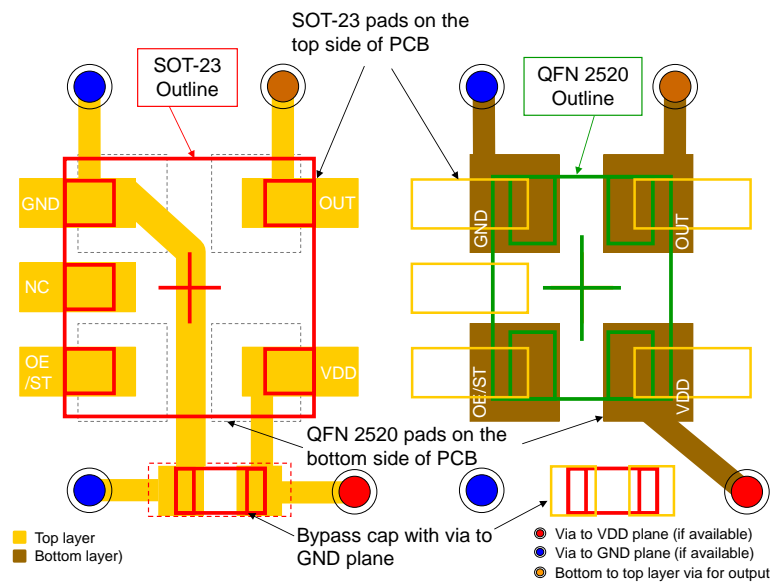
Figure 13: QFN 2016 and SOT23-5 stacked design layout example showing placement of both QFN 2016 and SOT23-5 devices



## 4.2 QFN 2520 and SOT23-5 Stacked Design



**Figure 14: QFN 2520 and SOT23-5 stacked design land pattern**



**Figure 15: QFN 2520 and SOT23-5 stacked design layout example showing placement of both QFN 2520 and SOT23-5 devices**

## 4.3 QFN 3225 and SOT23-5 Stacked Design

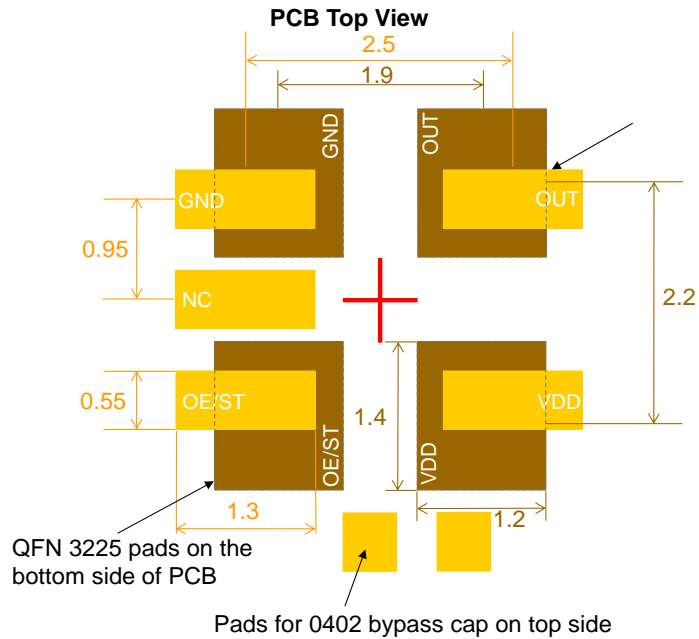


Figure 16: QFN 3225 and SOT23-5 stacked design land pattern

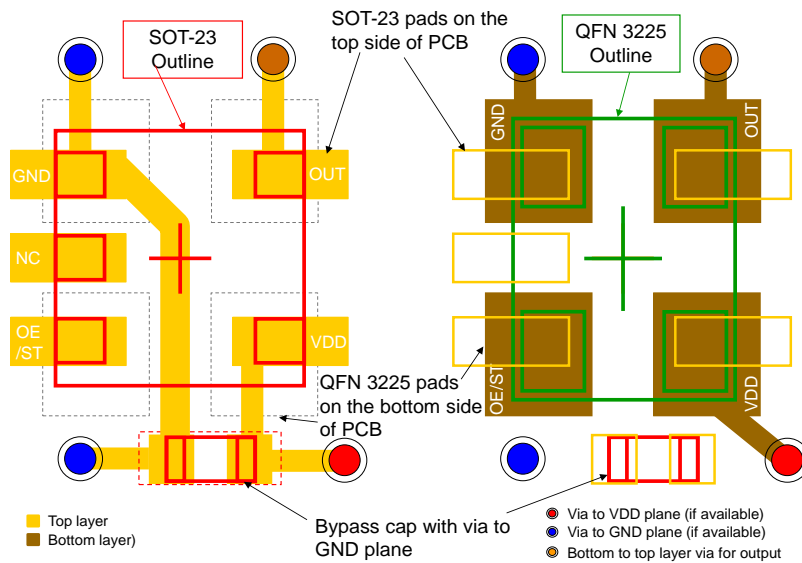


Figure 17: QFN 3225 and SOT23-5 stacked design layout example showing placement of both QFN 3225 and SOT23-5 devices

## 4.4 QFN 5032 and SOT23-5 Stacked Design

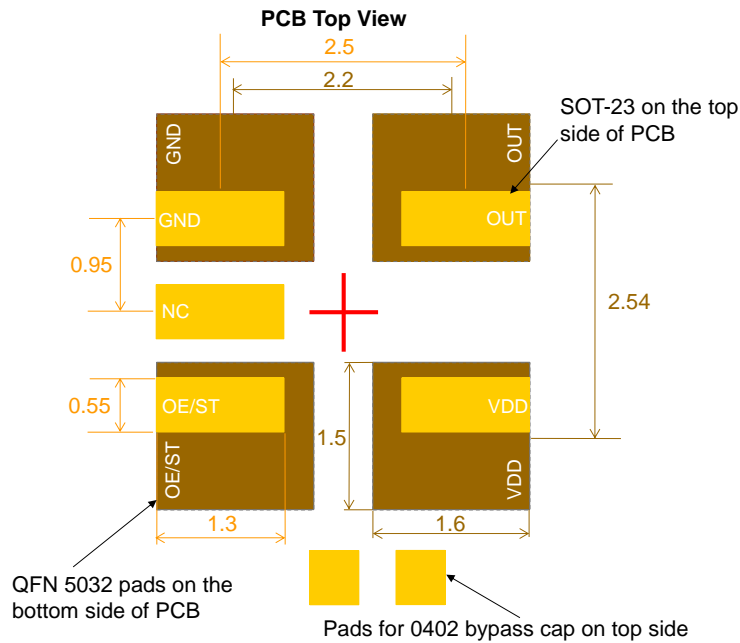


Figure 18: QFN 5032 and SOT23-5 stacked design land pattern

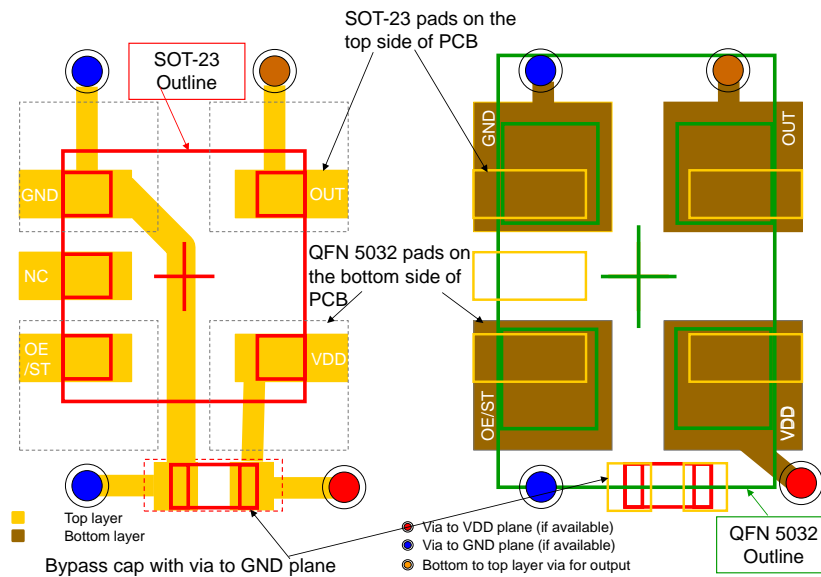


Figure 19: QFN 5032 and SOT23-5 stacked design layout example showing placement of both QFN 5032 and SOT23-5 devices

## 4.5 QFN 7050 and SOT23-5 Stacked Design

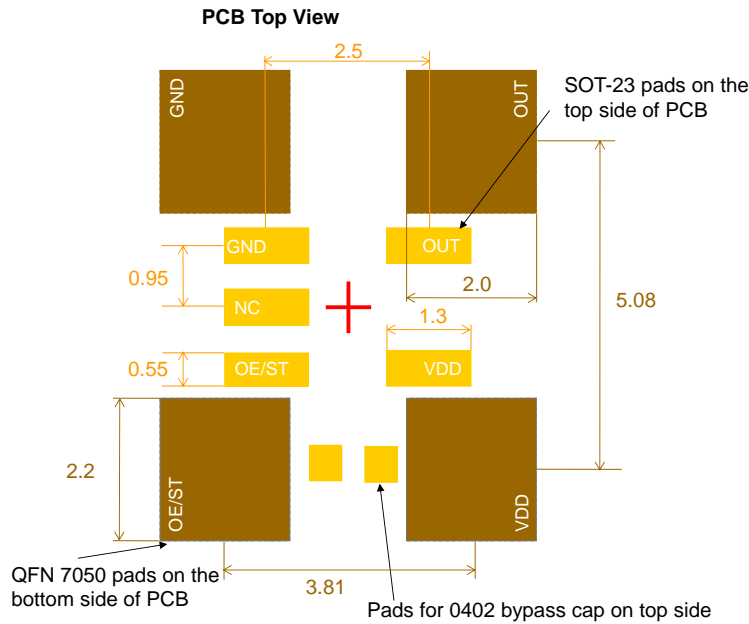


Figure 20: QFN 7050 and SOT23-5 stacked design land pattern

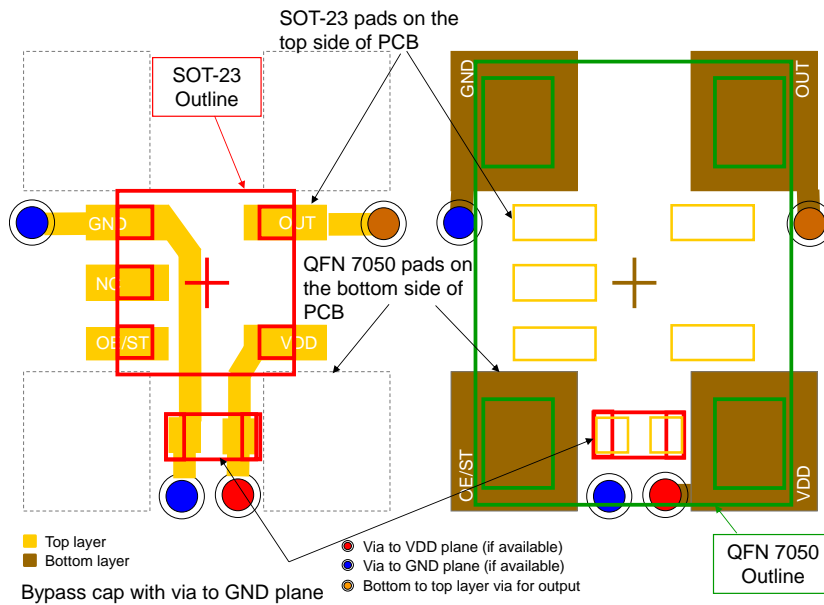


Figure 21: QFN 7050 and SOT23-5 stacked design layout example showing placement of both QFN 7050 and SOT23-5 devices

## 5 One-output Clock Generators vs. Standard Package Oscillators

The table below summarizes key specs of these devices along with their 4-pin oscillator counterparts. Detailed product information including datasheets can be found at: [www.sitime.com/products/clock-generators](http://www.sitime.com/products/clock-generators).

Clock Generator (SOT23-5)	Matching Oscillator (4-pin SMD)	AEC-Q100	Frequency (MHz)	Frequency Stability (PPM)	Temp Range (°C)	Supply Voltage (V)
<a href="#">SiT9201</a>	<a href="#">SiT8008</a>	-	1 to 110	±20 ±25 ±50	-20 to 70 -40 to 85	1.8V 2.5 to 3.3V
<a href="#">SiT2002</a>	<a href="#">SiT8009</a>	-	115 to 137			
<a href="#">SiT2018</a>	<a href="#">SiT8918</a>	-	1 to 110	±20 ±25 ±30 ±50	-40 to 105 -40 to 125	
<a href="#">SiT2019</a>	<a href="#">SiT8919</a>	-	115.194001 to 137			
<a href="#">SiT2020</a>	<a href="#">SiT8920</a>	-	1 to 110			
<a href="#">SiT2021</a>	<a href="#">SiT8921</a>	-	119.342001 to 137		-55 to 125	
<a href="#">SiT2024</a>	<a href="#">SiT8924</a>	Yes	1 to 110		-40 to 105 -40 to 125	
<a href="#">SiT2025</a>	<a href="#">SiT8925</a>	Yes	115.194001 to 137	-55 to 125		

## 6 Conclusion

This application note presents the co-planar and stacked co-layout designs for SiTime SOT23-5 and 4-pin QFN packages. Use of these co-layout designs enables customers to adopt the lowest cost SOT23-5 parts while maintaining flexibility to use QFN parts from multiple sources without redesigning the board.

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