**10 MHz, 4-Quadrant Multiplier/Divider**

**AD734**

**FEATURES**
- High Accuracy
  - 0.1% Typical Error
- High Speed
  - 10 MHz Full-Power Bandwidth
  - 450 V/µs Slew Rate
  - 200 ns Settling to 0.1% at Full Power
- Low Distortion
  - –80 dBc from Any Input
  - Third-Order IMD Typically –75 dBc at 10 MHz
- Low Noise
  - 94 dB SNR, 10 Hz to 20 kHz
  - 70 dB SNR, 10 Hz to 10 MHz
- Direct Division Mode
  - 2 MHz BW at Gain of 100

**APPLICATIONS**
- High Performance Replacement for AD534
  - Multiply, Divide, Square, Square Root
  - Modulator, Demodulator
  - Wideband Gain Control, RMS-DC Conversion
  - Voltage-Controlled Amplifiers, Oscillators, and Filters
  - Demodulator with 40 MHz Input Bandwidth

**PRODUCT DESCRIPTION**
The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function \( W = XY/U \). The AD734 provides a low-impedance voltage output with a full-power (20 V pk-pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of full scale. Distortion is typically less than –80 dBc and guaranteed. The low capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734’s input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of –40°C to +85°C and come in a 14-lead ceramic DIP. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of –55°C to +125°C, is available in a 14-lead ceramic DIP.

**PRODUCT HIGHLIGHTS**
The AD734 embodies more than two decades of experience in the design and manufacture of analog multipliers, to provide:
1. A new output amplifier design with more than twenty times the slew-rate of the AD534 (450 V/µs versus 20 V/µs) for a full power (20 V pk-pk) bandwidth of 10 MHz.
2. Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
3. Direct control of the denominator, resulting in higher multiplier accuracy and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD534 in divider modes.
4. Very clean transient response, achieved through the use of a novel input stage design and wide-band output amplifier, which also ensure that distortion remains low even at high frequencies.
5. Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 88 dB of dynamic range in a 20 kHz bandwidth.
AD734—SPECIFICATIONS

\[ W = A_0 \left\{ \frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} - (Z_1 - Z_2) \right\} \]

### TRANSFER FUNCTION

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<td>( W = XY/10 )</td>
<td>( W = XY/10 )</td>
<td>%</td>
</tr>
<tr>
<td>Total Static Error(^1)</td>
<td>(-10 \leq X, Y \leq 10 ) V</td>
<td>0.1</td>
<td>0.4</td>
<td>0.1</td>
<td>0.4</td>
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<tr>
<td>Over ( T_{MIN} ) to ( T_{MAX} ) vs. Temperature</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>0.004</td>
<td>0.003</td>
<td>0.004</td>
<td>%/(^\circ)C</td>
</tr>
<tr>
<td>vs. Either Supply</td>
<td>( \pm 7 \leq X \leq +10 ) V, ( Y = +10 ) V</td>
<td>0.01</td>
<td>0.05</td>
<td>0.01</td>
<td>0.05</td>
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<tr>
<td>Peak Nonlinearity</td>
<td>(-10 \leq Y \leq +10 ) V, ( X = +10 ) V</td>
<td>0.05</td>
<td>0.05</td>
<td>0.05</td>
<td>%</td>
</tr>
<tr>
<td>THD(^2)</td>
<td>( X = 7 ) V rms, ( Y = +10 ) V, f = 5 kHz</td>
<td>–58</td>
<td>–66</td>
<td>–58</td>
<td>( \text{dBc} )</td>
</tr>
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<td></td>
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<td>–55</td>
<td>–63</td>
<td>–55</td>
<td>( \text{dBc} )</td>
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<tr>
<td></td>
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<td>–60</td>
<td>–80</td>
<td>–60</td>
<td>( \text{dBc} )</td>
</tr>
<tr>
<td>Feedthrough</td>
<td>( X = 7 ) V rms, ( Y = ) nulled, f = 5 kHz</td>
<td>–85</td>
<td>–98</td>
<td>–85</td>
<td>–98</td>
</tr>
<tr>
<td></td>
<td>( Y = 7 ) V rms, ( X = ) nulled, f = 5 kHz</td>
<td>–85</td>
<td>–98</td>
<td>–85</td>
<td>–98</td>
</tr>
<tr>
<td>Noise (RTO)</td>
<td>( X = Y = 0 )</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>( \mu \text{V/( \sqrt{\text{Hz}} )} )</td>
</tr>
<tr>
<td>Total Output Noise</td>
<td>10 Hz to 20 kHz</td>
<td>–94</td>
<td>–88</td>
<td>–94</td>
<td>–88</td>
</tr>
<tr>
<td><strong>DIVIDER PERFORMANCE</strong> (( Y = 10 ) V)</td>
<td>Transfer Function</td>
<td>( W = XY/U )</td>
<td>( W = XY/U )</td>
<td>( W = XY/U )</td>
<td>%</td>
</tr>
<tr>
<td>Gain Error</td>
<td>( Y = 10 ) V, ( U = 100 ) mV to 10 V</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>X Input Clipping Level</td>
<td>( Y \leq 10 ) V</td>
<td>1.25 × ( U )</td>
<td>1.25 × ( U )</td>
<td>1.25 × ( U )</td>
<td>V</td>
</tr>
<tr>
<td>U Input Scaling Error(^3)</td>
<td>( U = 1 ) V to 10 V Step, ( X = 1 ) V</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>ns</td>
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<tr>
<td>(Output to 1%)</td>
<td>( U = 1 ) V to 10 V Step, ( X = 1 ) V</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td><strong>INPUT INTERFACES (X, Y, &amp; Z)</strong></td>
<td>3 dB Bandwidth</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>MHz</td>
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<tr>
<td>Operating Range</td>
<td>Differential or Common Mode</td>
<td>( \pm 12.5 )</td>
<td>( \pm 12.5 )</td>
<td>( \pm 12.5 )</td>
<td>V</td>
</tr>
<tr>
<td>X Input Offset Voltage</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>15</td>
<td>5</td>
<td>15</td>
<td>mV</td>
</tr>
<tr>
<td>Y Input Offset Voltage</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>10</td>
<td>5</td>
<td>10</td>
<td>mV</td>
</tr>
<tr>
<td>Z Input Offset Voltage</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>Z Input PSRR (Either Supply)</td>
<td>f = 1 kHz</td>
<td>54</td>
<td>70</td>
<td>54</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>dB</td>
</tr>
<tr>
<td>CMRR</td>
<td>f = 5 kHz</td>
<td>70</td>
<td>85</td>
<td>70</td>
<td>85</td>
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<tr>
<td>Input Bias Current (X, Y, Z Inputs)</td>
<td>50</td>
<td>300</td>
<td>50</td>
<td>300</td>
<td>50</td>
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<tr>
<td>Input Resistance</td>
<td>Differential</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>k\Omega</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Differential</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>pF</td>
</tr>
<tr>
<td><strong>DENOMINATOR INTERFACES (U0, U1, &amp; U2)</strong></td>
<td>Operating Range</td>
<td>VN to VP-3</td>
<td>VN to VP-3</td>
<td>VN to VP-3</td>
<td>V</td>
</tr>
<tr>
<td>Denominator Range</td>
<td>1000:1</td>
<td>1000:1</td>
<td>1000:1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface Resistor</td>
<td>U1 to U2</td>
<td>28</td>
<td>28</td>
<td>28</td>
<td>k\Omega</td>
</tr>
<tr>
<td><strong>OUTPUT AMPLIFIER (W)</strong></td>
<td>Output Voltage Swing</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>( \pm 12 )</td>
<td>( \pm 12 )</td>
<td>( \pm 12 )</td>
</tr>
<tr>
<td>Open-Loop Voltage Gain</td>
<td>( X = 0 ), Input to Z</td>
<td>72</td>
<td>72</td>
<td>72</td>
<td>dB</td>
</tr>
<tr>
<td>Dynamic Response</td>
<td>From X or Y Input, CL ( \leq 20 ) pF</td>
<td>8</td>
<td>10</td>
<td>8</td>
<td>10</td>
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<tr>
<td>W = 7 V rms</td>
<td></td>
<td>450</td>
<td>450</td>
<td>450</td>
<td>V/( \mu \text{s} )</td>
</tr>
<tr>
<td>Slew Rate</td>
<td></td>
<td>125</td>
<td>125</td>
<td>125</td>
<td>ns</td>
</tr>
<tr>
<td>Settling Time</td>
<td>+20 V or –20 V Output Step</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>To 1%</td>
<td></td>
<td>20</td>
<td>50</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>To 0.1%</td>
<td></td>
<td>20</td>
<td>50</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>( \pm 8 )</td>
<td>( \pm 16.5 )</td>
<td>( \pm 8 )</td>
<td>( \pm 16.5 )</td>
</tr>
<tr>
<td>Operating Range</td>
<td>( T_{MIN} ) to ( T_{MAX} )</td>
<td>( \pm 6 )</td>
<td>( \pm 12 )</td>
<td>( \pm 6 )</td>
<td>( \pm 12 )</td>
</tr>
</tbody>
</table>

**NOTES**

\(^1\)Figures given are percent of full scale (e.g., 0.01% = 1 mV).
\(^2\)dBc refers to deciBels relative to the full-scale input (carrier) level of 7 V rms.
\(^3\)See Figure 10 for test circuit.

All min and max specifications are guaranteed.
Specifications subject to change without notice.
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .................................. ±18 V
Internal Power Dissipation
for TJ max = 175°C .......................... 500 mW
X, Y and Z Input Voltages ............... VN to VP
Output Short Circuit Duration ........... Indefinite
Storage Temperature Range
Q .................................. –65°C to +150°C
Operating Temperature Range
AD734A, B (Industrial) .................. –40°C to +85°C
AD734S (Military) .................. –55°C to +125°C
Lead Temperature Range (soldering 60 sec) .... +300°C
Transistor Count ............................. 81
ESD Rating .................................. 500 V

NOTES
1Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
214-Lead Ceramic DIP: qJA = 110°C/W.

ORDERING GUIDE

<table>
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<th>Package Description</th>
<th>Package Option</th>
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<td>Plastic DIP</td>
<td>N-14</td>
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<tr>
<td>AD734BN</td>
<td>–40°C to +85°C</td>
<td>Plastic DIP</td>
<td>N-14</td>
</tr>
<tr>
<td>AD734AQ</td>
<td>–40°C to +85°C</td>
<td>Cerdip</td>
<td>Q-14</td>
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<td>AD734BQ</td>
<td>–40°C to +85°C</td>
<td>Cerdip</td>
<td>Q-14</td>
</tr>
<tr>
<td>AD734S/883B</td>
<td>–55°C to +125°C</td>
<td>Cerdip</td>
<td>Q-14</td>
</tr>
<tr>
<td>AD734SCHIPS</td>
<td>–55°C to +125°C</td>
<td>Die</td>
<td>Q-14</td>
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CHIP DIMENSIONS & BONDING DIAGRAM

Dimensions shown in inches and (mm).
(Contact factory for latest dimensions.)
FUNCTIONAL DESCRIPTION

Figure 1 is a simplified block diagram of the AD734. Operation is similar to that of the industry-standard AD534 and in many applications these parts are pin-compatible. The main functional difference is the provision for direct control of the denominator voltage, $U$, explained fully on the following page. Internal signals are actually in the form of currents, but the function of the AD734 can be understood using voltages throughout, as shown in this figure. Pins are named using upper-case characters (such as X1, Z2) while the voltages on these pins are denoted by subscripted variables (for example, $X_1$, $Z_2$).

The AD734’s differential X, Y and Z inputs are handled by wideband interfaces that have low offset, low bias current and low distortion. The AD734 responds to the difference signals $X = X_1 - X_2$, $Y = Y_1 - Y_2$ and $Z = Z_1 - Z_2$, and rejects common-mode voltages on these inputs. The X, Y and Z interfaces provide a nominally full-scale (FS) voltage of ±10 V, but, due to the special design of the input stages, the linear range of the differential input can be as large as ±17 V. Also unlike previous designs, the response on these inputs is not clipped abruptly above ±15 V, but drops to a slope of one half.

The bipolar input signals X and Y are multiplied in a translinear core of novel design to generate the product $XY/U$. The denominator voltage, $U$, is internally set to an accurate, temperature-stable value of 10 V, derived from a buried-Zener reference. An uncalibrated fraction of the denominator voltage $U$ appears between the voltage reference pin (ER) and the negative supply pin (VN), for use in certain applications where a temperature-compensated voltage reference is desirable. The uncommitted (open-loop) transfer function of the AD734 is

$$ W = A_0 \left\{ \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} - (Z_1 - Z_2) \right\}, $$

where $A_0$ is the open-loop transfer function of the AD734. It expresses a balance between the product $XY$ and the product $UZ$. The absence of the output, $W$, in this equation only reflects the fact that we have not yet specified which of the inputs is to be connected to the op amp output.

Most of the functions of the AD734 (including division, unlike the AD534 in this respect) are realized with $Z_1$ connected to $W$. So, substituting $W$ in place of $Z_1$ in the above equation results in an output:

$$ W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} + Z_2. $$

The free input $Z_2$ can be used to sum another signal to the output; in the absence of a product signal, $W$ simply follows the voltage at $Z_2$ with full 10 MHz bandwidth. When not needed for summation, $Z_2$ should be connected to the ground associated with the load circuit. We can show the allowable polarities in the following shorthand form:

$$ (\pm W) = \frac{(\pm X)(\pm Y)}{(\pm U)} \pm \pm Z. $$

In the recommended direct divider mode, the Y input is set to a fixed voltage (typically 10 V) and $U$ is varied directly; it may have any value from 10 mV to 10 V. The magnitude of the ratio $X/U$ cannot exceed 1.25; for example, the peak X-input for $U = 1$ V is ±1.25 V. Above this level, clipping occurs at the positive and negative extremities of the X-input.
the AD734 can be operated using the standard (AD534) divider connections (Figure 8), when the negative feedback path is established via the Y2 input. Substituting W for Y2 in Equation (2), we get

\[ W' = U \left( \frac{Z - Z_1}{X} \right) + Y_1. \]  

(5)

In this case, note that the variable X is now the denominator, and the above restriction (X/U ≤ 1.25) on the magnitude of the X input does not apply. However, X must be positive in order for the feedback polarity to be correct. Y1 can be used for summing purposes or connected to the load ground if not needed. The shorthand form in this case is

\[ (\pm W') = (\pm U) \left( \frac{Z}{+X} \right) + (\pm Y). \]  

(6)

In some cases, feedback may be connected to two of the available inputs. This is true for the square-rooting connections (Figure 9), where W is connected to both X and Y2. Setting \( X = W \) and \( Y_2 = W \) in Equation (2), and anticipating the possibility of again providing a summing input, so setting \( X_2 = S \) and \( Y_1 = S \), we find, in shorthand form

\[ (\pm W') = \sqrt{ (\pm U) (\pm Z) } + (\pm S). \]  

(7)

This is seen more generally to be the geometric-mean function, since both U and Z can be variable; operation is restricted to one quadrant. Feedback may also be taken to the U-interface. Full details of the operation in these modes is provided in the appropriate section of this data sheet.

**Direct Denominator Control**

A valuable new feature of the AD734 is the provision to replace the internal denominator voltage, U, with any value from +10 mV to +10 V. This can be used to (1) simply alter the multiplier scaling, thus improve accuracy and achieve reduced noise levels when operating with small input signals; (2) to implement an accurate two-quadrant divider, with a 1000:1 gain range and an asymptotic gain-bandwidth product of 200 MHz; (3) to achieve certain other special functions, such as AGC or rms.

Figure 2 shows the internal circuitry associated with denominator control. Note first that the denominator is actually proportional to a current, Iu, having a nominal value of 356 µA for \( U = 10 \) V, whereas the primary reference is a voltage, generated by a buried-Zener circuit and laser-trimmed to have a very low temperature coefficient. This voltage is nominally 8 V with a tolerance of ±10%.

![Figure 2. Denominator Control Circuitry](image)

After temperature-correction (block TC), the reference voltage is applied to transistor Qd and trimmed resistor Rr, which generate the required reference current. Transistor Qu and resistor Ru are not involved in setting up the internal denominator, and their associated control pins U0, U1 and U2 will normally be grounded. The reference voltage is also made available, via the 100 kΩ resistor Rr, at Pin 9 (ER); the purpose of Qr is explained below.

When the control pin DD (denominator disable) is connected to VP, the internal source of Iu is shut off, and the collector current of Qr must provide the denominator current. The resistor Ru is laser-trimmed such that the multiplier denominator is exactly equal to the voltage across it (that is, across pins U1 and U2). Note that this trimming only sets up the correct internal ratio; the absolute value of Ru (nominally 28 kΩ) has a tolerance of ±20%. Also, the alpha of Qu, (typically 0.995) which might be seen as a source of scaling error, is canceled by the alpha of other transistors in the complete circuit.

In the simplest scheme (Figure 3), an externally-provided control voltage, \( V_{G0} \), is applied directly to U0 and U2 and the resulting voltage across Ru is therefore reduced by one \( V_{BE} \). For example, when \( V_{G0} = 2 \) V, the actual value of U will be about 1.3 V. This error will not be important in some closed-loop applications, such as automatic gain control (AGC), but clearly is not acceptable where the denominator value must be well-defined. When it is required to set up an accurate, fixed value of U, the on-chip reference may be used. The transistor Qr is provided to cancel the \( V_{BE} \) of Qu, and is biased by an external resistor, R2, as shown in Figure 4. R1 is chosen to set the desired value of U and consists of a fixed and adjustable resistor.

![Figure 3. Low-Accuracy Denominator Control](image)

![Figure 4. Connections for a Fixed Denominator](image)

Table I shows useful values of the external components for setting up nonstandard denominator values.
The denominator can also be current controlled, by grounding Pin 3 (U0) and withdrawing a current of Iu from Pin 4 (U1).

The output ER may also be buffered, re-scaled and used as a general-purpose reference voltage. It is generated with respect to the negative supply line Pin 8 (VN), but this is acceptable when driving one of the signal interfaces. An example is shown in Figure 12, where a fixed numerator of 10 V is generated for a divider application. There, Y2 is tied to VN but Y1 is 10 V above this; therefore the common-mode voltage at this interface is still 5 V above VN, which satisfies the internal biasing requirements (see Specifications table).

OPERATION AS A MULTIPLIER

All of the connection schemes used in this section are essentially identical to those used for the AD534, with which the AD734 is pin-compatible. The only precaution to be noted in this regard is that in the AD534, Pins 3, 5, 9, and 13 are not internally connected and Pin 4 has a slightly different purpose. In many cases, an AD734 can be directly substituted for an AD534 with immediate benefits in static accuracy, distortion, feedthrough, and speed. Where Pin 4 was used in an AD534 application to achieve a reduced denominator voltage, this function can now be much more precisely implemented with the AD734 using alternative connections (see Direct Denominator Control, page 5).

Operation from supplies down to ±8 V is possible. The supply current is essentially independent of voltage. As is true of all high speed circuits, careful power-supply decoupling is important in maintaining stability under all conditions of use. The decoupling capacitors should always be connected to the load ground, since the load current circulates in these capacitors at high frequencies. Note the use of the special symbol (a triangle with the letter 'L' inside it) to denote the load ground.

**Standard Multiplier Connections**

Figure 5 shows the basic connections for multiplication. The X and Y inputs are shown as optionally having their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

The AD734 has an input resistance of 50 kΩ ± 20% at the X, Y, and Z interfaces, which allows ac-coupling to be achieved with moderately good control of the high-pass (HP) corner frequency; a capacitor of 0.1 μF provides a HP corner frequency of 32 Hz. When a tighter control of this frequency is needed, or when the HP corner is above about 100 kHz, an external resistor should be added across the pair of input nodes.

At least one of the two inputs of any pair must be provided with a dc path (usually to ground). The careful selection of ground returns is important in realizing the full accuracy of the AD734. The Z2 pin will normally be connected to the load ground, which may be remote, in some cases. It may also be used as an optional summing input (see Equations (3) and (4), above) having a nominal FS input of ±10 V and the full 10 MHz bandwidth.

In applications where high absolute accuracy is essential, the scaling error caused by the finite resistance of the signal source(s) may be troublesome; for example, a 50 Ω source resistance at just one input will introduce a gain error of −0.1%; if both the X- and Y-inputs are driven from 50 Ω sources, the scaling error in the product will be −0.2%. Provided the source resistance(s) are known, this gain error can be completely compensated by including the appropriate resistance (50 Ω or 100 Ω, respectively, in the above cases) between the output W (Pin 12) and the Z1 feedback input (Pin 11). If Rx is the total source resistance associated with the X1 and X2 inputs, and Ry is the total source resistance associated with the Y1 and Y2 inputs, and neither Rx nor Ry exceeds 1 kΩ, a resistance of Rx+Ry in series with pin Z1 will provide the required gain restoration.

Pins 9 (ER) and 13 (DD) should be left unconnected in this application. The U-inputs (Pins 3, 4 and 5) are shown connected to ground; they may alternatively be connected to VN, if desired. In applications where Pin 2 (X2) happens to be driven with a high-amplitude, high-frequency signal, the capacitive coupling to the denominator control circuitry via an ungrounded Pin 3 can cause high-frequency distortion. However, the AD734 can be operated without modification in an AD534 socket, and these three pins left unconnected, with the above caution noted.
Current Output
It may occasionally be desirable to convert the output voltage to a current. In correlation applications, for example, multiplication is followed by integration; if the output is in the form of a current, a simple grounded capacitor can perform this function.

The smallest FS current is simply ±10 V/50 kΩ, or ±200 µA, with a tolerance of about 20%. To guarantee a 1% conversion tolerance without adjustment, R5 must be less than 2.5 kΩ. The maximum full scale output current should be limited to about ±10 mA (thus, R5 = 1 kΩ). This concept can be applied to all connection modes, with the appropriate choice of terminals.

Squaring and Frequency-Doubling
Squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel; the phasing can be chosen to produce an output of E^2/U or -E^2/U as desired. The input may have either polarity, but the basic output will either always be positive or negative; as for multiplication, the Z2 input may be used to add a further signal to the output.

When the input is a sine wave, a squarer behaves as a frequency-doubler, since

\[(E \sin wt)^2 = E^2 (1 - \cos 2wt)/2\]  \(8\)

Equation (8) shows a dc term at the output which will vary strongly with the amplitude of the input, E. This dc term can be avoided using the connection shown in Figure 7, where an RC-network is used to generate two signals whose product has no dc term. The output is

\[W = 4 \left( \frac{E}{\sqrt{2}} \sin \left( \frac{wt + \pi}{4} \right) \right) \left( \frac{E}{\sqrt{2}} \sin \left( \frac{wt - \pi}{4} \right) \right) \left( \frac{1}{10 V} \right)\]  \(9\)

for \(w = 1/CR1\), which is just

\[W = E^2 (\cos 2wt)/(10 V)\]  \(10\)

which has no dc component. To restore the output to ±10 V when \(E = 10 V\), a feedback attenuator with an approximate ratio of 4 is used between W and Z1; this technique can be used wherever it is desired to achieve a higher overall gain in the transfer function.

In fact, the values of R3 and R4 include additional compensation for the effects of the 50 kΩ input resistance of all three interfaces; R2 is included for a similar reason. These resistor values should not be altered without careful calculation of the consequences; with the values shown, the center frequency \(f_0\) is 100 kHz for \(C = 1 \text{nF}\). The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at \(f = 0.9f_0\) and \(f = 1.1f_0\). The cross-connection is simply to produce the cosine output with the sign shown in Equation (10); however, the sign in this case will rarely be important.

OPERATION AS A DIVIDER
The AD734 supports two methods for performing analog division. The first is based on the use of a multiplier in a feedback loop. This is the standard mode recommended for multipliers having a fixed scaling voltage, such as the AD534, and will be described in this Section. The second uses the AD734’s unique capability for externally varying the scaling (denominator) voltage directly, and will be described in the next section.

Feedback Divider Connections
Figure 8 shows the connections for the standard (AD534) divider mode. Feedback from the output, W, is now taken to the Y2 (inverting) input, which, provided that the X-input is positive, establishes a negative feedback path. Y1 should normally be connected to the ground associated with the load circuit, but may optionally be used to sum a further signal to the output. If desired, the polarity of the Y-input connections can be reversed, with W connected to Y1 and Y2 used as the optional summation input. In this case, either the polarity of the X-input connections must be reversed, or the X-input voltage must be negative.

Figure 8. Standard (AD534) Divider Connection
The numerator input, which is differential and can have either polarity, is applied to pins Z1 and Z2. As with all dividers based on feedback, the bandwidth is directly proportional to the denominator, being 10 MHz for \(X = 10 V\) and reducing to 100 kHz for \(X = 100 \text{mV}\). This reduction in bandwidth, and the increase in output noise (which is inversely proportional to the denominator voltage) preclude operation much below a denominator of 100 mV. Division using direct control of the denominator (Figure 10) does not have these shortcomings.
but the difference \( U = U_1 - U_2 \) must be positive and in the
where the \( X, Y, \) and \( Z \) signals may all be positive or negative,

Note that the loading on the output side of the diode will be
always negative because of the reversed-polarity between these
two inputs. The \( Z \) input must have the polarity shown, but
because it is applied to a differential port, either polarity of
input can be accepted with reversal of \( Z_1 \) and \( Z_2 \), if necessary.
The diode \( D \), which can be any small-signal type (1N4148
being suitable) is included to prevent a latching condition which
could occur if the input momentarily was of the incorrect
polarity of the input, the output will be always negative.

Note that the loading on the output side of the diode will be
provided by the 25 kΩ of input resistance at \( X_1 \) and \( Y_2 \), and by
the user’s load. In high speed applications it may be beneficial
to include further loading at the output (to 1 kΩ minimum) to
speed up response time. As in previous applications, a further
signal, shown here as \( S \), may be summed to the output; if this
option is not used, this node should be connected to the load
ground.

**DIVISION BY DIRECT DENOMINATOR CONTROL**
The AD734 may be used as a two-quadrant divider with fixed scaling, the connections shown in
Figure 12 may be used. The reference voltage output appearing
between Pin 9 (ER) and Pin 8 (VN) is amplified and buffered
by the second op amp, to impose 10 V across the \( Y_1/Y_2 \) input.

Where a numerator of 10 V is needed, to implement a two-

\[ W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} + Z_2, \]  

where the \( X, Y, \) and \( Z \) signals may all be positive or negative,
but the difference \( U = U_1 - U_2 \) must be positive and in the
range +10 mV to +10 V. If a negative denominator voltage must
be used, simply ground the noninverting input of the op amp.
As previously noted, the \( X \) input must have a magnitude of less
than 1.25U.

This connection scheme may also be viewed as a variable-gain
element, whose output, in response to a signal at the \( X \) input, is
controllable by both the \( Y \) input (for attenuation, using \( Y \) less
than \( U \)) and the \( U \) input (for amplification, using \( U \) less than
\( Y \)). The ac performance is shown in Figure 11; for these results,
\( Y \) was maintained at a constant 10 V. At \( U = 10 \) V, the gain is
unity and the circuit bandwidth is a full 10 MHz. At \( U = 1 \) V,
the gain is 20 dB and the bandwidth is essentially unaltered. At
\( U = 100 \) mV, the gain is 40 dB and the bandwidth is 2 MHz.
Finally, at \( U = 10 \) mV, the gain is 60 dB and the bandwidth is
250 kHz, corresponding to a 250 MHz gain-bandwidth product.

**Figure 11. Three-Variable Multiplier/Divider Performance**
The 2 MΩ resistor is included to improve the accuracy of the
gain for small denominator voltages. At high gains, the \( X \) input
offset voltage can cause a significant output offset voltage. To
eliminate this problem, a low-pass feedback path can be used
from \( W \) to \( X_2 \); see Figure 13 for details.

Where a numerator of 10 V is needed, to implement a two-

\[ W = 10 \, V \left( \frac{X_1 - X_2}{U_1 - U_2} \right) + Z_2, \]  

The ac performance of this circuit remains as shown in Figure 11.
A PRECISION AGC LOOP

The variable denominator of the AD734 and its high gain-bandwidth product make it an excellent choice for precise automatic gain control (AGC) applications. Figure 13 shows a suggested method. The input signal, $E_{IN}$, which may have a peak amplitude of from 10 mV to 10 V at any frequency from 100 Hz to 10 MHz, is applied to the X input, and a fixed positive voltage $E_C$ to the Y input. Op amp A2 and capacitor C2 form an integrator having a current summing node at its inverting input. (The AD712 dual op amp is a suitable choice for this application.) In the absence of an input, the current in D2 and R2 causes the integrator output to ramp negative, clamped by diode D3, which is included to reduce the time required for the loop to establish a stable, calibrated, output level once the circuit has received an input signal. With no input to the denominator (U0 and U2), the gain of the AD734 is very high (about 70 dB), and thus even a small input causes a substantial output. Diode D1 and C1 form a peak detector, which rectifies the output and causes the integrator to ramp positive. When the current in R1 balances the current in R2, the integrator output holds the denominator output at a constant value. This occurs when there is sufficient gain to raise the amplitude of $E_{DC}$ to that required to establish an output amplitude of $E_C$ over the range of +1 V to +10 V. The X input of the AD734, which has finite offset voltage, could be troublesome at the output at high gains.

Figure 13. Precision AGC Loop

In applications not requiring operation down to low frequencies, amplifier A1 can be eliminated, but the AD734's input resistance of 50 kΩ between X1 and X2 will reduce the time constant and increase the input offset. Using a non-polar 20 μF tantalum capacitor for C1 will result in the same unity-gain high-pass corner; in this case, the offset gain increases to 20, still very acceptable.

Figure 14 shows the error in the output for sinusoidal inputs at 100 Hz, 100 kHz, and 1 MHz, with $E_C$ set to +10 V. The output error for any frequency between 300 Hz and 300 kHz is similar to that for 100 kHz. At low signal frequencies and low input amplitudes, the dynamics of the control loop determine the gain error and distortion; at high frequencies, the 200 MHz gain-bandwidth product of the AD734 limit the available gain.

The output amplitude tracks $E_C$ over the range +1 V to slightly more than +10 V.

Figure 14. AGC Amplifier Output Error vs. Input Voltage

WIDEBAND RMS-DC CONVERTER USING U INTERFACE

The AD734 is well suited to such applications as implicit RMS-DC conversion, where the AD734 implements the function

$$V_{RMS} = \frac{\text{avg} \left[ \frac{V_{IN}}{V_{RMS}} \right]^2}{V_{RMS}}$$

(13)

using its direct divide mode. Figure 15 shows the circuit. In this application, the AD734 and an AD708 dual op amp serve as a 2-chip RMS-DC converter with a 10 MHz bandwidth. Figure 16 shows the circuit's performance for square-, sine-, and triangle-wave inputs. The circuit accepts signals as high as 10 V p-p with a crest factor of 1 or 1 V p-p with a crest factor of 10. The circuit’s response is flat to 10 MHz with an input of 10 V, flat to almost 5 MHz for an input of 1 V, and to almost 1 MHz for inputs of 100 mV. For accurate measurements of input levels below 100 mV, the AD734’s output offset (Z interface) voltage, which contributes a dc error, must be trimmed out.

In Figure 15’s circuit, the AD734 squares the input signal, and its output ($V_{IN}^2$) is averaged by a low-pass filter that consists of R1 and C1 and has a corner frequency of 1 Hz. Because of the implicit feedback loop, this value is both the output value, $V_{RMS}$, and the denominator in Equation (13). U2a and U2b, an AD708 dual dc precision op amp, serve as unity-gain buffers, supplying both the output voltage and driving the U interface.
LOW DISTORTION MIXER

The AD734’s low noise and distortion make it especially suitable for use as a mixer, modulator, or demodulator. Although the AD734’s –3 dB bandwidth is typically 10 MHz and is established by the output amplifier, the bandwidth of its X and Y interfaces and the multiplier core are typically in excess of 40 MHz. Thus, provided that the desired output signal is less than 10 MHz, as would typically be the case in demodulation, the AD734 can be used with both its X and Y input signals as high as 40 MHz. One test of mixer performance is to linearly combine two closely spaced, equal-amplitude sinusoidal signals and then mix them with a third signal to determine the mixer’s 2-tone Third-Order Intermodulation Products.

If the two X1 inputs are at frequencies \( f_1 \) and \( f_2 \) and the frequency at the Y1 input is \( f_0 \), then the two-tone third-order intermodulation products should appear at frequencies \( 2f_1 - f_2 \pm f_0 \) and \( 2f_2 - f_1 \pm f_0 \). Figures 18 and 19 show the output spectra of the AD734 with \( f_1 = 9.95 \text{ MHz} \), \( f_2 = 10.05 \text{ MHz} \), and \( f_0 = 9.00 \text{ MHz} \) for a signal level of \( f_1 \) & \( f_2 \) of 6 dBm and \( f_0 \) of +24 dBm in Figure 18 and \( f_1 \) & \( f_2 \) of 0 dBm and \( f_0 \) of +24 dBm in Figure 19. This performance is without external trimming of the AD734’s X and Y input-offset voltages.

The possible Two Tone Intermodulation Products are at \( 2 \times 9.95 \text{ MHz} - 10.05 \text{ MHz} \pm 9.00 \text{ MHz} \) and \( 2 \times 10.05 \text{ MHz} - 9.95 \text{ MHz} \pm 9.00 \text{ MHz} \); of these only the third-order products at 0.850 MHz and 1.150 MHz are within the 10 MHz bandwidth of the AD734; the desired output signals are at 0.950 MHz and 1.050 MHz. Note that the difference (Figure 18) between the desired outputs and third-order products is approximately 78 dB, which corresponds to a computed third-order intercept point of +46 dBm.
AD734—Typical Characteristics

Figure 29. Gain vs. Frequency vs. CLOAD

Figure 30. Phase vs. Frequency vs. CLOAD

Figure 31. Pulse Response vs. CLOAD, CLOAD = 0 pF, 47 pF, 100 pF, 200 pF

Figure 32. Output Swing vs. Supply Voltage

Figure 33. Output Amplitude vs. Input Frequency, When Used as Demodulator

Figure 34. VOS Drift, X Input

Figure 35. VOS Drift, Z Input

Figure 36. VOS Drift, Y Input

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP (N) Package

14-Lead Ceramic DIP (Q) Package