Evaluation Board User Guide

EVAL-AD7626/25FMCZ

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Evaluating the AD7626/25 16-Bit, 10/6 MSPS PulSAR Differential ADC

FEATURES

Full-featured evaluation board for the AD7626 and AD7625
Versatile analog signal conditioning circuitry
On-board reference, reference buffers, and ADC drivers
System demonstration board compatible (EVAL-SDP-CH1Z)
PC software for control and data analysis of time and frequency domain

EVALUATION KIT CONTENTS

EVAL-AD7626/25FMCZ evaluation board

ADDITIONAL EQUIPMENT AND SOFTWARE NEEDED

System demonstration platform (EVAL-SDP-CH1Z)
Precision source
World-compatible, 12 V dc supply adapter (enclosed with EVAL-SDP-CH1Z)
Power supply, +7 V/−2.5 V (optional)
USB cable
SMA cable

ONLINE RESOURCES

Documents Needed
AD7626, AD7625 data sheet
EVAL-AD7626/25FMCZ user guide
Required Software
EVAL-AD7626/25FMCZ evaluation software
Design and Integration Files
Schematics, layout files, bill of materials

GENERAL DESCRIPTION

The EVAL-AD7626/25FMCZ is an evaluation board designed to demonstrate the low power AD7626/25 performance (16-bit, 10/6 MSPS PulSAR® differential ADC) and to provide an easy-to-understand interface for a variety of system applications. A full description of the AD7626 and AD7625 are available in the data sheet and should be consulted when utilizing this evaluation board. The user PC software executable controls the evaluation board over the USB through the Analog Devices, Inc., system demonstration platform board (SDP), EVAL-SDP-CH1Z.

On-board components include the following:

ADR3412/ADR4540 high precision, buffered band gap 1.2 V/4.096 V reference options

AD8031: reference buffer

ADA4899-1/ADA4897-1: a signal conditioning circuit with two op amps and an option to use a differential amplifier (ADA4932-1)

ADP7102, ADP7104, ADP124, and ADP2300: regulators to derive necessary voltage levels on board

This evaluation board interfaces to the SDP board via a 160-pin FMC connector. SMA connectors, JP1/JP4 and JP2/JP5, are provided for the low noise analog signal source.

Figure 1. Setting Up the EVAL-AD7626/25FMCZ

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REVISION HISTORY

7/14—Revision PrA: Preliminary Version

FUNCTIONAL BLOCK DIAGRAM

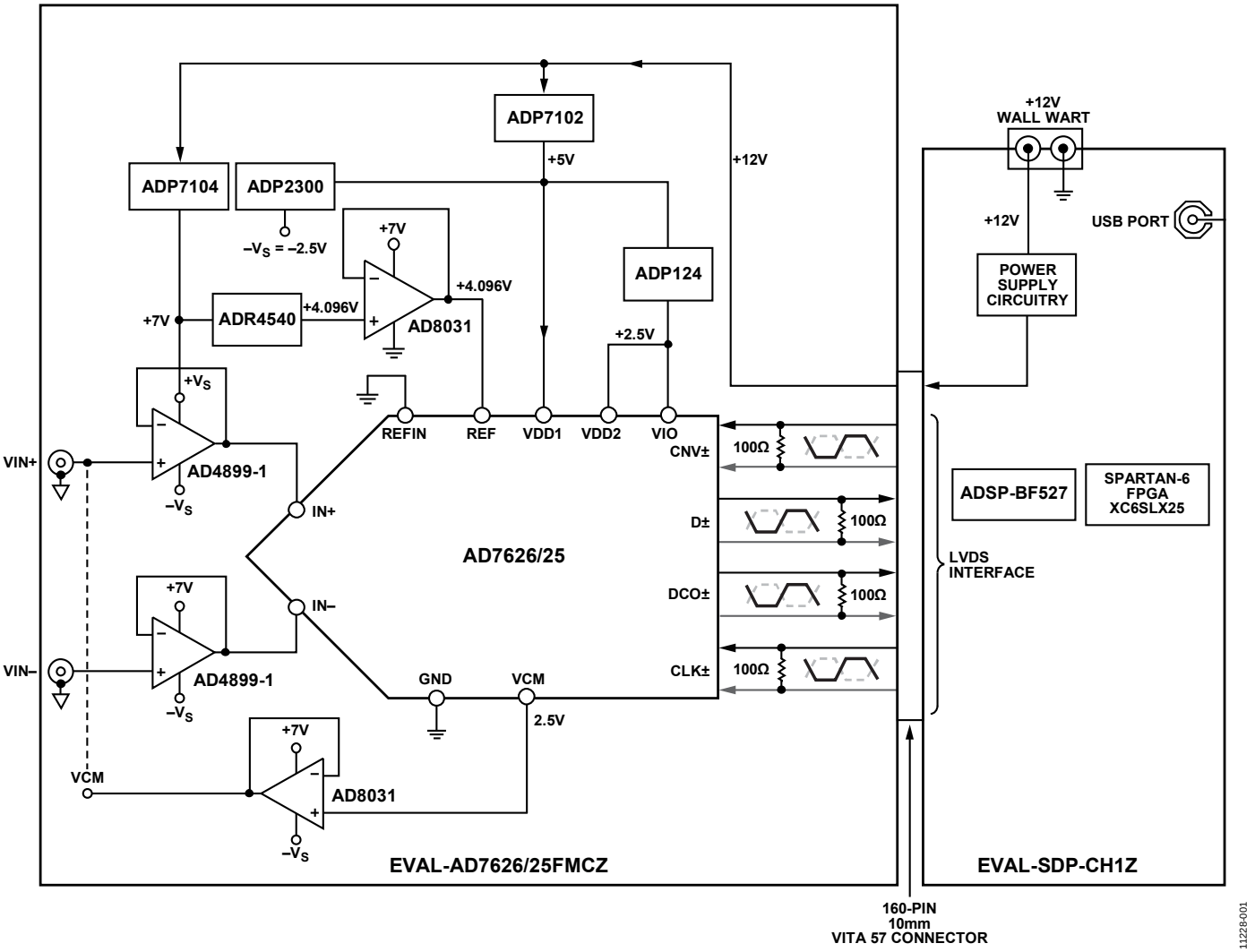

Figure 2.

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7626/25 are 10/6 MSPS, high precision, power efficient, 16-bit PulSAR ADC that uses SAR-based architecture and does not exhibit any pipeline delay or latency. The AD7626/25 are specified for use with 5 V and 2.5 V supplies (VDD1, VDD2). The interfaces from the digital host to the AD7626/25 use 2.5 V logic only.

The AD7626/25 use an LVDS interface to transfer data conversions. Complete AD7626/25 specifications are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details on the EVAL-SDP-CH1Z are available on the Analog Devices website.

HARDWARE LINK OPTIONS

The function of the link options are described in Table 1. When the user first receives the board, the default link setting on the board are as shown in Table 1 (analog input/reference/power supplies, and so on).

POWER SUPPLIES

The power (+12 V) for the EVAL-AD7626/25FMCZ board comes through a 160-pin FMC connector, J7, from the EVAL-SDP-CH1Z. The customer also has the option of using external bench top supplies to power the on-board amplifiers. On-board regulators generate required levels from the applied +12 V rail.

The ADP7102 (U18) supplies +7 V for the $+V_S$ of the ADC driver amplifiers (ADA4899-1 or ADA4932-1), external reference ADR4540 (U14), while the ADP7104 (U10) delivers +5 V for VDD1 (U1), external reference ADR3412 (U14), ADP2300 (U5), and ADP124 (U12 and U16). The ADP2300 (U5), in turn, generates −2.5 V for the amplifier's $-V_S$ and the ADP124 (U12 and U16), in turn, provides a 2.5 V for VDD2 and VIO (U1).

The +3.3 V supply for the EEPROM (U7) comes from the EVAL-SDP-CH1Z through a 160-pin FMC connector, J7. Each supply is decoupled where it enters the board and again at each device. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 1. Pin Jumper Descriptions

Link	Default	Purpose
JP1, JP2	B to center	Connect the CNV+ and CNV- from the FPGA. A to center connect the CNV signal from AD9513.
JP6	B to center	Connects +7 V to amplifier $+V_S$.
JP10	B to center	Connects −2.5 V to amplifier $-V_S$.
JP11, JP12	B to center	Connects analog inputs VIN+ and VIN− to the inputs of the ADC driver ADA4899-1 or ADA4897-1. A to center sets the fully differential path through ADA4932-1.
JP13, JP14	B to center	Connect outputs from ADA4899-1 to inputs of ADC. A to center set the fully differential path through ADA4932-1.
LK2	Inserted	Connects REFIN to 1.2 V external reference.
LK3	Inserted	Connects the 4.096V output from ADR4540 after buffer AD8031.
LK6	B	Connects the output of VCM buffer to VCM of amplifier.
LK9	A	Connects to +7 V coming from ADP7102.
LK10	A	Connects to −2.5 V coming from ADP2300.

Table 2. On-Board Connectors

Connector	Function
J1	SMA low noise, low jitter clock source input.
J2, J10	SMA CNV Input, this option is for using external CNV signal.
J3, J5, J6, J8	SMA Analog Input. Connects the low noise analog signal source to the inputs of the ADC driver ADA4899-1, ADA4897-1, or ADA4932-1.
J4	3-Pin Terminal. This option is for using external bench top supplies. Apply external +Vs, −Vs, and GND to power amplifiers on the EVAL-AD7626/25FMCZ board.
J9	6-Pin (2 × 3) Socket. This option is for interfacing with an external ADC driver board.
J7	160-Pin FMC 10 mm Male VITA 57 Connector. This connector mates with the EVAL-SDP-CH1Z board.
J11, J12	SMA low noise, low jitter clock output from AD9513.

Table 3. On-Board Power Supplies Description

Power Supply	Voltage Range (V)	Purpose
$+V_S$	+5 V to +7 V	ADP7104 (U10) and ADP7102 (U18) generate the necessary +5 V and +7 V, respectively, from +12 V coming from EVAL-SDP-CH1Z. The +7 V supply is recommended for on-board amplifier $+V_S$. The +5 V supply is provided to VDD1 (U1), external reference ADR3412 (U14), ADP2300 (U5), and ADP124 (U12 and U16). The user also has an option to use an external bench top supply $+V_S$ through J4.
$-V_S$	−2 V to −5 V	ADP2300 generates −2.5 V for amplifier $-V_S$. The user also has an option to use an external bench top supply $-V_S$ through J4.
$\|+V_S$ to $-V_S\|$	12 V[1]	Maximum range of supply for correct operation.
VDD1	5 V[2]	AD7626/25 Analog Supply Rail.
VDD2, VIO	2.5 V[2]	ADC Supply Rails.

[1]Dictated by ADA4899-1 supply operation.
[2]Refer to the AD7626 , AD7625 data sheet

SERIAL INTERFACE

The EVAL-AD7626/25FMCZ uses the serial interface connection to the EVAL-SDP-CH1Z. The EVAL-AD7626/25-FMCZ operates only in echo-clocked serial interface mode. This mode requires three LVDS pairs (D±, CLK±, and DCO±) between AD7626/25 and the digital host. The EVAL-SDP-CH1Z board features include

- XILINX Spartan®-6 FPGA
- DDR2
  - Micron MT47H32M16Hr-25E:G
    −8 Mb × 16 bits × 4 Banks(512 Mb/64 Mb)
- SRAM
  - ISSI IS61WV25616BLL-10BLI
    −256 kB × 16 bits (4 Mb/512 kB)
- 1 × 160-pin FMC-LPC connector (refer to the VITA 57 specification)
  - Samtec ASP-134603-01
  - Up to 1080 Mbps LVDS
  - Single-ended LVCMOS
  - Power
- Analog Devices ADSP-BF527 Blackfin® processor
  - Core performance up to 600 MHz
  - 208-ball CSP-BGA package
  - 24 MHz CLKIN oscillator
- 32 Mb flash memory
  - Numonyx M29W320EB or
  - Numonyx M25P32
- SDRAM memory
  - Micron MT48LC16M16A2P-6A
    −16 Mb × 16 bits (256 Mb/32 MB)
- 2 × 120-pin small foot print connectors
  - Hirose FX8-120P-SV1(91),120-pin header
- Blackfin processor peripherals exposed
  - SPI
  - SPORT
  - TWI/I²C
  - GPIO
  - PPI
  - Asynchronous parallel

ANALOG INPUTS

This section provides information on the analog input options and how these options can be configured as well as information on how customers should connect their signal source.

The analog inputs applied to the EVAL-AD7626/25FMCZ board are J3 and J5 SMA (push-on) connectors. These inputs are buffered with dedicated discrete driver amplifier circuitry (U13 and U15 or U6) as shown in Figure 1.

The circuit allows for different configurations, input range scaling, filtering, the addition of a dc component, and the use of a different op amp, and a differential amplifier and supplies. The analog input amplifiers are set as unity gain buffers at the factory. The driver amplifiers (U6, U13, and U15) positive rails are driven from +7 V (from ADP7102, U18) and negative rail from −2.5 V; the other reference buffers (U8 and U11) positive rails are driven from +7 V and negative rails are grounded; these could be changed to a different value as required.

The range of supplies possible is listed in Table 3. The default configuration sets both U13 and U15 at mid-scale generated from a buffered reference voltage (VCM) of the AD7626/25 (U1). The evaluation board is factory configured for providing either a single-ended path or a fully differential path as described in Table 1.

For dynamic performance, an FFT test can be performed by applying a very low distortion source.

For low frequency testing, the audio precision source can be used directly because the outputs on these are isolated. Set the outputs for balanced and floating. Different sources can be used though most are single ended and use a fixed output resistance.

Since the evaluation board uses the amplifiers in unity gain, the noninverting input has a common-mode input with a series

1K Ω resistor and it needs to be taken into account when directly connecting a source (voltage divider).

REFERENCE OPTIONS

The AD7626/25has an internal 4.096V reference along with and internal buffer useful for using an external reference or can use directly an external 4.096V reference. The evaluation board can be configured to use any of these references. For using the internal ADC reference, leave LK2 and LK3 open. To use the ADR4540, insert LK3, let LK2 open. (The 4.096V output of the ADR4540 is buffered by an AD8031in a unity gain configuration).

For using the internal reference buffer on the AD7626/25 REFIN pin, insert LK2, let LK3 open. The 1.2V reference voltage applied to REFIN, prior to the internal buffer in the AD7626/25device, which creates the required internal 4.096V. (The 1.2V output of the ADR3412 is buffered by an AD8031in a unity gain configuration). The various options for using this reference are controlled by the EN1 and EN0 pins (EN bits on software) as described in detail in the AD7626/25 data sheet.

LAYOUT GUIDELINES

When laying out the printed circuit board (PCB) for the AD7626/25, follow the recommended guidelines described in this section to obtain the maximum performance from the converter.

- Solder the AD7626/25 exposed paddle (Pin 33) directly to the PCB and connect the paddle to the ground plane of the board using multiple vias.
- Decouple all the power supply pins (VDD1, VDD2, and VIO) and the REF pin with low ESR and low ESL ceramic capacitors, typically 10 µF and 100 nF, placed close to the DUT (U1) and connected using short, wide traces. This provides low impedance paths and reduces the effect of glitches on the power supply lines.
- Use a 50 Ω single-ended trace and a 100 Ω differential trace.
- Separate analog and digital sections and keep power supply circuitry away from the AD7626/25.
- Avoid running digital lines under the device as well as crossover of digital and analog signals because these couple noise into the AD7626/25.
- Fast switching signals, such as CNV or clocks, should not run near analog signal paths.
- Remove the ground and power plane beneath the input (including feedback) and output pins of the amplifiers (U6, U13, and U15) since they create an undesired capacitor.

BASIC HARDWARE SETUP

The AD7626/25 evaluation board connects to the (EVAL-SDP-CH1Z) system demonstration board. The EVAL-SDP-CH1Z board is the controller board, which is the communication link between the PC and the main evaluation board.

Figure 1 shows a photograph of the connections made between the EVAL-AD7626/25FMCZ daughter board and the EVAL-SDP-CH1Z board.

1. Install the AD7626/25 software. Ensure the EVAL-SDP-CH1Z board is disconnected from the USB port of the PC while installing the software. The PC must be restarted after the installation.
2. Before connecting power, connect the EVAL-AD7626/-25FMCZ board's 160-pin FMC connector, J7, to the connector J4 on the EVAL-SDP-CH1Z board. Nylon screws are included in the EVAL-AD7626/25FMCZ evaluation kit and can be used to ensure the EVAL-AD7626/25FMCZ and the EVAL-SDP-CH1Z boards are connected firmly together.
3. Connect the +12 V power supply adapter included in the kit to the EVAL-SDP-CH1Z.
4. Connect the EVAL-SDP-CH1Z board to the PC via the USB cable. Windows XP users may need to search for the EVAL-SDP-CH1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CH1Z board if prompted by the operating system.
5. Launch the EVAL-AD7626/25FMCZ software from the **Analog Devices** subfolder in the **Programs** menu. The full software installation procedure is detailed in the Evaluation Board Software section.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The evaluation board software is available to download from the evaluation board page on Analog Devices website. Click the **setup.exe** file to run the install. The default location for the software is **C:\Program Files (x86)\Analog Devices\ AD7626_25 Evaluation Software**.

Install the evaluation software before connecting the evaluation board and EVAL-SDP-CH1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts of the software installation process:

- AD7626/25 evaluation board software installation
- EVAL-SDP-CH1Z board driver installation

Figure 3 to Figure 9 show the separate steps to install the AD7626/25 evaluation software while Figure 10 to Figure 14 show the separate steps to install the EVAL-SDP-CH1Z drivers. Proceed through all of the installation steps to allow the software and drivers to be placed in the appropriate locations. Only after the software and drivers have been installed, should you connect the EVAL-SDP-CH1Z board to the PC.

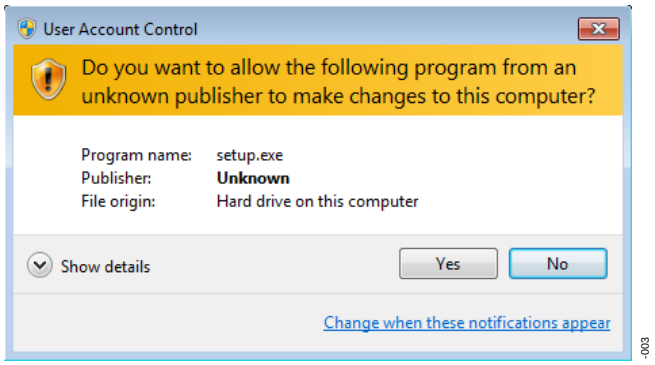

Figure 3. User Account Control

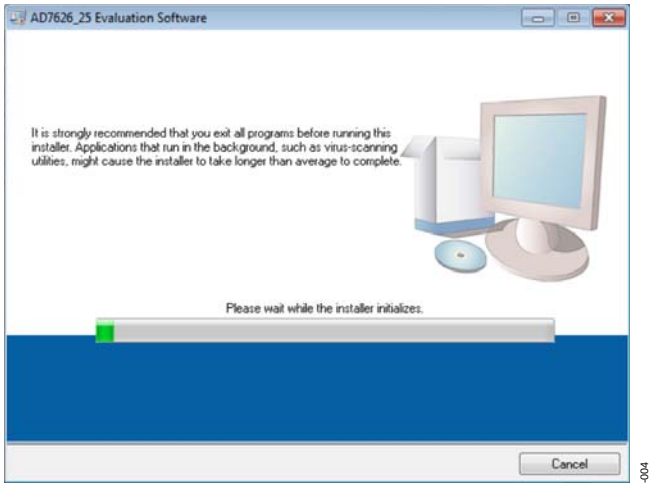

Figure 4. AD7626/25 Install Window 1

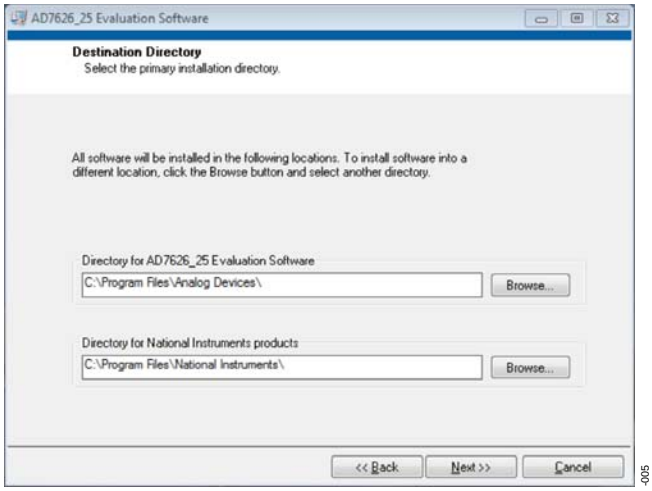

Figure 5. AD7626/25 Install Window 2

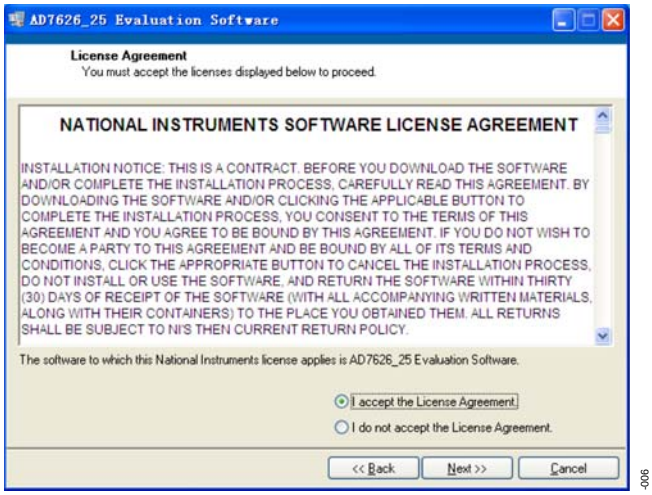

Figure 6. AD7626/25 Install Window 3

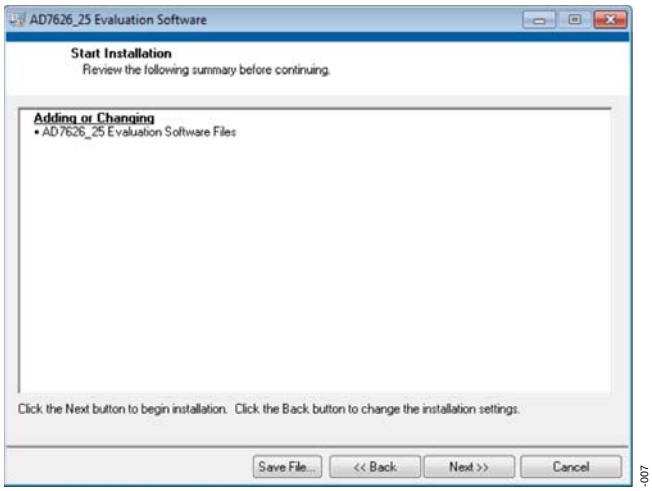

Figure 7. AD7626/25 Install Window 4

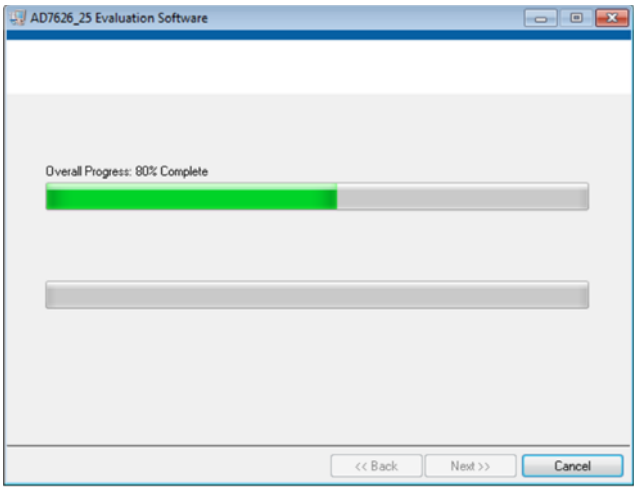

Figure 8. AD7626/25 Install Window 5

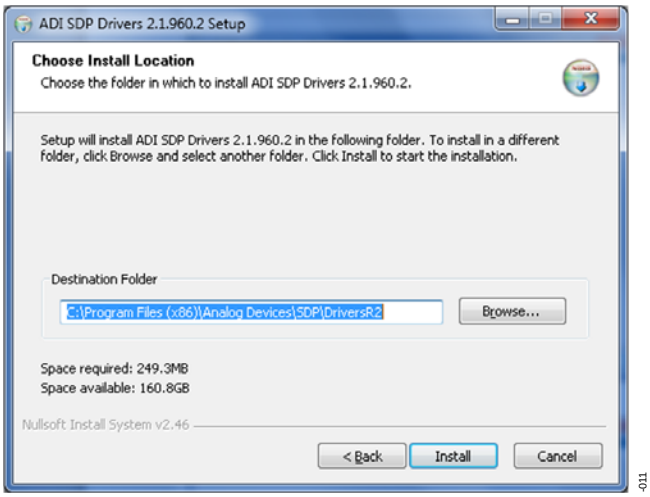

Figure 11. EVAL-SDP-CH1Z Drivers Setup Window 2

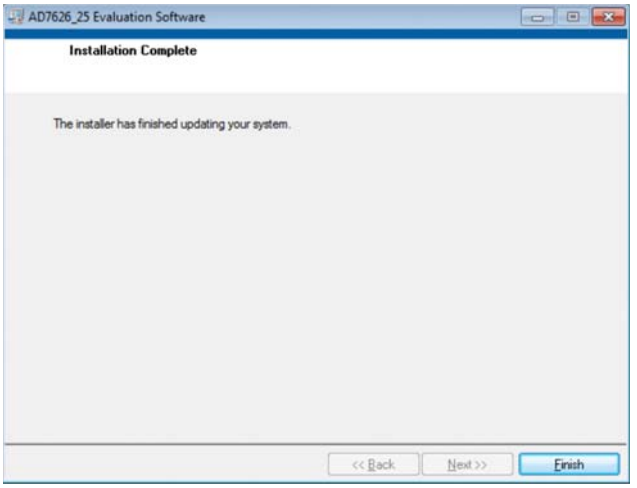

Figure 9. AD7626/25 Install Window 6

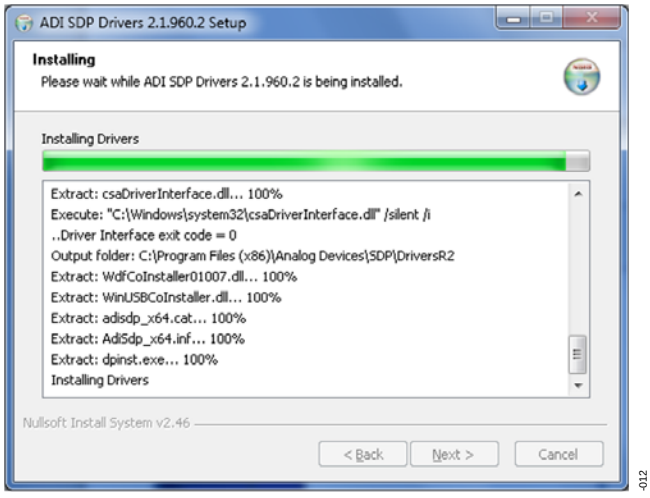

Figure 12. EVAL-SDP-CH1Z Drivers Setup Window 3

Figure 10. EVAL-SDP-CH1Z Drivers Setup Window 1

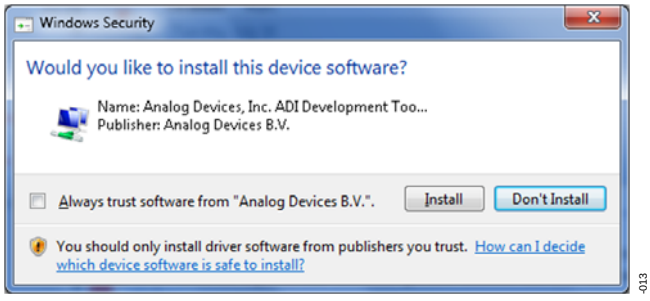

Figure 13. EVAL-SDP-CH1Z Drivers Setup Window 4

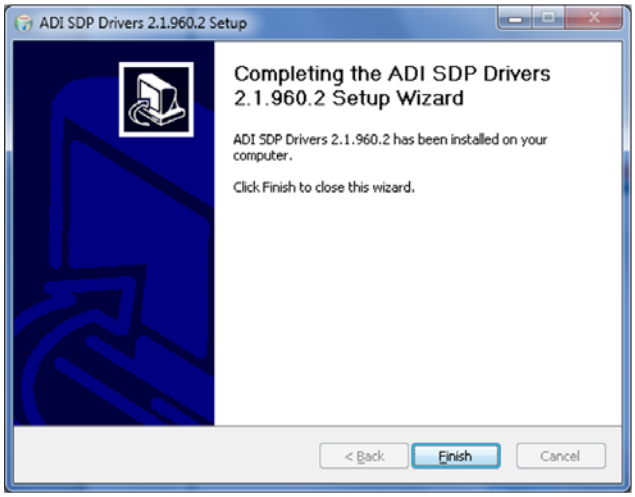

Figure 14. EVAL-SDP-CH1Z Drivers Setup Window 5

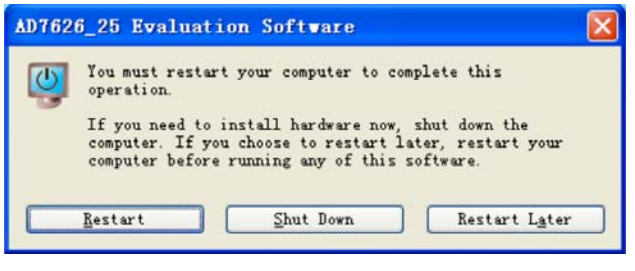

Figure 15. EVAL-SDP-CH1Z Drivers Setup Window 6

After installation is complete, connect the EVAL-AD7626/25FMCZ to the EVAL-SDP-CH1Z as described in the Evaluation Board Hardware section.

When you first plug in the EVAL-SDP-CH1Z board via the USB cable provided, allow the new **Found Hardware Wizard** to run. Once the drivers are installed, you can check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be accessed via **My Computer> Manage>Device Manager** from the list of **System Tools**. The EVAL-SDP-CH1Z board should appear under **ADI Development Tools**.

This completes the installation.

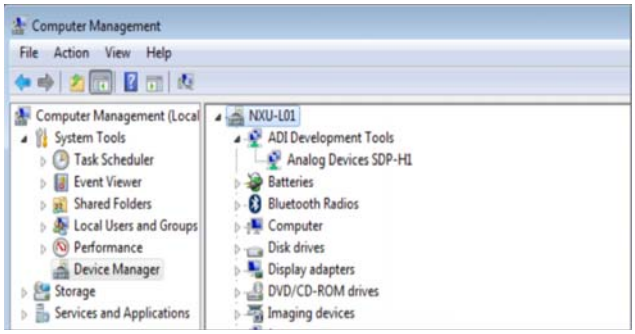

Figure 16. Device Manager

LAUNCHING THE SOFTWARE

Once the EVAL-AD7626/25FMCZ and EVAL-SDP-CH1Z are correctly connected to your PC, the AD7626/25 software can be launched.

1. From the **Start** menu, select **Programs>Analog Devices> AD7626_25 Evaluation Software**. The main window of the software then displays (see Figure 19).
   If the evaluation system is not connected to the USB port via the EVAL-SDP-CH1Z when the software is launched, a connectivity error displays (see Figure 17).
2. Connect the evaluation board to the USB port of the PC.
3. Wait for a few seconds and then click **Rescan** (see Figure 18.

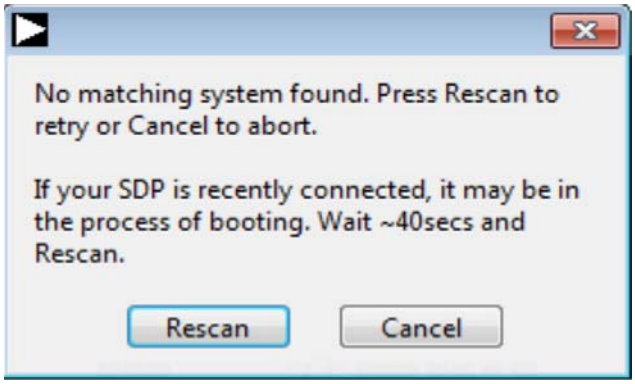

Figure 17. Connectivity Error Alert 1

Figure 18. Connectivity Error Alert 2

SOFTWARE OPERATION

This section describes the full software operation and all windows that appear. When the software is launched, the panel opens and the software searches for hardware connected to the PC. The user software panel launches as shown in Figure 19. The labels listed in this section correspond to the numbered labels in Figure 19.

File Menu (Label 1)

The **File** menu, labeled 1 in Figure 19, offers the choice to

- **Save Captured Data**: saves data to a .csv file
- **Load Captured Data**: loads data for analysis
- **Take Screenshot**: saves the current screen
- **Print:** prints the window to the default printer
- **Exit**: quits the application

Edit Menu (Label 2)

The **Edi**t menu, labeled 2, provides the following offering:

- **Initialize to Default Values**: This option resets the software to its initial state

Help Menu (Label 3)

The **Help** menu, labeled 3, offers help from the

- **Analog Devices website**
- **User Guide**
- **Context Help**
- **About**

Throughput (Label 4)

The default throughput (sampling frequency) is 10,000 kilo samples per second (kSPS) for AD7626, and 6,000 kilo samples per second (kSPS) for AD7625.The user can adjust the sampling frequency, however there are limitations around the sample frequency related to the SCLK frequency applied; the sample frequency must be at least 500 kSPS. If the user enters a value larger than the ability of the ADC (AD7626/25, maximum sample frequency 10M/6M), the software indicates this and the user must revert to the maximum sample frequency.

Samples (Label 5)

Select the number of **Samples** to analyze, when running the software; this number is limited to 1,048,576 samples.

Single Capture (Label 6) and Continuous Capture (Label 7)

Single Capture performs a single capture whereas **Continuous Capture** performs a continuous capture from the ADC.

Eval Board Connected (Label 8)

This indicator shows that the device connected.

Voltage Reference (Label 9)

The various options for using the external reference are controlled by the **Voltage Reference** option. The default value is set to **4.096 V (Internal Reference)**. The other options are **External Reference 4.096V**, **External 1.2V** and **Power Down**. It is recommended to use an on-board AD8031 as an external reference buffer.

PLL Enable (Lable 10)

This option is used when the CNV signal is coming from AD9513, at the same time, you need change the JP1 and JP2 selection to A to center.

Tabs

There are four additional tabs available for displaying the data in different formats.

- Waveform
- Histogram
- FFT
- Summary

To exit the software, go to **File>Exit**.

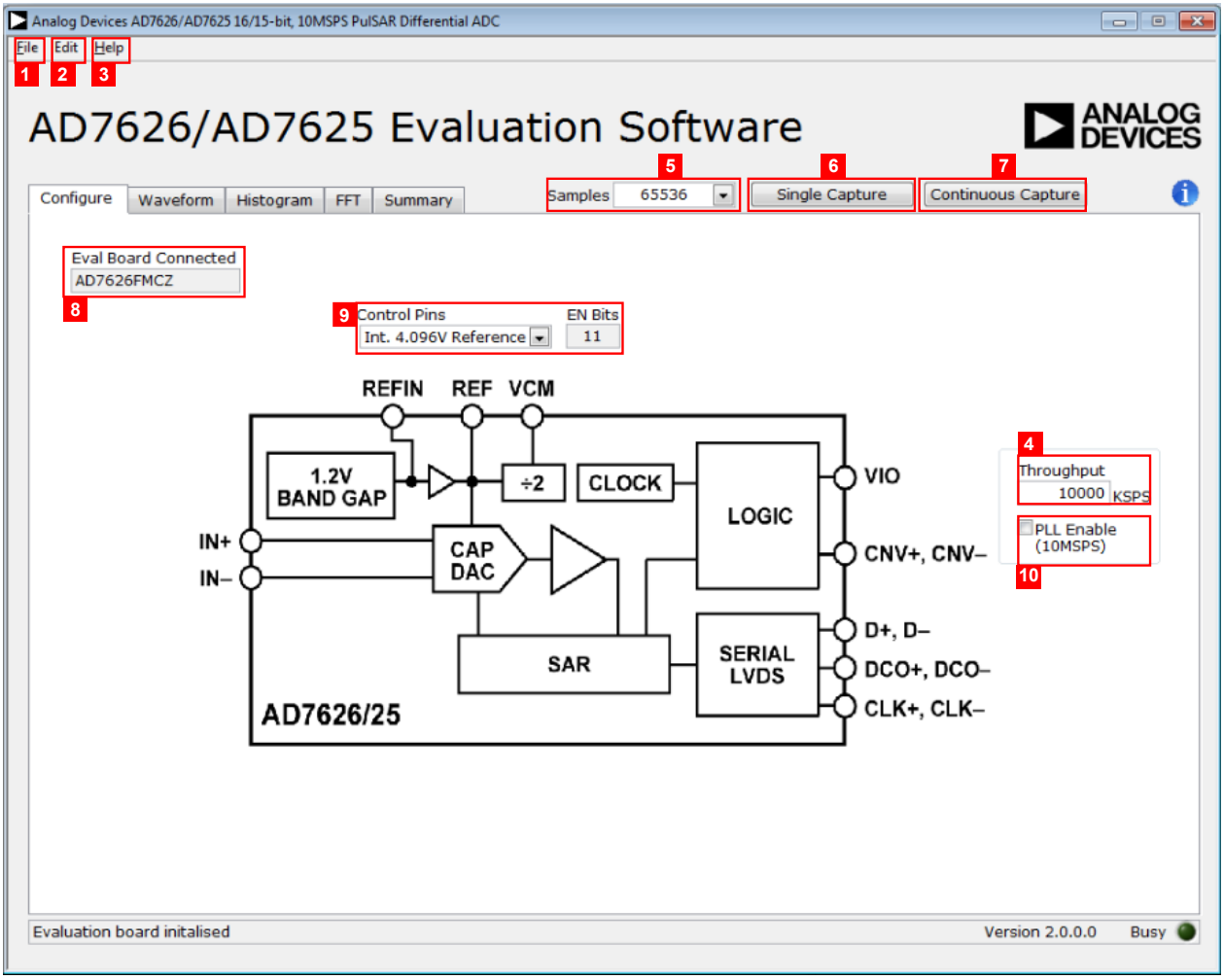

Figure 19. Setup Screen

WAVEFORM CAPTURE

Figure 20 illustrates the Waveform tab. The 20 kHz sine-wave input signal was used along with an on-board 4.096 V external reference.

Note that Label 1 shows the **Waveform Analysis** which reports the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

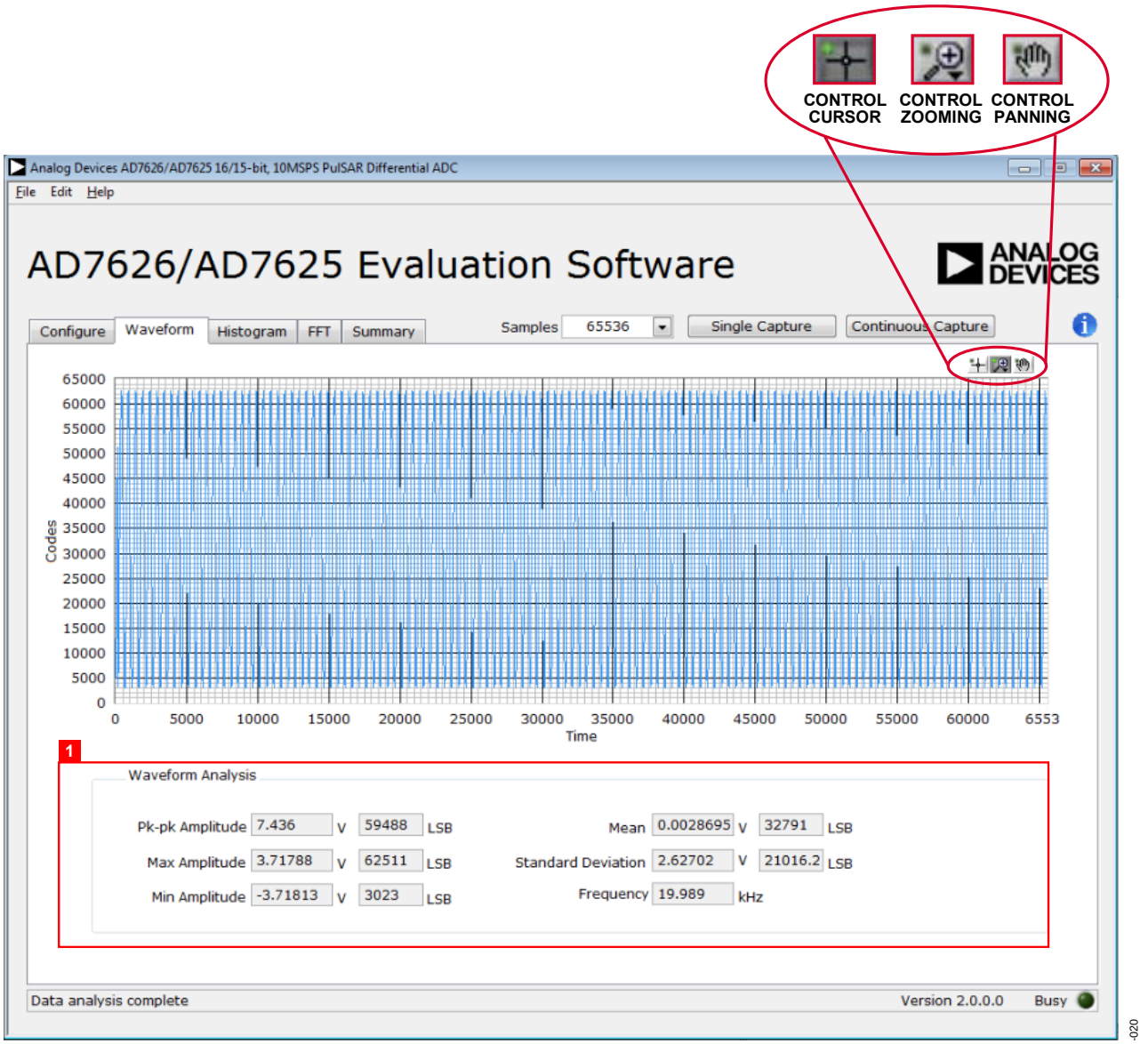

Figure 20. Waveform Capture Tab

DC TESTING—HISTOGRAM

The histogram is most often used for dc testing where a user tests the ADC for the code distribution for dc input and computes the mean and standard deviation, or transition noise, of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test,

1. Select the Histogram tab.
2. Click **Single Capture** or **Continuous Capture**.

Note that a histogram test can be performed without an external source since the evaluation board has a buffered $V_{REF}/2$ source at the ADC input.

To test other dc values, apply a source to the J3/J5 inputs. You may be required to filter the signal to make the dc source noise compatible with that of the ADC.

AC TESTING—HISTOGRAM

Figure 21 shows the Histogram tab. This tests the ADC for the code distribution for ac input and computes the mean and standard deviation, or transition noise, of the converter and displays the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test,

1. Select the Histogram tab.
2. Click **Single Capture** or **Continuous Capture**.

Note that an AC histogram needs a quality signal source applied to the input J3/J5 connectors.

Figure 21 shows the histogram for a 20 kHz sine wave applied to the ADC input and the results calculated.

The **Histogram Analysis** (Label 1) illustrates the various measured values for the data captured.

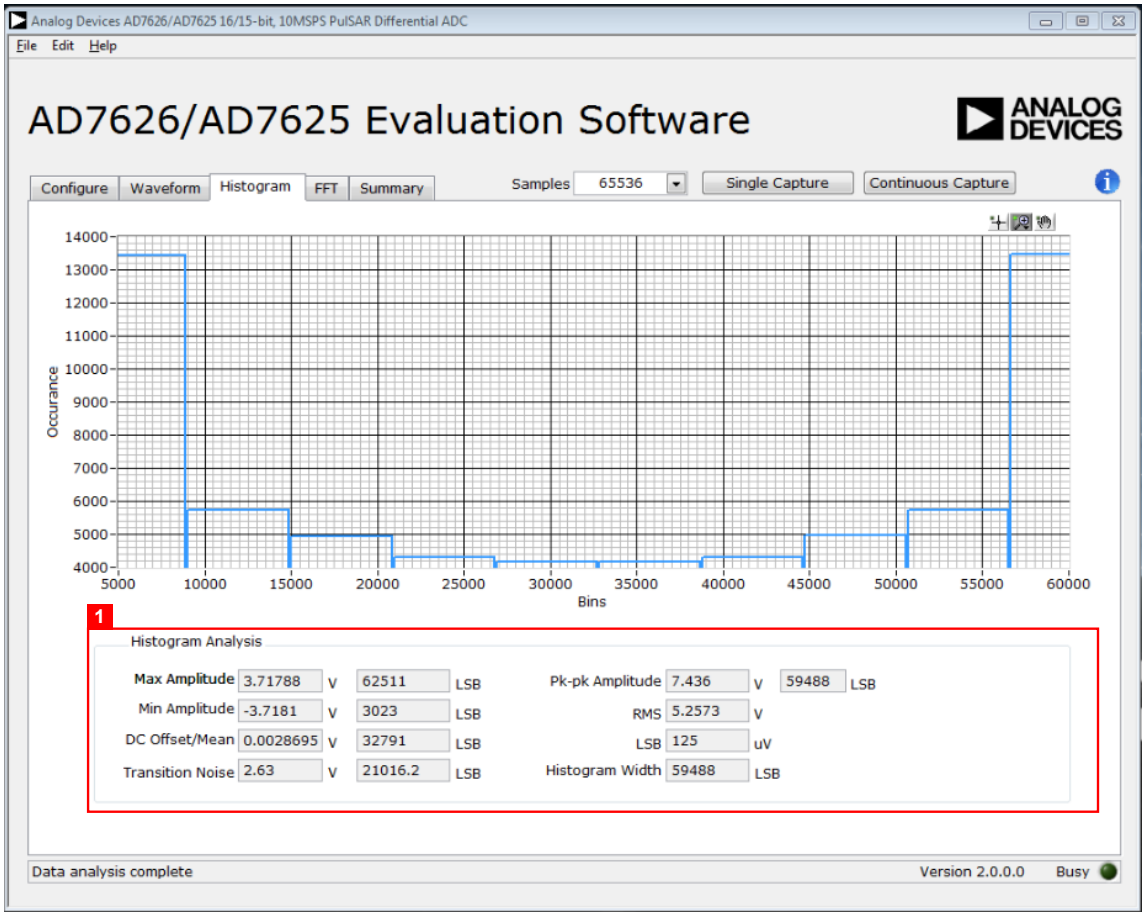

Figure 21. Histogram Capture Tab

AC TESTING—FFT CAPTURE

Figure 22 shows the FFT tab. This tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed displaying SNR, SINAD, THD, and SFDR.

To perform an ac test, apply a sinusoidal signal to the evaluation board at the SMA inputs J3/J5. Very low distortion, better than 130 dB input signal source (such as audio precision) is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but carefully consider the choices.

Furthermore, if using a low frequency band-pass filter when the full-scale input range is more than a few V p-p, it is recommended to use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 22 displays the results of the captured data.

- Shows the input signal information (see Label 1)
- Displays the fundamental frequency and amplitude in addition to the 2^{nd} to 5^{th} harmonics (see Label 2)
- Displays the performance data, including SNR, dynamic range, THD, SINAD, and noise performance (see Label 3)

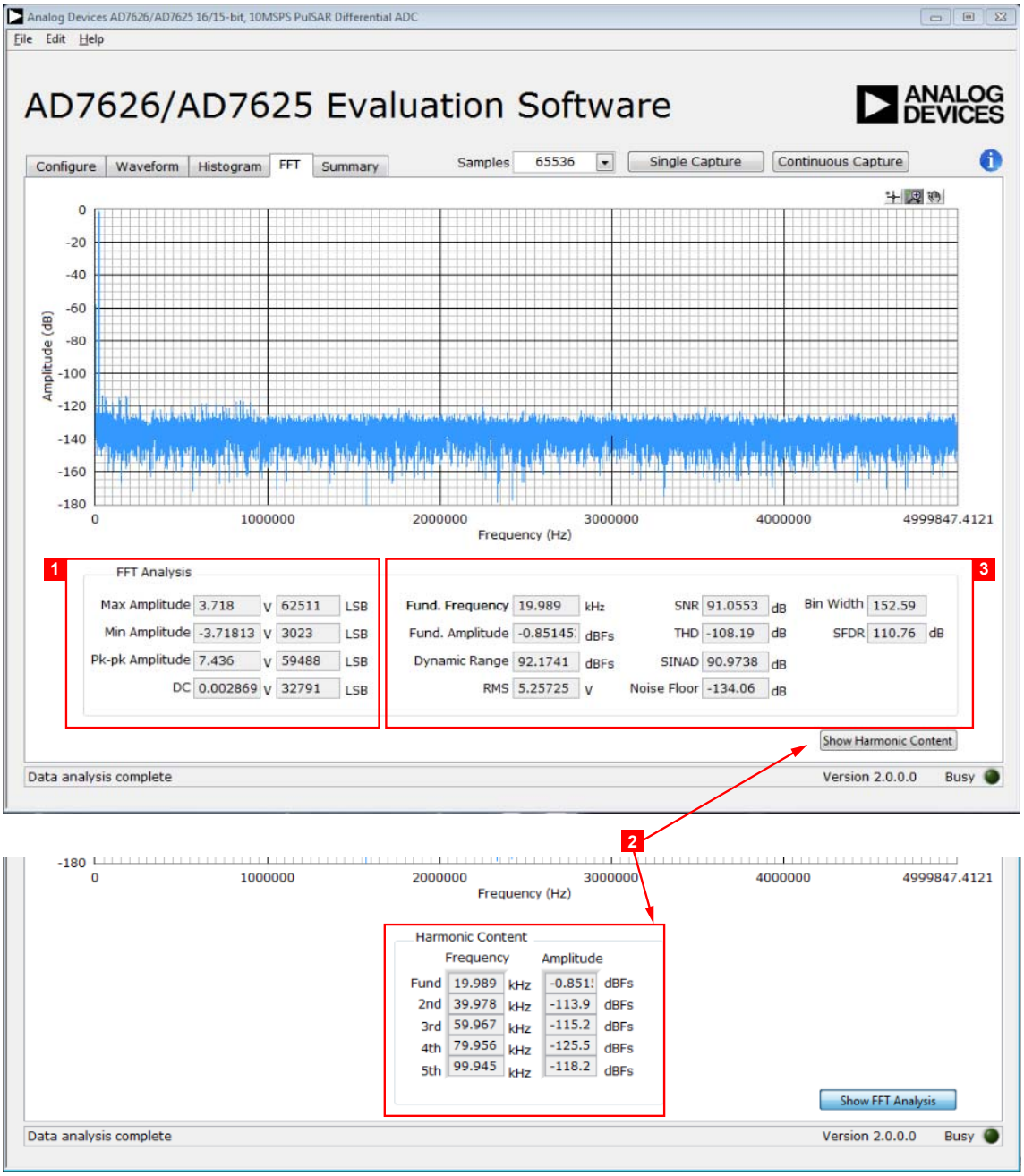

Figure 22. FFT Capture Tab

SUMMARY TAB

Figure 23 shows the Summary tab which captures all the display information and provides it in one panel with a synopsis of the information, including key performance parameters, such as SNR and THD.

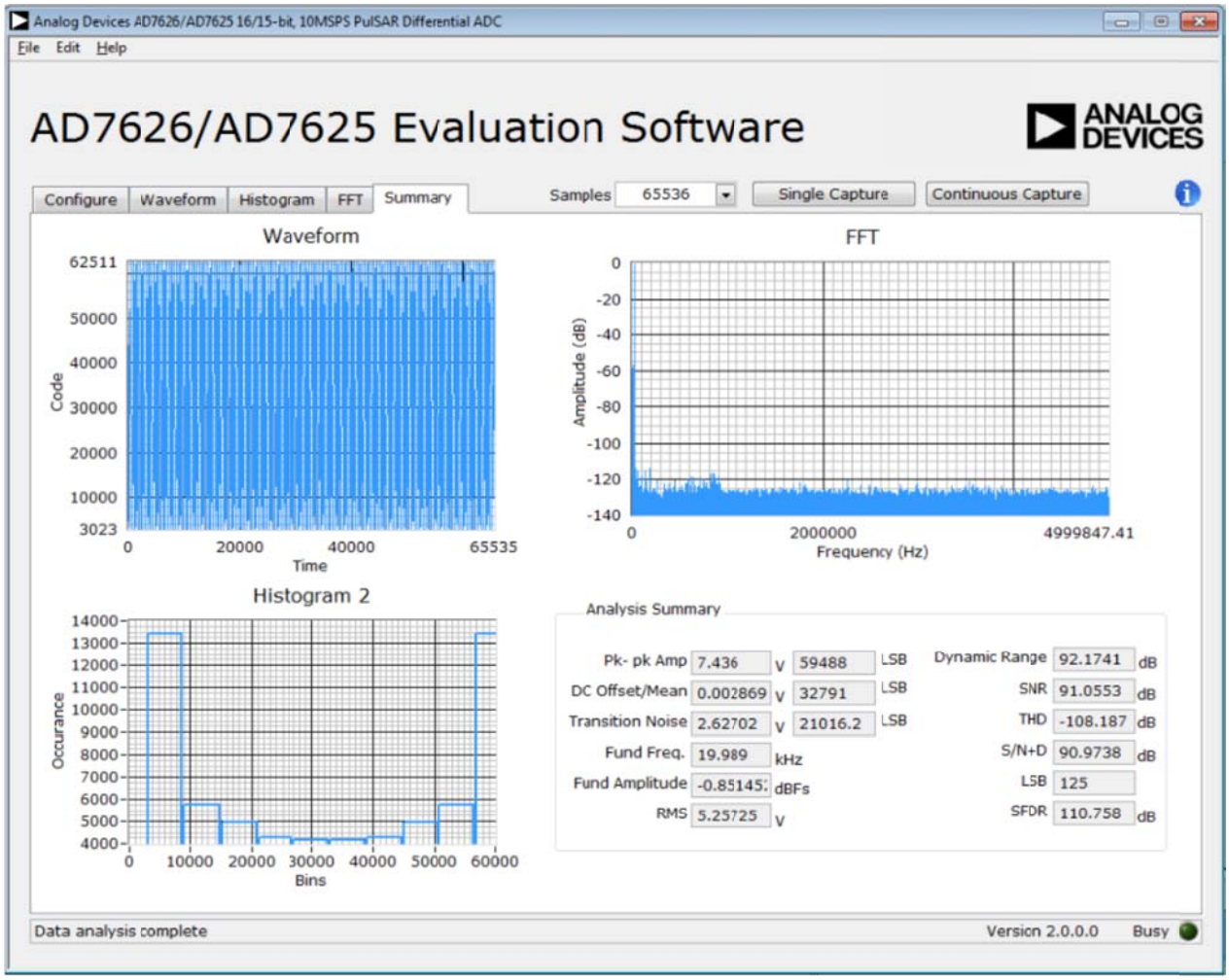

Figure 23. Summary Tab

TROUBLESHOOTING

This section provides hints on how to prevent problems and what to check when you encounter problems with the software and hardware.

SOFTWARE

Review the following points regarding software:

- Always install the software prior to connecting the hardware to the PC.
- Always allow the install to fully complete (the software installation is a two-part process: installing the ADC software and the SDP drivers). This may require a restart.
- When you first plug in the EVAL-SDP-CH1Z board via the USB cable provided, allow the new **Found Hardware Wizard** to run. Though this may take time, do this prior to starting the software.
- If the board does not appear to be functioning, ensure that the ADC evaluation board is connected to the EVAL-SDP-CH1Z board and that the board is recognized in the **Device Manager**, as shown in Figure 7.
- If connected to a slower USB port where the EVAL-SDP-CH1Z cannot read quickly, a timeout error may occur. In this case, it is advised not to read continuously or, alternatively, to lower the number of samples taken.
- Note that when reading continuously from the ADC, the recommended number of samples is up to 1,048,576.

HARDWARE

If the software does not read any data back,

- With the +12 V wall wart plugged in to the EVAL-SDP-CH1Z board, check to make sure that the voltage applied is within the ranges shown in Table 3.
- Using a DMM, measure the voltage present at +12 V and the VADJ test points, which should read +12 V and 2.5 V, respectively. The +12V_FMC LED of the EVAL-AD7626/25FMCZ board and the LEDs of the EVAL-SDP-CH1Z board (FMC_PWR_GO, SYS_PWR, FPGA_DONE, BF_POWER, LED0, and LED2) should all be lit.
- Launch the software and read the data. If nothing happens, exit the software.
- Remove the +12 V wall wart and USB from the EVAL-SDP-CH1Z board and then reconnect them and relaunch the software.
- If this is not successful, confirm that the EVAL-AD7626/25FMCZ and EVAL-SDP-CH1Z boards are connected together so that the EVAL-AD7626/25FMCZ is recognized in the **Device Manager**, as shown in Figure 7.

Note that when working with the software in standalone/offline mode (no hardware connected), if you later choose to connect hardware, first close and then re-launch the software.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).