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This Errata Sheet refers to:

AT91RM9200 devices packaged in 208-lead PQFP or 256-lead BGA with the marking AT91RM9200-CI or AT91RM9200-QI and with the product number 58A07F marked in the bottom left-hand corner of the package.

ARM920T-based Microcontroller

AT91RM9200

Errata Sheet

6015B–ATARM–09/03

36. USART: RS485 Mode, Faulty Description of RTS Pin Behavior in AT91RM9200 Datasheet, Atmel Literature Number 1768B

On page 419 of the datasheet, In the **RS485 Mode** section:

1. "The RTS pin is driven **low** when the trasnmitter is operating."
   Should read:
   "The RTS pin is driven **high** when the transmitter is operating.
2. "Significantly, the RTS pin remains **low** when timeguard is programmed..."
   Should read:
   "Significantly, the RTS pin remains **high** when timeguard is programmed..."
3. Figure 196 and Figure 197 give incorrect descriptions of RTS behavior. The correct descriptions of RTS behavior are as follows:

Figure 196. Typical Connection to a RS485 bus.

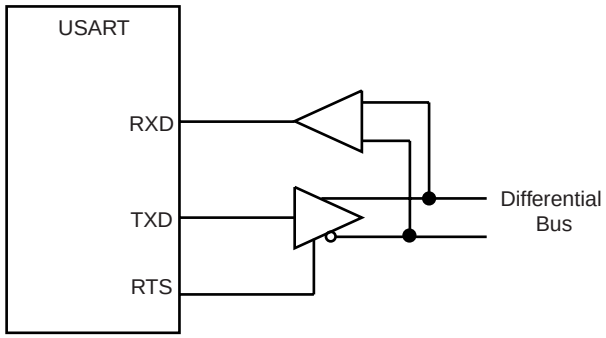
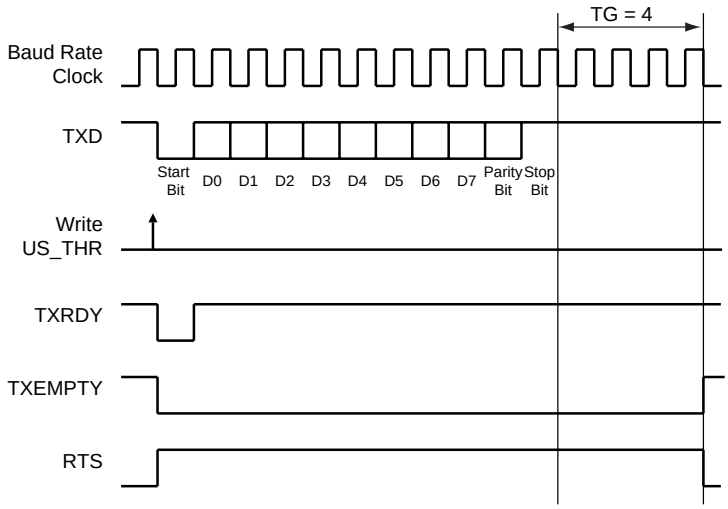


Figure 197. Example of RTS Drive with Timeguard



Problem Fix/Workaround

The correct sentences and correct figures are to be implemented in the next update of the datasheet, Lit° Number 1768C.

35. A24 not wired internally between the EBI and the PIO

A24 is not wired internally between the EBI and the PIO. Use only PIO mode on it.

Problem Fix/Workaround

Due to this error, static memories over 16M bytes per chip select cannot be used. To interface 32-Mbyte memories and over, the user must use two memory chips connected on two different chip selects.

34. Address Bus continuously active

The address bus is continuously driven with the address of the current access, even if it is an internal one.

Problem Fix/Workaround

None.

33. SDRAMC: SDRC_IMR can be written

The Interrupt Mask Register in the SDRAM Controller is not read-only. Thus, writing to it modifies the contents instead of having no effect.

Problem Fix/Workaround

None.

32. No wrap-around for SDRAM devices with two internal banks

In the case of SDRAM devices featuring two internal banks, when the physical address is higher than the memory size, the SDRAM controller does not wrap around. It activates virtual bank numbers three or four.

Problem Fix/Workaround

None.

31. SDRAMC: No t_{RC} after refresh when low-power mode is enabled

When low-power mode is enabled and after a refresh command is sent to the SDRAM, the SDRAM Controller enters low-power mode by asserting SDCKE low. The t_{RC} timing between Auto-refresh and Low-power mode is not respected. As SDCKE is low, the INHIBIT and NOP commands are not sent to the SDRAM.

For the moment this warning has no effect on the correct functionality of the SDRAM.

Problem Fix/Workaround

None.

30. SMC 16-bit write access constraints

When at least two SMC_CSR registers are programmed as follows:

– SMC_SCRx: With wait states (1 < NWS < 127), 16-bit data bus width, and byte write access (BAT field set to 0)

– SMC_CSRy: With wait states (1 < NWS < 127), 16-bit data bus width, and byte select access (BAT field set to 1),

the associated NCSx signal is not asserted for the write access.

Problem Fix/Workaround

For registers programmed with wait states and 16-bit data bus width configuration, the BAT fields in these registers must be programmed with the same value.

29. DBGU: Force NTRST feature not implemented

Writing 1 to DBGU_FNR of the Debug Unit does not prevent access to the processor through the ICE/JTAG.

Problem Fix/Workaround

None.

28. PMC: Constraints on the Master Clock selection sequence

The PMC_MCKR register must not be programmed in a single write operation.

Problem Fix/Workaround

The preferred programming sequence for the PMC_MCKR register is as follows:

1. Program the CSS field in the PMC_MCKR.
2. Wait for the MCKRDY bit to be set in the PMC_SR register.
3. Program the PRES field (in the PMC_MCKR).

An exception to this sequence occurs when the processor clock frequency is greater than the master clock frequency. In this case, the PRES field should be written first.

27. PMC: MCKRDY does not rise in some cases

When re-programming the Master Clock Register, if both fields PRES and CSS are written with the same values as the ones already stored, or if both fields are written with different values than the ones already stored, the status bit MCKRDY does not rise. When one and only one of the fields PRES and CSS is changed, the MCKRDY bit operates normally.

Problem Fix/Workaround

If both fields must be re-programmed, carry out the change in two steps.

26. PMC, Clock Generator: Bad switching when writing PLL registers with same MUL and DIV values

When the fields MUL and DIV in the CKGR_PLLBR register are written with the same values as already programmed, the Master Clock signal switches to Main Clock (output of the Main Oscillator) until a different value is programmed in the register.

When the fields MUL and DIV in the CKGR_PLLAR register are written with the same values as already programmed, the Master Clock signal switches to Slow Clock (output of the 32768 Hz Oscillator) until a different value is programmed in the register.

Problem Fix/Workaround

The user must be sure that either the DIV or MUL field changes when setting the CKGR_PLLBR or CKGR_PLLAR register.

25. TWI: Disabling Does not Operate Correctly

Any transfer in progress is immediately frozen if the Control Register (TWI_CR) is written with the bit MSDIS at 1. Furthermore, the status bits TXCOMP and TXRDY in the Status Register (TWI_SR) are not reset.

Problem Fix/Workaround

The user must wait for the end of transfer before disabling the TWI. In addition, the interrupts must be disabled before disabling the TWI.

24. TWI: NACK Status Bit Lost

During a master frame, if TWI_SR is read between the Non Acknowledge condition detection and the TXCOMP bit rising in the TWI_SR, the NACK bit is not set.

Problem Fix/Workaround

The user must wait for the TXCOMP status bit by interrupt and must not read the TWI_SR as long as transmission is not completed.

Note: TXCOMP and NACK fields are set simultaneously and the NACK field is reset after the read of the TWI_SR.

23. TWI: Possible Receive Holding Register Corruption

When loading the TWI_RHR, the transfer direction is ignored. The last data byte received in the TWI_RHR is corrupted at the end of the first subsequent transmit data byte. Neither RXRDY nor OVERRUN status bits are set if this occurs.

Problem Fix/Workaround

The user must be sure that received data is read before transmitting any new data.

22. TWI: Clock Divider Limitation

The CKDIV field on the Clock Waveform Generator (TWI_CWGR) has a maximum value of 0x5.

Problem Fix/Workaround

None.

21. SSC: Receiver does not take into account a start condition while receiving data

The SSC receiver does not support reception of the last data sequence of a frame that overlaps a new start of frame, regardless of the mode of detection of the start condition. For example, this prevents reception of the last data of a TDM bus.

Problem Fix/Workaround

None.

20. SSC: RXSYN and TXSYN not cleared when read

The status bits RXSYN and TXSYN are active during a complete serial clock period and are not immediately cleared when SSC_SR is read.

Problem Fix/Workaround

The user must enable the interrupt relevant to RXSYN and TXSYN.

19. SSC: Receiver Speed Limitations

– If RF is programmed as input, the maximum clock frequency is MCK divided by 2.
– If RF is programmed as output and RK is programmed as input, the maximum clock frequency is MCK divided by 6.
– If RF and RK are both programmed as output, the maximum clock frequency is MCK divided by 4.

Problem Fix/Workaround

None.

18. SSC: Transmitter Speed Limitations

– If both TF and TK are programmed as output, the maximum clock frequency is MCK divided by 4.
– If TF is programmed in output and TK is programmed as input, the maximum clock frequency is MCK divided by 8.
– If both TF and TK are programmed as input, the maximum clock frequency is MCK divided by 8.
– If TF is programmed in input and TK is programmed as output, the maximum clock frequency is MCK divided by 4.

Problem Fix/Workaround

None.

17. Disabling the SSC does not stop the Frame Synchronization signal generation

Generating RF can be stopped only by programming the FSOS field in SSC_RFMR to 0x0.

Generating TF can be stopped only by programming the FSOS field in SSC_TFMR to 0x0.

Problem Fix/Workaround

None.

16. SSC: No delay when start condition overlays data transmit

When transmission of data is programmed at the end of a frame and the start condition of the following frame is detected at the end of the current frame, the delay programmed by the STTDLY bit (in the SSC_RCMR and in the SSC_TCMR registers) is not performed on the next frame. Transmission starts immediately regardless of the programming of the field STTDLY.

Problem Fix/Workaround

None.

15. SPI: Slave Mode Receiver does not mask the highest data bits

If the SPI receives a frame followed by 8 bits of data, the user needs to mask the highest byte of the Receive Holding Register, as this data may be incorrect and not 0.

Problem Fix/Workaround

The user should implement the PDC. If the PDC is not implemented, the user should mask the highest byte of the Receive Holding register.

14. SPI: No chip select configuration change before end of current transfer

If the SPI is programmed in Master Mode and in Fixed Peripheral Mode, and data is being sent to a slave, the user has to wait for completion of the transfer before changing the slave number. Programming a new slave number (PCS) and/or a new DLYBCS field locks the SPI on the current slave.

Problem Fix/Workaround

The user should use the Variable Peripheral Mode.

13. SPI: NPCSx rises if no data is to be transmitted

If the SPI has sent all the data written in the SPI_TDR, the current NPCS rises immediately. This might be inconvenient in the case of several SPI peripherals requiring their chip select line to remain active until a complete data buffer has been transmitted. The PDC channel may be late in providing data to be transmitted when bus latencies are too high.

Problem Fix/Workaround

For high-speed applications, the relevant PIO pins can be used to manage the data transmission.

12. PIO: Output Data Status Register is always Read/Write

The programming of the register PIO_OWSR has no effect on the read/write features of PIO_ODSR, which is always read/write accessible.

Problem Fix/Workaround

None.

11. EMAC: Using Receive frames and buffers not word-aligned

The Ethernet MAC in Receiver Mode allows word-aligned receive frames and buffers. When using receive frames and receive buffers which are not word-aligned, the pointer is not de-asserted and a new valid pointer cannot be set for the next frame. The next receive frame can be rejected even if the pointer is freed.

Problem Fix/Workaround

When using frames that are not word-aligned, the user must disable and re-enable the RE field of the Ethernet Control Register (ETH_CTL) each time a buffer is unavailable.

10. TC: Wrong Compare at restart if burst low

If the counter was stopped or disabled, unwanted Compare RA, RB or RC may occur at restart if the clock selected by the counter is masked by a low selected burst input when the trigger event is recognized at the selected clock active edge. All compare effects are affected, as the flags are set incorrectly and CPC trigger, CPC stop or CPC disable may occur.

Problem Fix/Workaround

None.

9. TC: Wrong 0 captured before Compare RC trigger

A wrong 0 is captured in RA or RB during the last selected counter clock period if CPCTRG is active and the capture event occurred at least one Master Clock cycle after the last counter value update.

Problem Fix/Workaround

None.

8. TC: Erroneous capture with burst low

The value captured is not equal to the Counter Value if the selected burst input is low at capture time, i.e., at the selected clock active edge where the capture event is recognized.

The captured value may be 0; otherwise, it is the Counter Value plus one instead of the Counter Value.

Problem Fix/Workaround

None.

7. TC: Bad capture at restart if burst low

The captured value is not zero if burst is low when the preceding trigger event is recognized. Instead, the captured value is the Counter Value before the trigger.

Problem Fix/Workaround

None.

6. TC: TIOA and TIOB outputs stuck in case of simultaneous events

In the register TC_CMR, if at least one of the fields ASWTRG or AEEVT or ACPC is set to 0x0 (none), the event programmed by ACPA is not carried out.

In the register TC_CMR, if at least one of the fields ASWTRG or AEEVT is set to 0x0 (none), the event programmed by ACPC is not carried out.

In the register TC_CMR, if the field ASWTRG is set to 0x0 (none), the event programmed by AEEVT is not carried out.

The same problem exists on the TIOB output with the fields BSWTRG, BEEVT, BCPC and BCPB.

Problem Fix/Workaround

An order of priority for TIOA and/or TIOB events must be defined depending on the user application.

5. TC: TIMER_CLOCK2 not sampled on same edge as TIMER_CLOCK0 and TIMER_CLOCK1

TIMER_CLOCK2/TIMER_CLOCK5 is sampled on the system clock falling edge of Master Clock, whereas TIMER_CLOCK0/TIMER_CLOCK3 and TIMER_CLOCK1/TIMER_CLOCK4 are sampled on the rising edge of Master Clock. This should not have any effect on the functional operations of the Timer Counter unless the Timer Counter is used at its speed limit.

Problem Fix/Workaround

None.

4. TC: Triggers do not clear the counter in Up/Down Mode

When the field WAVESEL in TC_CMR is at value 0x2 or 0x3, the triggers do not reset the counter value. The counter value can be reset only by modifying the field WAVESEL.

Problem Fix/Workaround

None.

3. TC: Triggers in Up/Down Mode are lost when burst signal is active

When the field WAVESEL in TC_CMR is at value 0x2 or 0x3, the triggers occurring while the selected burst signal is active (clock disabled) are not taken into account.

Problem Fix/Workaround

None.

2. TC: Clock Selection Limitation in Up/Down Mode

Selecting the Master Clock or the Master Clock divided by 2 as the Timer Counter Clock may lead to unpredictable result when the field WAVESEL in TC_CMR is at value 0x2 or 0x3.

Problem Fix/Workaround

None.

1. TC: Spurious counter overflow in Up/Down Mode

When the field WAVESEL in TC_CMR is at value 0x2 or 0x3 and when the counter reaches the value 0xFFFF, it inverts its sense and decrements to 0xFFFE. At the same time, the OVF bit in TC_SR is set.

Problem Fix/Workaround

None.

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