The ExpressLane™ PEX8714 device offers Multi-Host PCI Express switching capability enabling users to connect multiple hosts to their respective endpoints via scalable, high bandwidth, non-blocking interconnection to a wide variety of applications including servers, storage systems, and communications platforms. The PEX8714 is well suited for fan-out, aggregation, and peer-to-peer applications.

Multi-Host Architecture
The PEX8714 employs an enhanced architecture, which allows users to configure the device in legacy single-host mode or multi-host mode with up to two host ports by using NT capability. This powerful architectural enhancement enables users to build PCIe based systems to support high-availability, failover, redundant and clustered systems.

High Performance & Low Packet Latency
The PEX8714 architecture supports packet cut-thru with a maximum latency of 158ns (x4 to x4). This, combined with large packet memory, flexible common buffer/FC credit pool and non-blocking internal switch architecture, provides full line rate on all ports for performance-hungry applications such as servers and switch fabrics. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the device supports a packet payload size of up to 2048 bytes, enabling the user to achieve even higher throughput.

Data Integrity
The PEX8714 provides end-to-end CRC (ECRC) protection and Poison bit support to enable designs that require end-to-end data integrity. PLX also supports data path parity and memory (RAM) error correction circuitry throughout the internal data paths as packets pass through the switch.

Flexible Configuration
The PEX8714’s 5 ports can be configured to lane widths of x2, x4, or x8. Flexible buffer allocation, along with the device's flexible packet flow control, maximizes throughput for applications where more traffic flows in the downstream, rather than upstream, direction. Any port can be designated as the upstream port, which can be changed dynamically. Figure 1 shows some of the PEX8714’s common port configurations in legacy Single-Host mode.
The PEX8714 also provides several ways to configure its registers. The device can be configured through strapping pins, I²C interface, host software, or an optional serial EEPROM. This allows for easy debug during the development phase, performance monitoring during the operation phase, and driver or software upgrade.

**Dual-Host & Failover Support**

In Single-Host mode, the PEX8714 supports a **Non-Transparent (NT) Port**, which enables the implementation of dual-host systems for redundancy and host failover capability. The NT port allows systems to isolate host memory domains by presenting the processor subsystem as an endpoint rather than another memory system. Base address registers are used to translate addresses; doorbell registers are used to send interrupts between the address domains; and scratchpad registers (accessible by both CPUs) allow inter-processor communication (see Figure 3).

**Hot-Plug for High Availability**

Hot plug capability allows users to replace hardware modules and perform maintenance without powering down the system. The PEX8714 Hot-Plug capability feature makes it suitable for **High Availability (HA) applications**. One downstream ports include a Standard Hot Plug Controller. If the PEX8714 is used in an application where one or more of its downstream ports connect to PCI Express slots, each port’s Hot-Plug Controller can be used to manage the Hot-Plug event of its associated slot. Every port on the PEX8714 is equipped with a Hot-Plug control/status register to support Hot-Plug capability through external logic via the I²C interface.

**SerDes Power and Signal Management**

The PEX8714 supports software control of the SerDes outputs to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical, and high. The SerDes block also supports **loop-back modes** and **advanced reporting of error conditions**, which enables efficient management of the entire system.

**Interoperability**

The PEX8714 is designed to be fully compliant with the PCI Express Base Specification r3.0, and is backwards compatible to PCI Express Base Specification r1.1 and r1.0a. Additionally, it supports **auto-negotiation**, **lane reversal**, and **polarity reversal**. Furthermore, the PEX8714 is tested for Microsoft Windows Logo compliance. All PLX switches undergo thorough interoperability testing in PLX’s **Interoperability Lab** and **compliance testing at the PCI-SIG plug-fest**.
performancePAK™
Exclusive to PLX, performancePAK is a suite of unique and innovative performance features which allows PLX’s Gen 3 switches to be the highest performing Gen 3 switches in the market today. The performancePAK features consists of Multicast, and Dynamic Buffer Pool.

SSC Isolation
The PEX8714 employs a multi-clock domain which allows the user to terminate Spread Spectrum Clock enabled domains. Terminating the SSC clock removes the need to pass a common clock across a backplane. The PEX8714 supports SSC isolation on four of its ports.

visionPAK™
Another PLX exclusive, visionPAK is a debug diagnostics suite of integrated hardware and software instruments that users can use to help bring their systems to market faster. visionPAK features consist of Performance Monitoring, SerDes Eye Capture, Error Injection, SerDes Loopback, and more.

Performance Monitoring
The PEX8714’s real time performance monitoring allows users to literally “see” ingress and egress performance on each port as traffic passes through the switch using PLX’s Software Development Kit (SDK). The monitoring is completely passive and therefore has no affect on overall system performance. Internal counters provide extensive granularity down to traffic & packet type and even allows for the filtering of traffic (i.e. count only Memory Writes).

SerDes Eye Capture
Users can evaluate their system’s signal integrity at the physical layer using the PEX8714’s SerDes Eye Capture feature. Using PLX’s SDK, users can view the receiver eye of any lane on the switch. Users can then modify SerDes settings and see the impact on the receiver eye. Figure 5 shows a screenshot of the SerDes Eye Capture feature in the SDK.

Figure 3. SerDes Eye Capture

Error Injection & SerDes Loopback
Using the PEX8714’s Error Injection feature, users can inject malformed packets and/or fatal errors into their system and evaluate a system’s ability to detect and recover from such errors. The PEX8714 also supports Internal Tx, External Tx, Recovered Clock, and Recovered Data Loopback modes.

Applications
Suitable for host-centric as well as peer-to-peer traffic patterns, the PEX8714 can be configured for a wide variety of form factors and applications.

Host Failover
The PEX8714 can also be utilized in applications where host failover is required. In the below application (Figure 8), two hosts may be active simultaneously and controlling their own domains while exchange status information through doorbell registers or I2C interface. The devices can be programmed to trigger fail-over if the heartbeat information is not provided. In the event of a failure, the surviving device will reset the endpoints connected to the failing CPU and enumerate them in its own domain without impacting the operation of endpoints already in its domain.

Figure 4. Host Fail-Over
Software Usage Model

From a system model viewpoint, each PCI Express port is a virtual PCI to PCI bridge device and has its own set of PCI configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The virtual PCI to PCI bridges within the PEX8714 are compliant to the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI to PCI bridge are accessible by type 0 configuration cycles through the virtual primary bus interface (matching bus number, device number, and function number).

Interrupt Sources/Events

The PEX8714 switch supports the INTx interrupt message type (compatible with PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by PEX8714 for hot plug events, doorbell interrupts, baseline error reporting, and advanced error reporting.

Development Tools

PLX offers hardware and software tools to enable rapid customer design activity. These tools consist of a hardware module (PEX8714 RDK), hardware documentation (available at www.plxtech.com), and a Software Development Kit (also available at www.plxtech.com).

ExpressLane PEX8714 RDK

The PEX8714 RDK is a baseboard RDK containing the PEX8714 and multiple PCIe slots for connecting endpoints. The PEX8714 RDK can be used to test and validate customer software, or used as an evaluation vehicle for PEX8714 features and benefits. The PEX8714 RDK provides everything that a user needs to get their hardware and software development started.

Software Development Kit (SDK)

PLX’s Software Development Kit is available for download at www.plxtech.com/sdk. The software development kit includes drivers, source code, and GUI interfaces to aid in configuring and debugging the PEX8714.

Both performancePAK and visionPAK are supported by PLX’s RDK and SDK, the industry’s most advanced hardware- and software-development kits.

Product Ordering Information

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<tr>
<th>Part Number</th>
<th>Description</th>
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<tr>
<td>PEX8714-AB80B1G</td>
<td>12-Lane, 5-Port PCI Express Gen 3 Switch, Pb-Free (19x19mm²)</td>
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<tr>
<td>PEX8714-AA RDK</td>
<td>PEX8714 Rapid Development Kit</td>
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