S25FL128S
S25FL256S

SUPPLEMENT

128 Mbit (16 Mbyte) and 256 Mbit (32 Mbyte), 3 V, MirrorBit® Flash

General Description

This supplementary document provides information on a device designed for limited distribution. It describes how the features, operation, and ordering options of this device have been enhanced or changed from the standard device on which it is based. The information contained in this document modifies any information on the same topics established by the data sheets listed in the Affected Documents/Related Documents table and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the S25FL128S and S25FL256S data sheets. It is intended for hardware system designers and software developers of applications, operating systems, or tools.

Affected Documents/Related Documents

Title	Spansion Publication Number	Cypress Document Number
S25FL128S and S25FL256S Data Sheet	S25FL128S_256S_00	001-98283

1. Device Description

1.1 Permanent Lock Description

The Secure Model devices offer a unique Permanent Lock feature that allows the host system to permanently secure data in the memory array. Initiating this locking feature makes the selected block protection scheme permanent, thereby disabling both program and erase operations in the protected region of the array.

1.2 Advanced Sector Protection Description

The secure model devices modify the Advanced Sector Protection (ASP) features:

- All Dynamic Protection Bits (DYB) are modified to be in the protected state following power-up
- All Persistent Protection Bits (PPB) are modified to be One Time Programmable (OTP). After a PPB bit is programmed, the related sector is permanently protected. PPB bits are not erasable. PPB bits may be programmed while the PPBLOCK Bit = 0.

2. Registers

2.1 Configuration Register 1 (CR1)

Bit 4 called LOCK is added to CR1. When set to 1, the Block Protection configuration is permanent.

Configuration Register (CR1)

Bits	Field Name	Function	Default State	Description
7	LC1	Latency Code	0	Selects number of initial read latency cycles. See Latency Code Tables.
6	LC0		0	
5	TBPROT	Configures Start of Block Protection and selects readable boot sector in Read Password Mode	0	1 = BP starts at bottom (Low address) 0 = BP starts at top (High address)
4	LOCK	Permanently locks BP2-0 and TBPROT bits in their state when LOCK is set to 1	0	1 = Locked 0 = Un-locked
3	BPNV	Configures BP2-0 in Status Register	0	1 = Volatile 0 = Non-Volatile
2	TBPARM	Configures Parameter Sectors location	0	1 = 4 kB physical sectors at top (High address) 0 = 4 kB physical sectors at bottom (Low address) RFU in uniform sector devices.
1	QUAD	Puts the device into Quad I/O operation	0	1 = Quad 0 = Dual or Serial
0	FREEZE	Lock current state of BP2-0 bits in Status Register, TBPROT, and TBPARM in Configuration Register, and OTP regions	0	1 = Block Protection and OTP locked 0 = Block Protection and OTP un-locked

2.2 ASP Register (ASPR)

Bits 3 and 4 are added to make PPB bits OTP and DYB bits default to protected state following power-up.

ASP Register (ASPR)

Bits	Field Name	Function	Default State	Description
15 to 9	RFU	Reserved	1	Reserved for Future Use
8	RFU	Reserved	0	Reserved for Future Use
7	RFU	Reserved	0	Reserved for Future Use
6	RFU	Reserved	1	Reserved for Future Use
5	RFU	Reserved	1	Reserved for Future Use
4	DYBLBB	DYB Lock Boot Bit	0	0 = All DYB power-up in the protected state (0)
3	PPBOTP	PPB OTP Bit	0	0 = PPB bits are OTP
2	PWDMLB	Password Protection Mode Lock Bit	1	0 = Password Protection Mode permanently enabled. 1 = Password Protection Mode not permanently enabled.
1	PSTMLB	Persistent Protection Mode Lock Bit	1	0 = Persistent Protection Mode permanently enabled. 1 = Persistent Protection Mode not permanently enabled.
0	RFU	Reserved	1	Reserved for Future Use

3. Block Protection

3.1 Lock Bit

Bit 4 of the Configuration Register is the LOCK bit. When the LOCK bit is programmed to a 1 the BP2-0 bits in the Status Register and the TBPROT bit in the Configuration Register are permanently locked to their nonvolatile values, they cannot be erased or programmed; thereby permanently locking the selected portion of the memory array from change by programming or erasure. The FREEZE bit and BPNV bits in the Configuration Register no longer affect the BP2-0 bits, because the LOCK bit has permanently frozen the BP2-0 bits in their non-volatile state. Any attempt to change the BP bits with the WRR command while LOCK = 1 is ignored and no error status is set. The LOCK bit is a one-time programmable value, so once set it cannot be changed back.

4. Advanced Sector Protection

4.1 ASP Register

The ASP register is used to permanently configure the behavior of Advanced Sector Protection (ASP) features.

The ASPR[4] DYB Lock Boot Bit is shipped from the factory as 0, which means all the DYB are powered up in the Protected State.

The ASPR[3] PPB OTP Bit is shipped from the factory as 0, which means all the PPB bits are One Time Programmable. Once a PPB bit is programmed to 0, the related sector is permanently protected.

The PPBLOCK bit controls when PPB bits are programmable or protected as described in the standard device models data sheet. The Persistent and Password protection modes control the PPBLOCK bit state as described in the standard device models data sheet.

4.2 Read Password Protection Mode

If enabled the Read Password Method is a security option that will replace the default PPB Password Protection Mode. The Read Password Protection Mode enables protecting the main Flash array from read, program and erase. Only the lowest or highest address range, selected by the configuration register TBPROT bit, remains readable until a successful Password Unlock command is completed.

In this mode the PPB Lock bit is used to control the high order bits of address. When the PPB Lock bit is 1, the address bits operate normally. When the PPB Lock bit is 0, the address bits that select a main array sector address range are forced either to Zeros

(TBPROT = 0) or to Ones (TBPROT = 1) to select the lowest or highest address main Flash array address range per the table below. When TBPROT is cleared to a 0, the bottom (zero address) 64 kB or 256 kB of the array is readable. When TBPROT is set to a 1, the top (maximum address) 64 kB or 256 kB of the array is readable. The selection of 64 kB or 256 kB depends on the OPN selection for size of the sector erase command.

Sector size option	TBPARM = 0 (bottom of the chip)		TBPARM = 1 (top of the chip)	
	TBPROT = 0	TBPROT = 1	TBPROT = 0	TBPROT = 1
64 kB (Hybrid)	User is confined to the lowest address sixteen 4 kB sectors.	User is confined to the highest address 64 kB sector	User is confined to the lowest address 64 kB sector	User is confined to the highest address sixteen 4 kB sectors
256 kB (Uniform) TBPARM is ignored	User is confined to the lowest address sector	User is confined to highest address sector	User is confined to the lowest address sector	User is confined to highest address sector

This address range selection is independent of the bank address register. The Bank Address Register remains at the default value of zero. The BRWR command does not work during read password mode so the user must be aware to set the BAR to the desired address immediately after the password unlock to normal read mode.

The PPB bits are protected from program and erase when PPB Lock is 0 and may be programmed or erased when PPB Lock is 1.

The PPB Lock bit is set to 0 by power-on reset or hardware reset — same as in PPB Password Protection Mode.

Read Password Protection Notes:

1. The user can program the ASPR[5] bit to 0 and use read password, or not, as desired.
2. The command sequence for programming, reading, and locking of the Password for Read Password Method is the same as the default for the PPB Password Method.
3. When the Read Password Mode and Password Protection Mode are enabled (i.e. ASPR[2] and ASPR[5] are programmed to 0), then all addresses are redirected to the Boot Sector until the password unlocking sequence is properly entered, with the correct password. At which time, the Read Password Mode is disabled and all addressing will select the proper location.
4. If a system hardware reset occurs, then the Read Password Mode is re-enabled.
5. ASPR[5] is used to select between Read Password vs. PPB Password options. If ASPR[5]=0 then the device is ready for Read Password. However, Read Password is not enabled until ASPR[2]=0. At which point, all addresses select only within the top or bottom sectors, until the device is unlocked with the proper unlocking sequence and Password. When ASPR[2] is not = 1 the addresses select normally. This allows users to program in code, test it, provide a password, and then lock it by programming ASPR[2]= 0.
6. The PLBWR command has undefined results if sent when Read Password Protection is in use. The PPB Lock bit may only be returned to 0 by a hardware reset or power-on reset.
7. Only the read commands and the Password Unlock command are valid during Read Password Mode while the PPB Lock bit = 1. Other commands are disabled until the password is supplied to enable reading of the entire device and normal command operation.
8. When Read Password Protection mode is active (ASPR[5]=0, ASPR[2]=0, PPB Lock = 0), reading of the main array is allowed but forced to have only the boot sector visible via the forcing of memory sector address to zero or ones. Reading the OTP, DYB, and PPB address space returns undefined data.
9. Programming memory spaces or writing registers is not allowed when Read Password Protection mode is active. The WRR, WRDI, WREN, ABWR, BRWR, ASPP, CLSR, OTPP, PNVDLR, WVDLR, PLBWR, DYBWR, PPBP, PPBE and PASSP commands do not change memory or register state when Read Password Protection mode is active. RESET operates normally, and bus protocol may be modified by resetting mode bits.
10. AutoBoot is disabled when the Read Password feature is enabled, as part of the ASP. This removes any conflicts when the AutoBoot address is within the Protected Area. The user won't be able to AutoBoot since a password is required prior to addressing the "boot" code. Cypress recommends that the ABE Bit 0 should be cleared to 0 when the Read Password feature is enabled.
11. All ID Read commands - ABh, 90h, 9Fh, and 5Ah (FL512S only) - are enabled and can be used when the device is in Read Password Protection mode.

12. The BRAC and WRR combined command sequence is illegal when Read Password mode is active, prior to the password being provided.

5. Commands

5.1 Reset Commands

5.1.1 Software Reset Command (RESET F0h)

The Software Reset command (RESET) restores the device to its initial power up state, except for the volatile FREEZE bit in the Configuration register CR1[1] and the volatile PPB Lock bit in the PPB Lock Register. The Freeze bit and the PPB Lock bit will remain set at their last value prior to the software reset. To clear the FREEZE bit and set the PPB Lock bit to its protection mode selected power on state, a full power-on reset sequence or hardware reset must be done. Note that all bits in the configuration register retain their previous state after a Software Reset. The Block Protection bits BP2, BP1, and BP0, in the status register will only be reset if they are configured as volatile via the BPNV bit in the Configuration Register (CR1[3]) and FREEZE (CR1[0]) is cleared to zero and LOCK (CR1[4]) is cleared to zero. The software reset cannot be used to circumvent the FREEZE or PPBLOCK bit protection mechanisms for security configuration bits (SR1[4:2], CR1[5:2], and PPB bits). The reset command is executed when CS# is brought to high state and requires t_{RPH} time to execute.

In case of power-up failure, if the user applies a RESET command, a full power up sequence is triggered. Meanwhile program and erase commands are ignored.

6. Software Interface Reference

6.1 Device ID and Common Flash Interface (ID-CFI) Address Map

CFI Alternate Vendor-Specific Extended Query Parameter 88h Data Protection

Parameter Relative Byte Address Offset	Data	Description
00h	88h	Parameter ID (Data Protection)
01h	04h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter)
02h	0Ah	OTP size 2^N bytes, FFh = not supported
03h	01h	OTP address map format, 01h = FL-S format, FFh = not supported
04h	02h	Block Protect Type, model dependent 00h = FL-P, FL-S, FFh = not supported, 02h = FL-S Lock Bit Enabled
05h	03h	Advanced Sector Protection type, model dependent 01h = FL-S ASP, 03h = FL-S ASP with DYB Lock Boot and PPBOTP

6.2 Initial Delivery State

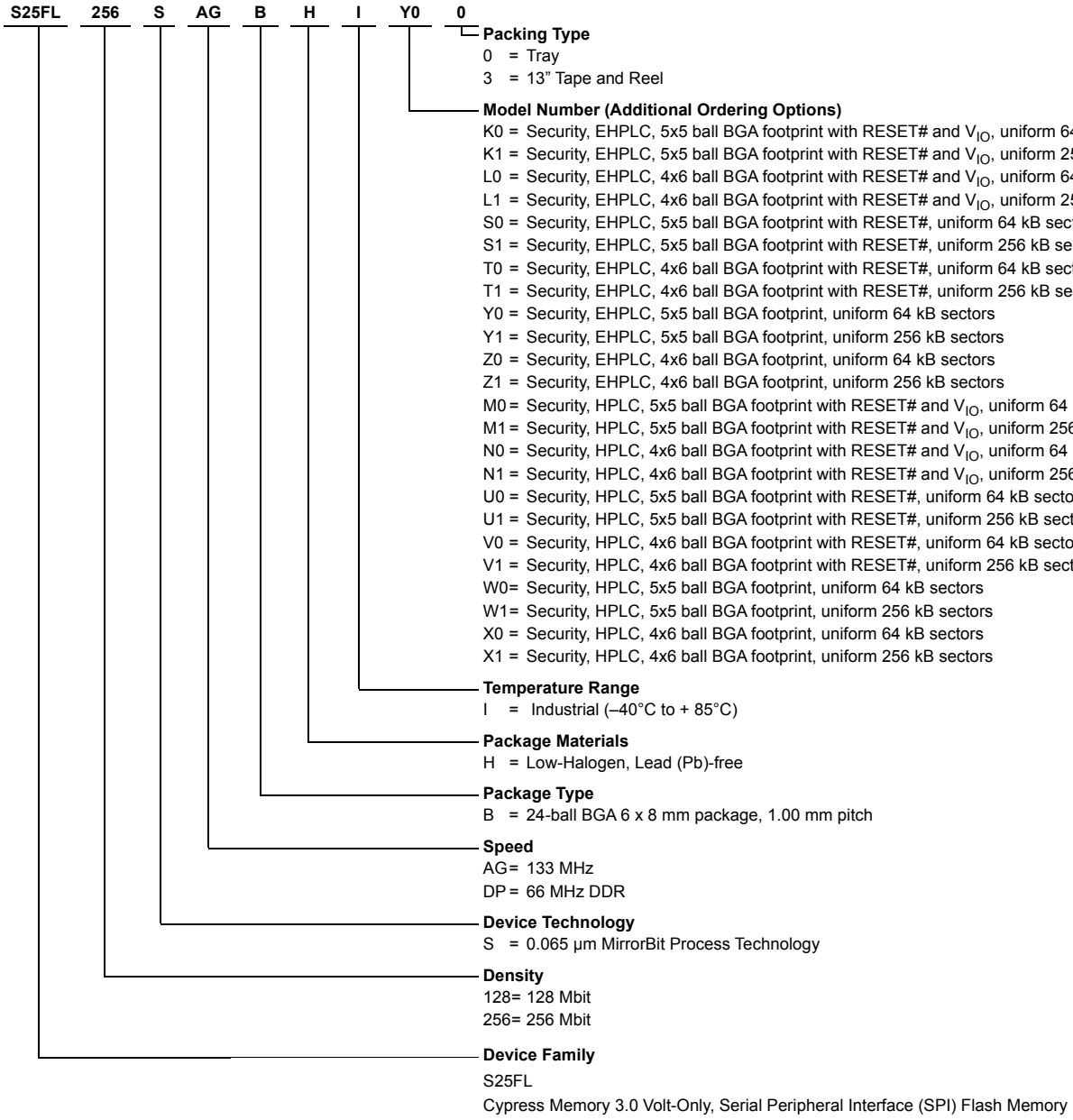
The ASP Register contents depend on the ordering options selected:

Ordering Options

Ordering Part Number Model	ASPR Default Value
K0, L0. S0, Y0, K1, L1. S1, Y1, M0, N0, U0, V0, W0, X0, M1, N1, U1, V1, W1, X1	FE67h
T0, Z0 T1, Z1	FE6Fh

7. Ordering Information – FL128S and FL256S Enhanced Security

Enhanced Security devices enable an option to permanently lock the Block Protection controls and enable all PPB bits to be One Time Programmable (OTP). The ordering part number is formed by a valid combination of the following:



Notes:

1. *EHPLC = Enhanced High Performance Latency Code table*
2. *HPLC = High Performance Latency Code table*
3. *Uniform 64 kB sectors = A hybrid of 32 x 4 kB sectors with all remaining sectors being 64 kB, with a 256B programming buffer.*
4. *Uniform 256 kB sectors = All sectors are uniform 256 kB with a 512B programming buffer.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S25FL256S Valid Combinations Secure					
Base Ordering Part Number	**Speed Option**	**Package and Temperature**	**Model Number**	**Packing Type**	**Package Marking**
S25FL128S or S25FL256S	AG	BHI	Y0, Z0, S0, T0, K0, L0	0, 3	FL + (Density) + SA + (Temp) + H + (Model Number)
			Y1, Z1, S1, T1, K1, L1		
	DP	BHI	(1)		FL + (Density) + SD + (Temp) + H + (Model Number)

Note:

1. Contact factory for availability.

8. Revision History

Spansion Publication Number: S25FL128S_256S_Secure_SP

Section	Description
Revision 01 (September 2, 2011)	
	Initial release.
Revision 02 (June 4, 2012)	
Advanced Sector Protection Description	Updated text.
Read Password Protection Mode	Removed section. This feature is available under a separate OPN data sheet.
Revision 03 (March 8, 2013)	
Initial Delivery State	Updated Ordering Options table.

Document History Page

Document Title: S25FL128S, S25FL256S 128 Mbit (16 Mbyte) and 256 Mbit (32 Mbyte), 3 V, MirrorBit® Flash Document Number: 002-00627				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	ANSI	09/02/2011	Initial release
*A	-	ANSI	06/04/2012	Advanced Sector Protection Description: Updated text Read Password Protection Mode: Removed section. This feature is available under a separate OPN data sheet
*B	-	ANSI	03/08/2013	Initial Delivery State: Updated Ordering Options table
*C	5000952	ANSI	11/18/2015	Updated to Cypress template
*D	5767606	ECAO	06/09/2017	Added Section 4.2, *Read Password Protection Mode* on page 3. Updated logo and copyright.

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