FXL3SD206
Level Shifting Voltage Translator
Two-Port SDIO MUX/DEMUX with Three Configurable Power Supplies for SDIO Device Port Expansion

Features
- Bi-Directional Interface between Two Levels: 1.65 to 3.6V
- Fully Configurable: Inputs and Outputs Track VDD
- Flexible and Programmable VDD of B and C Ports
- Non-Preferential Power-up; either VDD Can Power Up First
- Output Remains in 3-State until Active VDD Level is Reached
- Output Switches to 3-state if either VDD is at GND
- Power-off Protection
- Bus-Hold on Data Input Eliminates the Need for SDIO Pull-up Resistors
- 2:1 MUX/DEMUX of SDIO Devices in 24-Terminal Micro-MLP Package (2.5mm x 3.4mm)
- Direction Control is Automatic
- Power Switching Time (VDD_HI to VDD_LO or Reverse) is Less than 1.7µs
- 60Mbps Throughput
- ESD Protection Exceeds:
  - 12KV HBM (A, B, and C port I/O to GND) (per JESD22-A114)
  - 1KV CDM (per ESD STM5.3)

Description
FXL3SD206 is a voltage translator with multiplexing and de-multiplexing functions for SDIO devices. It is designed for voltage translation over a wide range of input and output levels, from 1.65V to 3.6V.

The multiplexing/de-multiplexing function of this device allows expansion of a host SDIO interface to two SDIO peripheral devices. When selected, each SDIO peripheral can communicate with the host through the same host interface. An alternative application allows two host devices to interface with a single SDIO peripheral.

Port A is intended to connect to a host device and the voltage level tracks the VDDA. Ports B and C are intended to connect to peripheral devices. Peripheral I/O voltage levels track either VDD_HI or VDD_LO as determined by the VDD_SEL pin. During normal operation, VDD_HI must be greater than or equal to VDD_LO. The CH_SEL, VDD_SEL, and OE pins are referenced to VDD_CON. Channel communication from either Port A to Port B or Port A to Port C is controlled by the CH_SEL pin.

The selected channel remains in 3-state until the VDD of each side reaches an active level and the OE pin reaches a valid high. Internal power-down circuitry places the selected channel of the device in 3-state if either side VDD removed.

The direction of data is controlled automatically by the device. No direction control pin is required. The device senses input signals on any port automatically and transfers the data to the corresponding output.

Applications
- SDIO Devices
- Cell Phone, PDA, Digital Camera, Portable GPS

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Eco Status</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FXL3SD206UMX</td>
<td>-40 to +85°C</td>
<td>Green</td>
<td>24-Pin, Micro-MLP, Quad, .6mm Thick, 2.5mm x 3.4mm Body</td>
<td>Tape &amp; Reel</td>
</tr>
</tbody>
</table>

For Fairchild’s definition of “green” Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html)
Application Diagrams

Figure 1. Single Host to Two SDIO Application Diagram

Figure 2. Dual Host to Single SDIO Application
Pin Configuration

![Pin Configuration Diagram](image)

Figure 3. Pin Configuration (Top Through View)

Pin Definitions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D0_A</td>
<td>Data</td>
<td>Data Pin of A Port</td>
</tr>
<tr>
<td>2</td>
<td>D1_A</td>
<td>Data</td>
<td>Data Pin of A Port</td>
</tr>
<tr>
<td>3</td>
<td>D2_A</td>
<td>Data</td>
<td>Data Pin of A Port</td>
</tr>
<tr>
<td>4</td>
<td>D3_A</td>
<td>Data</td>
<td>Data Pin of A Port</td>
</tr>
<tr>
<td>5</td>
<td>CLK_A</td>
<td>Data</td>
<td>Clock Pin of A Port</td>
</tr>
<tr>
<td>6</td>
<td>----</td>
<td>NC</td>
<td>No Connect</td>
</tr>
<tr>
<td>7</td>
<td>CMD_A</td>
<td>Data</td>
<td>Command Pin of A Port</td>
</tr>
<tr>
<td>8</td>
<td>----</td>
<td>NC</td>
<td>No Connect</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Power</td>
<td>Ground</td>
</tr>
<tr>
<td>10</td>
<td>CMD_C</td>
<td>Data</td>
<td>Command Pin of C Port</td>
</tr>
<tr>
<td>11</td>
<td>----</td>
<td>NC</td>
<td>No Connect</td>
</tr>
<tr>
<td>12</td>
<td>CMD_B</td>
<td>Data</td>
<td>Command Pin of B Port</td>
</tr>
<tr>
<td>13</td>
<td>CLK_BC</td>
<td>Data</td>
<td>Clock Pin of B or C Port</td>
</tr>
<tr>
<td>14</td>
<td>D3_BC</td>
<td>Data</td>
<td>Data Pin of B or C Port</td>
</tr>
<tr>
<td>15</td>
<td>D2_BC</td>
<td>Data</td>
<td>Data Pin of B or C Port</td>
</tr>
<tr>
<td>16</td>
<td>D1_BC</td>
<td>Data</td>
<td>Data Pin of B or C Port</td>
</tr>
<tr>
<td>17</td>
<td>D0_BC</td>
<td>Data</td>
<td>Data Pin of B or C Port</td>
</tr>
<tr>
<td>18</td>
<td>VDD_LO</td>
<td>Power</td>
<td>B or C Port, Low Power Supply</td>
</tr>
<tr>
<td>19</td>
<td>VDD_HI</td>
<td>Power</td>
<td>B or C Port, High Power Supply</td>
</tr>
<tr>
<td>20</td>
<td>VDD_CON</td>
<td>Power</td>
<td>Control Pin Power Supply</td>
</tr>
<tr>
<td>21</td>
<td>VDDA</td>
<td>Power</td>
<td>A-Port Power Supply</td>
</tr>
<tr>
<td>22</td>
<td>VDD_SEL</td>
<td>Control</td>
<td>Power Supply Select Pin of B and C Ports</td>
</tr>
<tr>
<td>23</td>
<td>CH_SEL</td>
<td>Control</td>
<td>Channel Select Pin</td>
</tr>
<tr>
<td>24</td>
<td>OE</td>
<td>Control</td>
<td>Output Enable Pin</td>
</tr>
</tbody>
</table>
Function Diagram

![Function Diagram](Image)

Figure 4. Function Diagram

Function Table

<table>
<thead>
<tr>
<th>OE</th>
<th>CH_SEL</th>
<th>VDD_SEL</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW</td>
<td>Don’t Care</td>
<td>Don’t Care</td>
<td>3-State</td>
</tr>
<tr>
<td>HIGH</td>
<td>HIGH</td>
<td>HIGH</td>
<td>Normal operation; Port A to Port B channel selected; Port B tracks VDD_HI level</td>
</tr>
<tr>
<td>HIGH</td>
<td>HIGH</td>
<td>LOW</td>
<td>Normal operation; Port A to Port B channel selected; Port B tracks VDD_LO level</td>
</tr>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>HIGH</td>
<td>Normal operation; Port A to Port C channel selected; Port C tracks VDD_HI level</td>
</tr>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>LOW</td>
<td>Normal operation; Port A to Port C channel selected; Port C tracks VDD_LO level</td>
</tr>
</tbody>
</table>

Note:
1. VDD_CON: This is a power supply pin that is used by the three control pins (VDD_SEL, CH_SEL, and OE). In single host mode, VDD_CON should be tied to the same supply as the VDDA pin. In dual host mode, VDD_CON should be tied to the same supply as either the VDD_HI or the VDD_LO pin, depending upon which host is used to drive the control pins.
### Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td>VDDA, VDD_HI, VDD_LO, VDD_CON</td>
<td>-0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>DC Input Voltage</td>
<td>Data Ports A, B, and C</td>
<td>-0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Control Inputs (OE, CH_SEL, VDD_SEL)</td>
<td>-0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage(2)</td>
<td>Output 3-State</td>
<td>-0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Active (Port A)</td>
<td>-0.5</td>
<td>VDDA+0.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Active (Port B or C)</td>
<td>-0.5</td>
<td>VDD_HI+0.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Active (Port B or C)</td>
<td>-0.5</td>
<td>VDD_LO+0.5</td>
<td></td>
</tr>
<tr>
<td>IK</td>
<td>DC Input Diode Current</td>
<td>V&lt;0V</td>
<td>-50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>OK</td>
<td>DC Output Diode Current</td>
<td>V&lt;0V</td>
<td>-50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&gt;VCC</td>
<td>+50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IOK/IOL</td>
<td>DC Output Source/Sink Current</td>
<td>VDDA, VDD_HI, VDD_LO, VDD_CON</td>
<td>-50</td>
<td>+50</td>
<td>mA</td>
</tr>
<tr>
<td>IDD</td>
<td>DC VDD or Ground Current per Supply Pin</td>
<td>VDDA, VDD_HI, VDD_LO, VDD_CON</td>
<td>±100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature Range</td>
<td>-65 to +150 °C</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:** 2. IO absolute maximum rating must be observed.

### Recommended Operating Conditions (3)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Power Supply Operating</td>
<td>VDDA, VDD_HI, VDD_LO, VDD_CON</td>
<td>1.65</td>
<td>3.60</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD_HI ≥ VDD_LO(4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Input Voltage</td>
<td>Port A</td>
<td>0</td>
<td>VDDA</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Port B and C(5)</td>
<td>0</td>
<td>VDD_HI</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Port B and C(5)</td>
<td>0</td>
<td>VDD_LO</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Free Air Operation Temperature</td>
<td>Data Port A at VDDA=1.65 to 3.6V</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data Ports B and C at VDD_A=1.65 to 3.6V</td>
<td></td>
<td>10</td>
<td>ns/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OE, CH_SEL, VDD_SEL at VDD_CON=1.65 to 3.6V</td>
<td></td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
3. All unused inputs and input/outputs must be held at VDD or GND.
4. During normal operation, VDD_HI must be greater than or equal to VDD_LO.
5. The input and output voltages of Ports B and C are determined by which VDD is selected.
Application Information

Power-Up / Power-Down Sequencing

FXL translators offer an advantage in that any V_{DD} may be powered up first. This benefit derives from the chip design. When VDDA or both VDD_HI and VDD_LO pins are at 0 volts, outputs are in a high-impedance state (see Power Up Operation table below). As a multiplexer, the device allows the unselected port to remain in a high-impedance state for power saving. The control inputs (OE, CH_SEL, VDD_SEL) are designed to track VDD_CON. An external pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive current, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

During normal operation, V_{DD,HI} must be greater than or equal to V_{DD,LO}. During power-up or power-down, V_{DD,LO} may exceed V_{DD,HI} without damaging the device.

The recommended power-up sequence is:
1. Apply the power to the first V_{DD}.
2. Apply the power to the second V_{DD}.
3. Set the CH_SEL and VDD_SEL pin according to the application.
4. Drive the OE input high to enable the device.

The recommended the power-down sequence is:
1. Drive the OE input low to disable the device.
2. Remove the setting of CH_SEL and VDD_SEL pin.
3. Remove power from either V_{DD}.
4. Remove power from other V_{DD}.

<table>
<thead>
<tr>
<th>VDDA</th>
<th>VDD_HI</th>
<th>VDD_LO</th>
<th>VDD_SEL</th>
<th>Port B or C Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>Don’t Care</td>
<td>Don’t Care</td>
<td>Don’t Care</td>
<td>High Impedance</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>Don’t Care</td>
<td>High Impedance</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>HIGH</td>
<td>Enabled, Reference to VDD_HI</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LOW</td>
<td>High Impedance</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>HIGH</td>
<td>High Impedance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LOW</td>
<td>Enabled, Reference to VDD_LO</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>HIGH</td>
<td>Enabled, Reference to VDD_HI</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LOW</td>
<td>Enabled, Reference to VDD_LO</td>
</tr>
</tbody>
</table>
## DC Electrical Characteristics

$T_A=-40^\circ C$ to $85^\circ C$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>$V_{DD_A}$, $V_{DD_n}$ (V)</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IHA}$</td>
<td>High Level Input Voltage(6)</td>
<td>Data Inputs Dn_A, CMD_A, CLK_A, CH_SEL=A</td>
<td>1.65 – 3.6</td>
<td>0.6 x $V_{DD_A}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IHB}$</td>
<td>High Level Input Voltage(6)</td>
<td>Data Inputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H</td>
<td>1.65 – 3.6</td>
<td>0.6 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IHC}$</td>
<td>High Level Input Voltage(6)</td>
<td>Data Inputs Dn_BC, CMD_C, CLK_BC, CH_SEL=L</td>
<td>1.65 – 3.6</td>
<td>0.6 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td></td>
<td>OE, VDD_SEL, CH_SEL</td>
<td>1.65 – 3.6</td>
<td>0.6 x $V_{DD_CON}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ILA}$</td>
<td>Low Level Input Voltage(6)</td>
<td>Data Inputs Dn_A, CMD_A, CLK_A, CH_SEL=A</td>
<td>1.65 – 3.6</td>
<td>0.35 x $V_{DD_A}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ILB}$</td>
<td>Low Level Input Voltage(6)</td>
<td>Data Inputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H</td>
<td>1.65 – 3.6</td>
<td>0.35 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ILC}$</td>
<td>Low Level Input Voltage(6)</td>
<td>Data Inputs Dn_BC, CMD_C, CLK_BC, CH_SEL=L</td>
<td>1.65 – 3.6</td>
<td>0.35 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td></td>
<td>OE, VDD_SEL, CH_SEL</td>
<td>1.65 – 3.6</td>
<td>0.35 x $V_{DD_CON}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OHA}$</td>
<td>High Level Output Voltage(6, 7)</td>
<td>Data Outputs Dn_A, CMD_A, CLK_A, I_HOLD=-20µA</td>
<td>1.65 – 3.6</td>
<td>0.75 x $V_{DD_A}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OHB}$</td>
<td>High Level Output Voltage(6, 7)</td>
<td>Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H, I_HOLD=+20µA</td>
<td>1.65 – 3.6</td>
<td>0.75 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OHC}$</td>
<td>High Level Output Voltage(6, 7)</td>
<td>Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=L, I_HOLD=+20µA</td>
<td>1.65 – 3.6</td>
<td>0.75 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OLA}$</td>
<td>Low Level Output Voltage(6, 7)</td>
<td>Data Outputs Dn_A, CMD_A, CLK_A, I_HOLD=+20µA</td>
<td>1.65 – 3.6</td>
<td>0.25 x $V_{DD_A}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OLB}$</td>
<td>Low Level Output Voltage(6, 7)</td>
<td>Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H, I_HOLD=+20µA</td>
<td>1.65 – 3.6</td>
<td>0.25 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OLC}$</td>
<td>Low Level Output Voltage(6, 7)</td>
<td>Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=L, I_HOLD=+20µA</td>
<td>1.65 – 3.6</td>
<td>0.25 x $V_{DD_n}$</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

6. Port B and Port C share the same data and clock pin, and $VDD_n$ refers to $VDD\_HI$ or $VDD\_LO$, whichever is selected. During normal operation, $VDD\_HI$ must be greater than or equal to $VDD\_LO$.

7. This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”
### DC Electrical Characteristics (Continued)

$T_A=\text{-}40°C$ to $85°C$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>$V_{DD_A}$ (V)</th>
<th>$V_{DD_n}$ (V)</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ODH}$</td>
<td>Bushold Input Overdrive High Current$^6$</td>
<td>Data Inputs $Dn_A$, $CMD_A$, $CLK_A$, $Dn_BC$, $CMD_B$, $CMD_C$, $CLK_BC$</td>
<td>3.6</td>
<td>3.6</td>
<td>450</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7</td>
<td>2.7</td>
<td>300</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.95</td>
<td>1.95</td>
<td>200</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{ODL}$</td>
<td>Bushold Input Overdrive Low Current$^6$</td>
<td>Data Inputs $Dn_A$, $CMD_A$, $CLK_A$, $Dn_BC$, $CMD_B$, $CMD_C$, $CLK_BC$</td>
<td>3.6</td>
<td>3.6</td>
<td>-450</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7</td>
<td>2.7</td>
<td>-300</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.95</td>
<td>1.95</td>
<td>-200</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_I$</td>
<td>Input Leakage Current</td>
<td>Control Inputs $OE$, $CH_{SEL}$, $VDD_{SEL}$, $V=VDD_{CON}$ or GND</td>
<td>1.65 to 3.6</td>
<td>3.6</td>
<td>±1.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>Power Off Leakage Current</td>
<td>$Dn_A$, $CMD_A$, $CLK_A$; $V_O=0$ to 3.6V</td>
<td>0</td>
<td>3.6</td>
<td>±2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Dn_BC$, $CMD_B$, $CMD_C$, $CLK_BC$; $V_O=0$ to 3.6V</td>
<td>3.6</td>
<td>0</td>
<td>±2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>3-state Output Leakage</td>
<td>$Dn_A$, $CMD_A$, $CMD_B$, $CMD_C$, $CLK_A$, $CLK_B$; $V_O=0$ or 3.6V; $OE=V_{IL}$</td>
<td>3.6</td>
<td>3.6</td>
<td>±2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Dn_A$, $CMD_A$, $CLK_B$; $V_O=0$ or 3.6V; $OE=Don't Care$$^{10}$</td>
<td>3.6</td>
<td>0</td>
<td>±2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Dn_BC$, $CMD_B$, $CMD_C$, $CLK_BC$; $V_O=0$ or 3.6V; $OE=Don't Care$</td>
<td>0</td>
<td>3.6</td>
<td>±2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Quiescent Supply Current$^{11, 12}$</td>
<td>$V=VDDI$ or GND; $I_O=0$</td>
<td>1.65 to 3.6</td>
<td>1.65 to 3.6</td>
<td>5.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>1.65 to 3.6</td>
<td>2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.65 to 3.6</td>
<td>0</td>
<td>2.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{CCZ}$</td>
<td>Quiescent Supply Current$^{11}$</td>
<td>$V=VDDI$ or GND; $I_O=0$, $OE=VIL$</td>
<td>1.65 to 3.6</td>
<td>1.65 to 3.6</td>
<td>5.0</td>
<td>$\mu A$</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

8. An external driver must source at least the specified current to switch LOW-to-HIGH.
9. An external driver must source at least the specified current to switch HIGH-to-LOW.
10. “Don’t care” indicates any valid logic level.
11. $VDDI$ is the $VDD$ associated with the input side.
12. Reflects current per supply, $V_{DD_A}$ or $V_{DD_n}$. 
## Dynamic Output Electrical Characteristics

**A Port (Dn_A, CMD_A, CLK_A), B and C Port (CMD_B, CMD_C)**

Output Load: $CL=15pF$, $RL \geq 1M\Omega$ ($C_{I/O}=10pF$). $T_A=-40^\circ C$ to $85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V_{DD}=2.8V$ to $3.6V$</th>
<th>$V_{DD}=2.3V$ to $2.7V$</th>
<th>$V_{DD}=1.65V$ to $1.95V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{rise}$</td>
<td>Output Rise Time A Port$^{(13)}$</td>
<td>3.0</td>
<td>3.5</td>
<td>4.0</td>
</tr>
<tr>
<td>$t_{fall}$</td>
<td>Output Fall Time A Port$^{(14)}$</td>
<td>3.0</td>
<td>3.5</td>
<td>4.0</td>
</tr>
<tr>
<td>$I_{OHD}$</td>
<td>Dynamic Output Current High$^{(13)}$</td>
<td>-14.0</td>
<td>-10.0</td>
<td>-6.2</td>
</tr>
<tr>
<td>$I_{OLD}$</td>
<td>Dynamic Output Current Low$^{(14)}$</td>
<td>+14.0</td>
<td>+10.0</td>
<td>+6.2</td>
</tr>
</tbody>
</table>

**B and C Port (Dn_BC, CLK_BC)**

Output Load: $CL=30pF$, $RL \geq 1M\Omega$ ($C_{I/O}=10pF$). $T_A=-40^\circ C$ to $85^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V_{DD}=2.8V$ to $3.6V$</th>
<th>$V_{DD}=2.3V$ to $2.7V$</th>
<th>$V_{DD}=1.65V$ to $1.95V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{rise}$</td>
<td>Output Rise Time B and C Port$^{(13)}$</td>
<td>3.0</td>
<td>3.5</td>
<td>4.0</td>
</tr>
<tr>
<td>$t_{fall}$</td>
<td>Output Fall Time B and C Port$^{(14)}$</td>
<td>3.0</td>
<td>3.5</td>
<td>4.0</td>
</tr>
<tr>
<td>$I_{OHD}$</td>
<td>Dynamic Output Current High$^{(13)}$</td>
<td>-22.4</td>
<td>-15.8</td>
<td>-10.0</td>
</tr>
<tr>
<td>$I_{OLD}$</td>
<td>Dynamic Output Current Low$^{(14)}$</td>
<td>+22.4</td>
<td>+15.8</td>
<td>+10.0</td>
</tr>
</tbody>
</table>

**Notes:**

13. See Figure 9.
14. See Figure 10.
### AC Characteristics

**V\text{DD}_A=2.8\text{V to 3.6V and } T_A=-40^\circ \text{C to 85}\text{°C}.$**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V\text{DD}_A=2.8\text{V to 3.6V}$</th>
<th>$V\text{DD}_n=2.3\text{V to 2.7V}$</th>
<th>$V\text{DD}_n=1.65\text{V to 1.95V}$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{PLH}}$</td>
<td>A to B/C</td>
<td>0.2</td>
<td>3.5</td>
<td>0.3</td>
<td>3.9</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>B/C to A</td>
<td>0.2</td>
<td>3.5</td>
<td>0.2</td>
<td>3.8</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>OE to A</td>
<td>1.7</td>
<td></td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>OE to B/C</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>$t_{\text{PCH}}$</td>
<td>CH_SEL B to C</td>
<td>1.7</td>
<td></td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PCH}}$</td>
<td>or C to B</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>$t_{\text{skew}}$</td>
<td>A, B, C Port((^{(15)}))</td>
<td>0.5</td>
<td>0.5</td>
<td>1.0</td>
<td></td>
</tr>
</tbody>
</table>

**V\text{DD}_A=2.3\text{V to 2.7V and } T_A=-40^\circ \text{C to 85}\text{°C}.$**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V\text{DD}_A=2.3\text{V to 2.7V}$</th>
<th>$V\text{DD}_n=2.3\text{V to 2.7V}$</th>
<th>$V\text{DD}_n=1.65\text{V to 1.95V}$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{PLH}}$</td>
<td>A to B/C</td>
<td>0.3</td>
<td>3.8</td>
<td>0.4</td>
<td>4.5</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>B/C to A</td>
<td>0.3</td>
<td>3.9</td>
<td>0.4</td>
<td>4.5</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>OE to A</td>
<td>1.7</td>
<td></td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>OE to B/C</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>$t_{\text{PCH}}$</td>
<td>CH_SEL B to C</td>
<td>1.7</td>
<td></td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PCH}}$</td>
<td>or C to B</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>$t_{\text{skew}}$</td>
<td>A, B, C Port((^{(15)}))</td>
<td>0.5</td>
<td>0.5</td>
<td>1.0</td>
<td></td>
</tr>
</tbody>
</table>

**V\text{DD}_A=1.65\text{V to 1.95V and } T_A=-40^\circ \text{C to 85}\text{°C}.$**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$V\text{DD}_A=1.65\text{V to 1.95V}$</th>
<th>$V\text{DD}_n=2.3\text{V to 2.7V}$</th>
<th>$V\text{DD}_n=1.65\text{V to 1.95V}$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{PLH}}$</td>
<td>A to B/C</td>
<td>1.7</td>
<td>5.0</td>
<td>0.5</td>
<td>5.5</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>B/C to A</td>
<td>0.5</td>
<td>5.4</td>
<td>0.5</td>
<td>5.6</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>OE to A</td>
<td>1.7</td>
<td></td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>OE to B/C</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>$t_{\text{PCH}}$</td>
<td>CH_SEL B to C</td>
<td>1.7</td>
<td></td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PCH}}$</td>
<td>or C to B</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>$t_{\text{skew}}$</td>
<td>A, B, C Port((^{(15)}))</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
15. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port and switching with the same polarity (LOW to HIGH or HIGH to LOW). See Figure 12. Skew is guaranteed, but not tested.
Maximum Data Rate

$T_A=-40°C$ to $85°C$.

<table>
<thead>
<tr>
<th>$V_{DD_A}$</th>
<th>Direction</th>
<th>$V_{DD_n}=2.8$ to $3.6V$</th>
<th>$V_{DD_n}=2.3$ to $2.7V$</th>
<th>$V_{DD_n}=1.65$ to $1.95V$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Min.</td>
<td>Min.</td>
<td>Mbps</td>
</tr>
<tr>
<td>$V_{DD_A}=2.8$ to $3.6V$</td>
<td>A to B/C</td>
<td>100</td>
<td>100</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B/C to A</td>
<td>100</td>
<td>100</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>$V_{DD_A}=2.3$ to $2.7V$</td>
<td>A to B/C</td>
<td>100</td>
<td>100</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B/C to A</td>
<td>100</td>
<td>100</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>$V_{DD_A}=1.65$ to $1.95V$</td>
<td>A to B/C</td>
<td>80</td>
<td>80</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B/C to A</td>
<td>80</td>
<td>80</td>
<td>60</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
16. Maximum Data Rate is specified in megabits per second. See Figure 11. It is equivalent to two times the $f_{TOGGLE}$ frequency, specified in megahertz. For example, 100Mbps is equivalent to 50MHz.

Capacitance

$T_A=+25°C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance Control Pins (OE, VDD_SEL, CH_SEL)</td>
<td>$V_{DD_CON}=GND$</td>
<td>4.0</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>Input/Output Capacitance Dn_A, CMD_A,CLK_A Dn_BC, CMD_B, CMD_C, CLK_BC</td>
<td>$V_{DD_A}=V_{DD_n}=3.3V$, OE=$V_{DD_A}$, CH_SEL=$V_{DD_A}$ or GND</td>
<td>5.0</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{PD}$</td>
<td>Power Dissipation Capacitance</td>
<td>$V_{DD_A}=V_{DD_n}=3.3V$, $V_I=0V$ or $V_{DD}$, $f=10MHz$</td>
<td>25</td>
<td>pF</td>
</tr>
</tbody>
</table>
Test Diagrams

![Figure 5. AC Test Circuit](image)

Table 2. AC Test Conditions

<table>
<thead>
<tr>
<th>Test</th>
<th>Input Signal</th>
<th>Output Enable Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH, tPHL</td>
<td>Data Pulses</td>
<td>V = VDD, CON</td>
</tr>
<tr>
<td>tPZL</td>
<td>0V</td>
<td>LOW to HIGH Switch</td>
</tr>
<tr>
<td>tPZH</td>
<td>VCCI</td>
<td>LOW to HIGH Switch</td>
</tr>
</tbody>
</table>

Table 3. AC Load

<table>
<thead>
<tr>
<th>VCCo</th>
<th>CL</th>
<th>RL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port A, B, or C</td>
<td>Port A, CMD_B, CMD_C</td>
<td>Port A, B, or C</td>
</tr>
<tr>
<td>1.8V ± 0.15V</td>
<td>15pF</td>
<td>30pF</td>
</tr>
<tr>
<td>2.5V ± 0.2V</td>
<td>15pF</td>
<td>30pF</td>
</tr>
<tr>
<td>2.8V to 3.6V</td>
<td>15pF</td>
<td>30pF</td>
</tr>
</tbody>
</table>

![Figure 6. Waveform for Inverting and Non-Inverting Functions](image)

Notes:
17. Input tR = tF = 2.0ns, 10% to 90%.
18. Input tR = tF = 2.5ns, 10% to 90%, at VCC = 3.0V to 3.6V only.
Figure 7. 3-State Output Low Enable Time for Low Voltage Logic

Notes:
19. Input $t_R = t_F = 2.0\text{ns}$, 10% to 90%.
20. Input $t_R = t_F = 2.5\text{ns}$, 10% to 90%, at $V_I = 3.0\text{V}$ to $3.6\text{V}$ only.

Figure 8. 3-State Output High Enable Time for Low Voltage Logic

Notes:
21. Input $t_R = t_F = 2.0\text{ns}$, 10% to 90%.
22. Input $t_R = t_F = 2.5\text{ns}$, 10% to 90%, at $V_I = 3.0\text{V}$ to $3.6\text{V}$ only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>$V_{DD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{MI}$</td>
<td>$V_{DDI}/2$</td>
</tr>
<tr>
<td>$V_{MO}$</td>
<td>$V_{DDO}/2$</td>
</tr>
<tr>
<td>$V_X$</td>
<td>$0.9 \times V_{DDO}$</td>
</tr>
<tr>
<td>$V_Y$</td>
<td>$0.1 \times V_{DDO}$</td>
</tr>
</tbody>
</table>
Figure 9. Active Output Rise Time and Dynamic Output Current High

\[ I_{OH} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \cdot V_{CCO}}{t_{RISE}} \]

Figure 10. Active Output Fall Time and Dynamic Output Current Low

\[ I_{OH} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \cdot V_{CCO}}{t_{FALL}} \]

Figure 11. Maximum Data Rate

\[ t_W = \frac{1}{f} \]

Figure 12. Output Skew Time

\[ t_{skew} = (t_{pHL\max} - t_{pHL\min}) \text{ or } (t_{pLH\max} - t_{pLH\min}) \]
Physical Dimensions

Figure 13. 24-Pin, Micro-MLP, Quad, .6mm Thick, 2.5mm x 3.4mm Body

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/
**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks:

- Build It Now™
- CoreFLEX™
- CrossPower™
- CTRL™
- Current Transfer Logic™
- EcoPower®
- EfficentMax™
- E2Switch™
- E2V®
- Fairchild®
- Fairchild Semiconductor®
- FACT®
- Quiet Series™
- FAST™
- F-A-V®
- FlashWrite™
- FFS™
- F-FET™
- FRFET™
- Global Power Resource™
- Green FET™
- Green FFS™
- GTOP™
- IntelMAX™
- ISSOPLANAR™
- MicroCoupler™
- MicroFET™
- MicroPower™
- MMIC™
- MotionMax™
- Motion-SPI™
- OPTOLOGIC™
- OPTOPLANAR®
- POP™
- Power-SPI™
- PowerTrench®
- PowerST™
- Programmable Active Droop™
- Q8™
- Quiet Series™
- RapidConfigure™
- Saving our world, 1mW/WW at a time™
- SmartMax™
- SMART START™
- SPI™
- STEALTH™
- SuperFET™
- SuperSOIC™
- SuperSOT™
- SuperSOT™-A
- SynFET™
- SYSTEM™
- The Power Franchise®
- TinBar™
- TinyBoost™
- TinyBoost C™
- TinyLogic™
- TinyOCTO™
- TinyPower™
- TinyPower C™
- TinyVGA™
- TrueFault Detect™
- TrueCurrent™
- uCerTest™
- Ultra FET™
- UniFET™
- VCC™
- VisualMax™
- X5™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN WITHOUT INFRINGING THE RIGHTS TO PATENTS PRESENTLY ISSUED OR PENDING IN THE UNITED STATES OR OTHER COUNTRIES. FAIRCHILD DOES NOT ASSUMES LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation’s Anti-Counterfeiting Policy. Fairchild’s Anti-Counterfeiting Policy is also stated on our external website, www.fairchilsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failure, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed on our website.

As a customer, you have the right to expect (a) that your semiconductor parts will function to specifications, (b) that your parts will not fail during normal operation, (c) protection of your intellectual property, and (d) a supply of parts for a reasonable period of time. Counterfeit parts can yield significant losses in each of these areas. The semiconductor industry is developing standards to combat counterfeiting, and Fairchild will support efforts to make semiconductor parts safe for our customers.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advance Information</td>
<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not in Production</td>
<td>Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.</td>
</tr>
</tbody>
</table>