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ıMCP HTLRBL32L Breakout Board

HTLRBL32L SiP Breakout Board

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Date: 01/02/2023

Code: HTLRBL32L-Breakout

SUMMARY

DOCUMENT INFO

This document provides the technical information about the iMCP HTLRBL32L Breakout Board.

1. GENERAL DESCRIPTION

The HTLRBL32L Breakout Board was designed to be a simple first contact of the customer with the HTLRBL32L SiP, ensuring you can start testing and developing your own product with a minimal structure. All the features of the HTLRBL32L are present on this board.

2. FEATURES AND BENEFITS

2.1. KEY FEATURES

- iMCP HTLRBL32L
- 256kB of flash memory
- 64kB of RAM
- 7 kB ROM
- SWD interface
- MCU bootloader
- 18 GPIOs
- SPI, UART, I2C
- 2 SMA Antenna connector

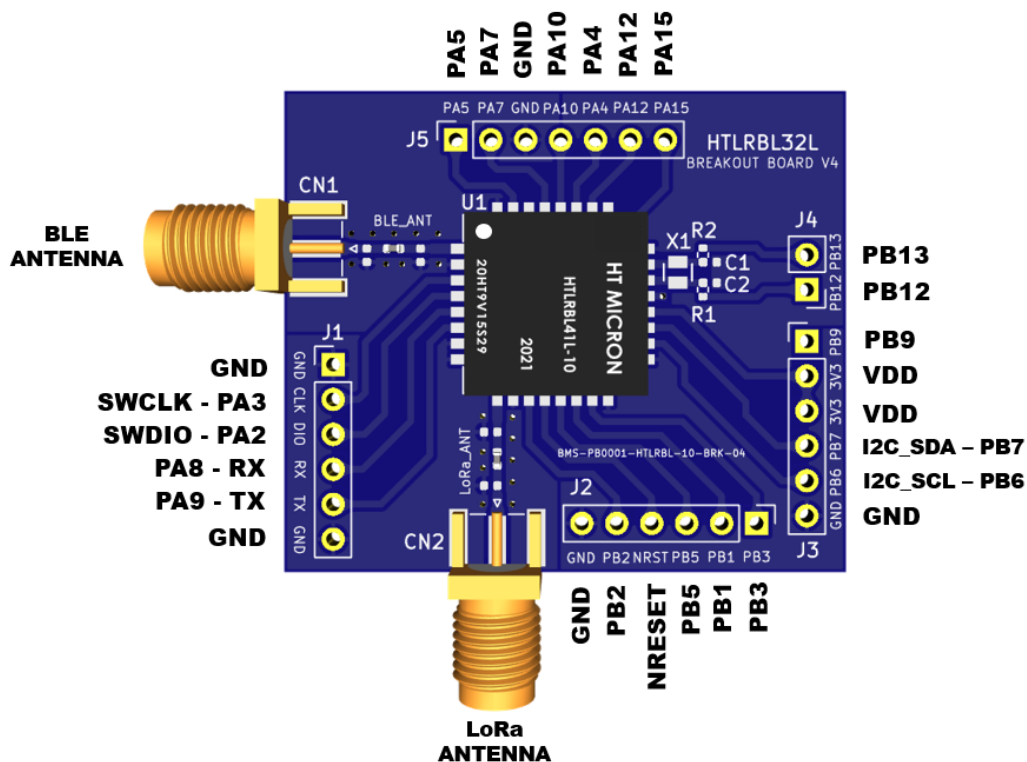# 3. PINOUT INFORMATION

3.1. PIN DIAGRAM

Figure 1: Pin Diagram

3.2. CONNECTIONS DESCRIPTION

Table 1: Detailed pin functions.

Connector	Number	Name	Alt. Functions	Type	Additional Feature
CN1	-	BLE Antenna	-	RF I/O	-
CN2	-	LoRa Antenna	-	RF I/O	-
J1	1	GND	-	Ground	-
	2	PA3	SWCLK USART_RTS_DE TIM_BKIN2 SPI3_SCK TIM1_CH6 I2S3_SCK	Digital I/O	Wakeup
	3	PA2	SWDIO USART_CK TIM_BKIN SPI3_MCK TIM1_CH5 I2S3_MCK	Digital I/O	Wakeup
	4	PA8	USART_RX SPI1_MOSI RX_SEQUENCE SPI3_MISO TIM1_CH3 I2S3_MISO	Digital I/O	Wakeup, GPIO in DEEPSTOP, RTC_OUT
	5	PA9	USART_TX SPI1_SCK RTC_OUT SPI3_NSS TIM1_CH4 I2S3_WS	Digital I/O	Wakeup, GPIO in DEEPSTOP, LCO
	6	GND	-	-	-
J2	1	GND	-	-	-
	2	PB2	USART_RTS_DE PDM_DATA TIM1_CH3	Digital I/O	ADC_VINM0, wakeup
	3	NRESET	-	Digital Input	-
	4	PB5	LPUART_RX SPI2_MOSI PDM_CLK I2S2_SD	Digital I/O	PGA_VBIAS_MIC, wakeup

	5	**PB1**	SPI1_NSS PDM_CLK TIM1_ETR	Digital I/O	ADC_VINP1, wakeup
	6	**PB3**	USART_CTS LPUART_TX TIM1_CH4	Digital I/O	ADC_VINP0, wakeup
J3	1	**PB9**	USART_TX LPUART_CTS SPI2_MCK TIM1_CH1N TIM1_CH2N I2S2_MCK	Digital I/O	Wakeup
	2	**VDD**	-	Power	-
	3	**VDD**	-	Power	-
	4	**PB7**	I2C2_SDA SPI2_SCK LPUART_RX TIM1_CH2 I2S2_SCK	Digital I/O	Wakeup
	5	**PB6**	I2C2_SCL SPI2_NSS LPUART_TX TIM1_CH1 I2S2_WS	Digital I/O	Wakeup
	6	**GND**	-	Ground	-
J4	1	**PB13**	SPI1_MISO I2C2_SCL PDM_CLK TIM1_BKIN2 TIM1_CH4	Digital I/O LS Crystal Input	SXTAL1
	2	**PB12**	SPI1_SCK LCO PDM_DATA TIM1_BKIN TIM1_CH3	Digital I/O LS Crystal Input	SXTAL0

J5	1	**PA5**	MCO SPI2_SCK LPUART_RX TIM1_CH2 I2S2_SCK	Digital I/O	Wakeup, GPIO in DEEPSTOP, LCO
	2	**PA7**	LPUART_RTS_DE SPI2_MISO SPI2_SCK TIM1_CH2 I2S2_MISO I2S2_SCK	Digital I/O	Wakeup, GPIO in DEEPSTOP, RTC_OUT
	3	**GND**	-	Ground	-
	4	**PA10**	LCO SPI1_MISO TX_SEQUENCE SPI3_MCK TIM1_CH5 I2S3_MCK	Digital I/O	BOOT, wakeup, GPIO in DEEPSTOP, LCO
	5	**PA4**	LCO SPI2_NSS LPUART_TX TIM1_CH1 I2S2_WS	Digital I/O	Wakeup, GPIO in DEEPSTOP, LCO
	6	**PA12**	I2C1_SMBA SPI1_NSS SPI2_MOSI TIM1_CH1 I2S2_SD	Digital I/O	ADC_VINM3, wakeup
	7	**PA15**	I2C2_SMBA SPI1_MOSI TIM1_BKIN2	Digital I/O	ADC_VINP2, wakeup

For reference manuals and information related to pin functions please consult STM's BlueNRG-LP Datasheet

3.3. PERIPHERAL PINS

Table 2: Other pins description.

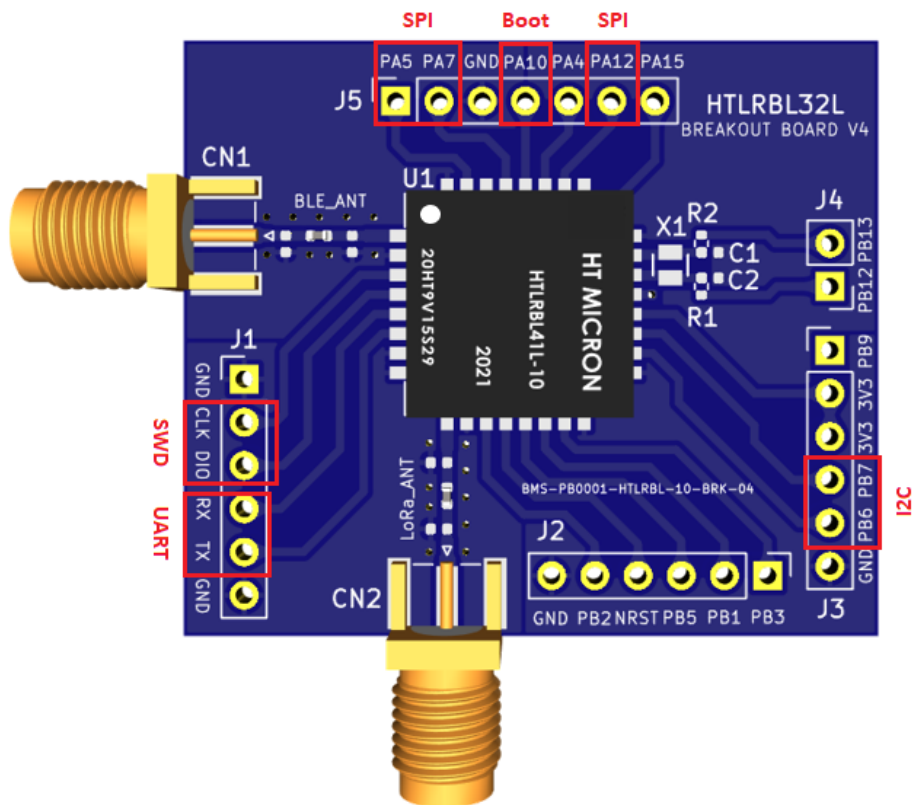| Pins	Description
I²C	Serial interface. Alternative functions are also available on these pins. These pins can also be used as GPIO
SWD	Serial Wire Debug interface to programming and debug the HTLRBL32L. These pins can also be used as GPIO
TX/RX	These pins can be used to communicate with HTLRBL32L through UART. Alternative functions are also available on these pins. These pins can also be used as GPIO.
SPI	Suggested Serial Peripheral Interface pins, can also be used as GPIO.
Boot	Activation of bootloader process, enable it by toggling PA10 on state HIGH during a reset.

Figure 2: Other pins.

4. STATIC CHARACTERISTICS

4.1. GENERAL OPERATING RANGE

Table 3: General operating conditions.

Parameter	Min	Typ.	Max	Unit
Supply Voltage	2.7	3.3	3.6	V
Supply Current	-	-	300	mA
Operating Temperature	-20	25	70	°C
External XTAL Frequency	-	-	32.768	kHz

4.2. EXTERNAL CLOCK RESONATOR

The iMCP HTLRBL32L is provided with an internal clock generator of 33 kHz with a standard deviation of frequency spread vs. temperature of 140 ppm/°C. Also, as presented in Table 1, PB12 and PB13 pins have multiple functionalities, one of which is to be the input and output for a low-speed external crystal oscillator. If a higher frequency precision than the internal clock generator is needed, a 32.768 kHz can be connected to these pins. The crystal specifications are shown in Table 4. The load capacitors C1 and C2 should be defined based on the load capacitance of the selected crystal. A rule of thumb is to use the following formula to find the capacitors' value:

$$C1, C2 = 2*CL - 2*Cstray$$

Cstray is the parasitic capacitance generated by the traces and ground planes. Often the stray capacitance is defined to be a value around 2 to 5 pF.
If an external clock oscillator is not needed, PB12 and P13 pins can be used as GPIOs. In this case, 0 Ohm resistors must be soldered on R1 and R2 footprints (0402 inches sized) to connect the headers to the iMCP pins.

Table 4: 32.768kHz crystal requirements.

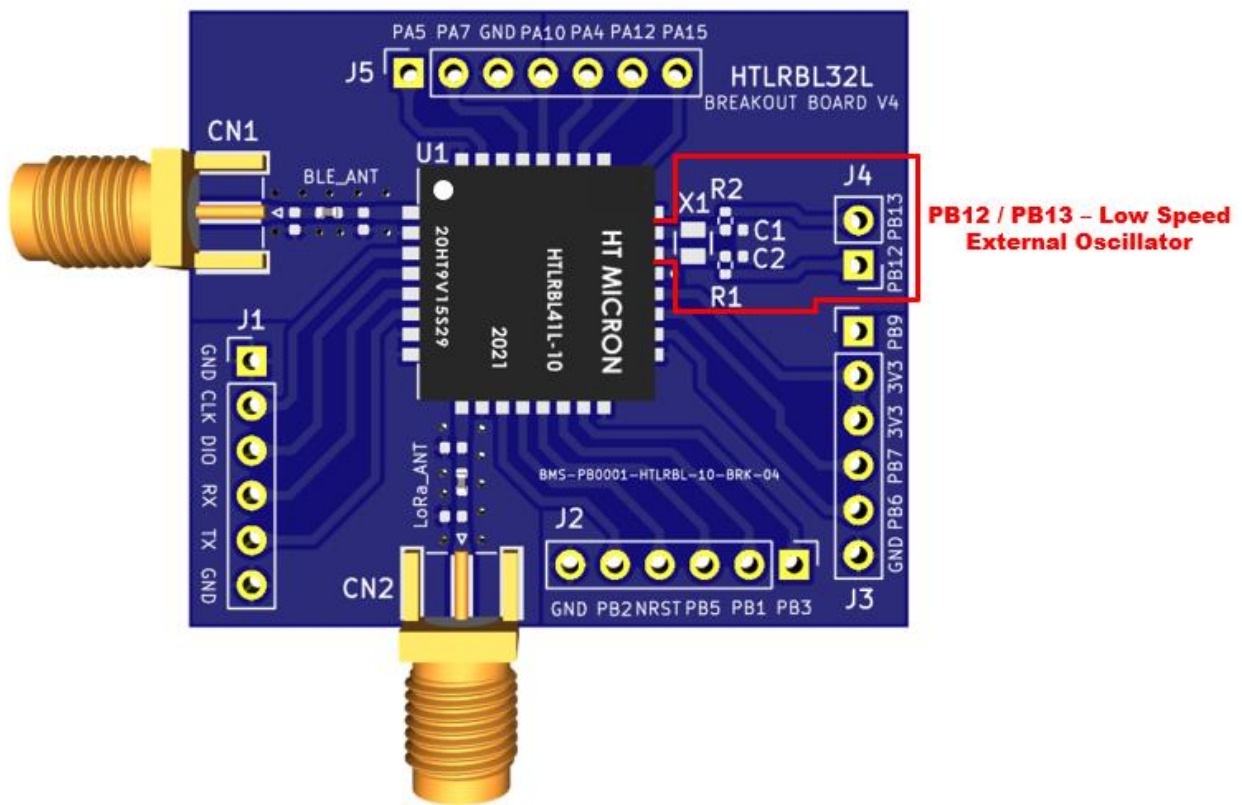| Parameter	Min	Typ.	Max	Unit
Nominal Frequency	-	32.768	-	kHz
Equivalent Series Resistance	-	-	90	kΩ
Drive Level	-	-	0.1	µW

Figure 3: PB12 and PB13 - External low speed oscillator or GPIO pins.

5. RF CHARACTERISTICS

The breakout board can be directly connected to 50 Ω antennas. If the antenna impedance or the input impedance of the circuit connected to the SMA connectors is 50 Ω, only the 0 Ω series resistor already provided in the board is necessary. However, if the impedances are different from 50 Ω, some of the power may be lost due to impedance mismatch. In this case, the footprints left available between the iMCP pads and the SMA connectors can be used to match the impedances through an L or π matching network. The footprints are 0402 inches sized.

Table 5: Operation frequencies and expected TX max. output power. TA = 25°C and supply voltage of 3.3V;

Parameter	Min	Typ.	Max	Unit
LoRa RF Characteristics				
RF Frequency	433	-	928	MHz
Tx max. output power	-	-	TBD	dBm
BLE RF Characteristics				
RF Frequency	2,402	-	2,480	GHz
Tx max. output power	-	-	TBD	

For detailed information about HTLRBL32L V1.6 RF characteristics, please refer to HTLRBL32L V1.6 datasheet.

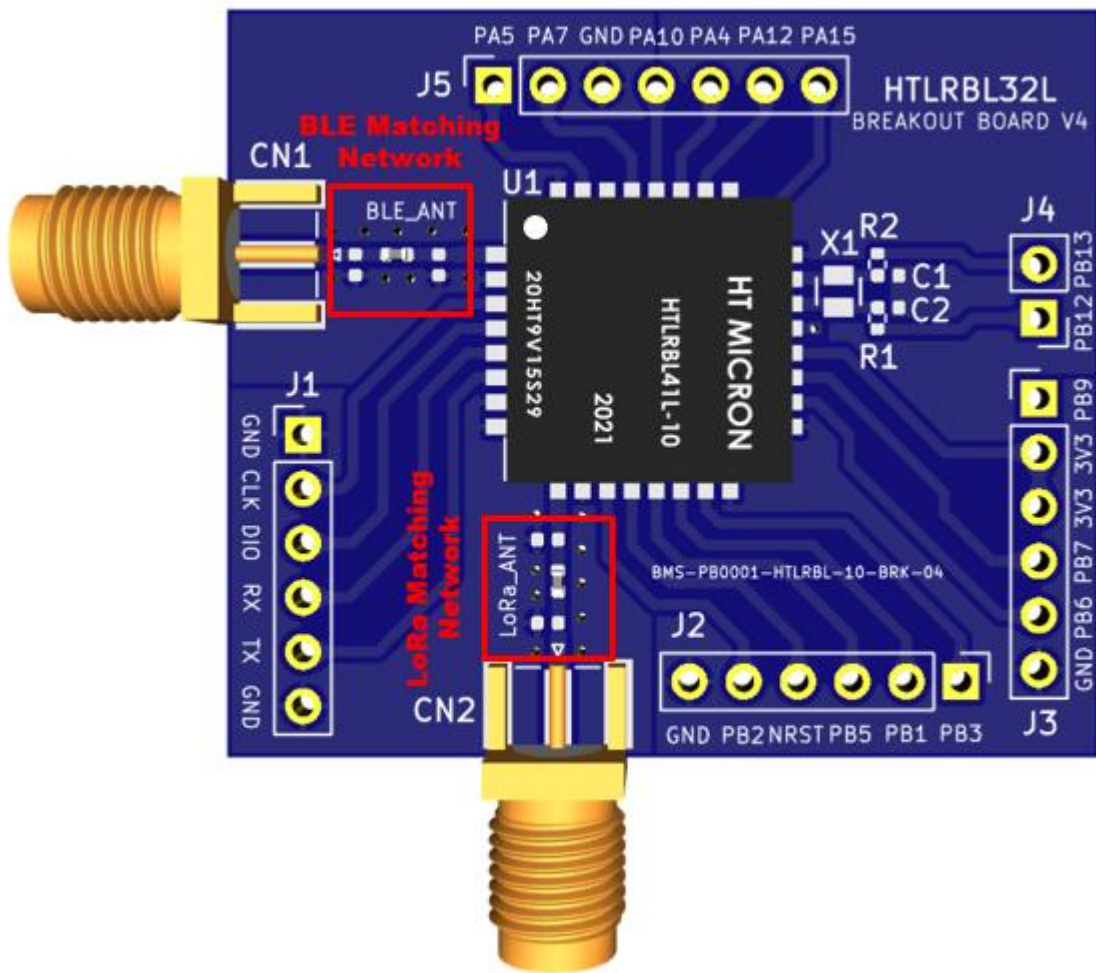Figure 4: BLE and LoRa matching networks area.
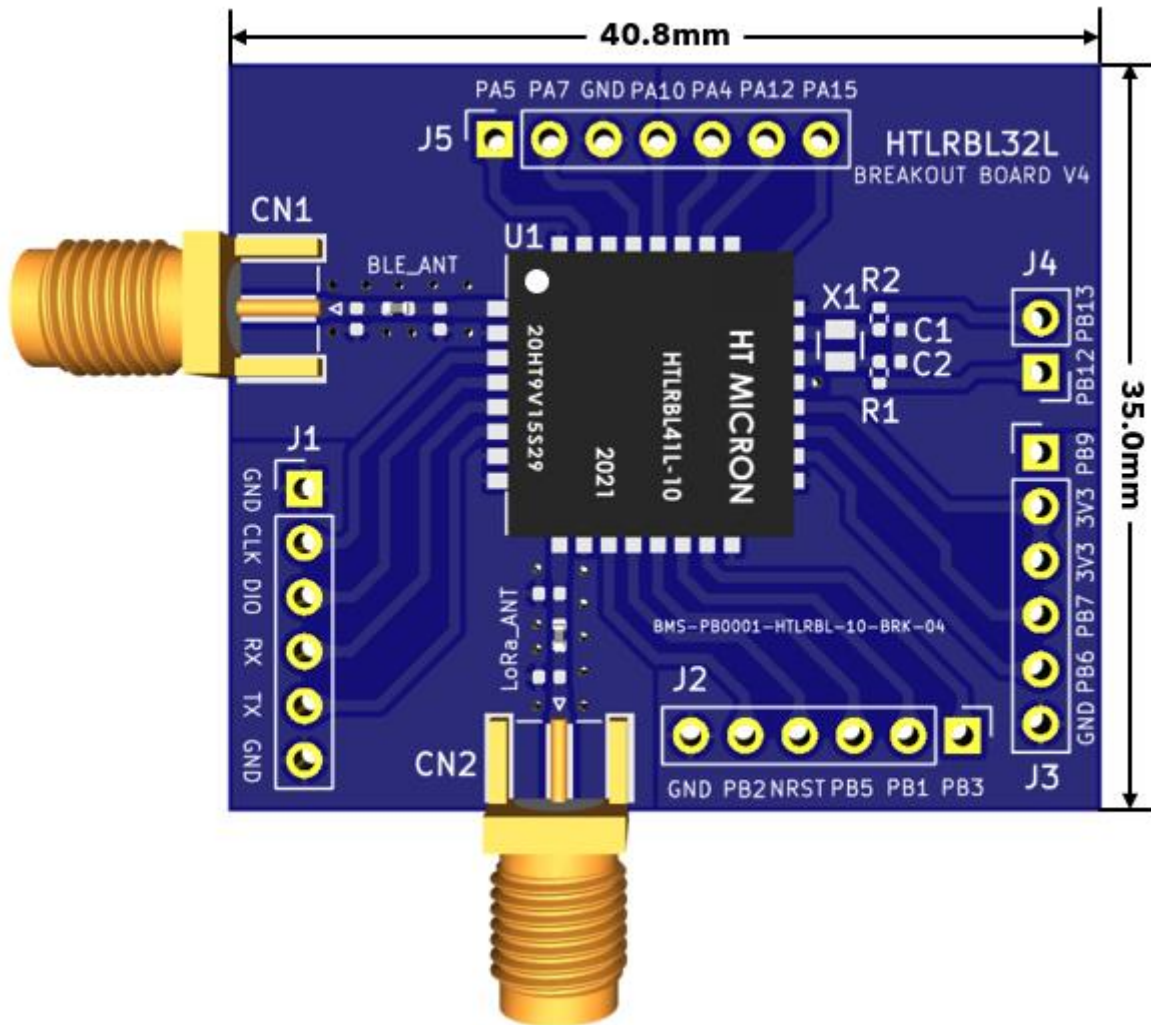
6. BOARD DIMMENSIONS

Figure 5: Board dimensions.

ABBREVIATIONS

Table 6: Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
BLE	Bluetooth Low Energy
CLK	Clock
GPIO	General Purpose Input Output
IO	Input Output
MCU	Microcontroller Unit
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
RF	Radio Frequency
RX	Receiver
SCL	Serial Clock
SDA	Serial Data
SMA	SubMiniature version A
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter

LIST OF FIGURES

LIST OF TABLES

REVISION HISTORY

Version	Date	Changes	Authors
00	03/06/2023	- Initial draft	CL
01	03/08/2023	- First complete version	CL / MC

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