8-Port Serial RapidIO® Switch

Product Brief
80KSW0003

Device Overview

The CPS-8, device number 80KSW0003, is a serial RapidIO switch whose functionality is central to routing packets for distribution among DSPs, processors, FPGAs, other switches, or any other sRIO-based devices. It may also be used in serial RapidIO backplane switching. The CPS-8 supports serial RapidIO packet switching (unicast, multicast, and an optional broadcast) from any of its 8 input ports to any of its 8 output ports.

Features

- **Interfaces - sRIO**
  - *8 bidirectional serial RapidIO (sRIO) lanes v 1.3*
  - *Port Speeds selectable: 3.125Gbps, 2.5Gbps, or 1.25Gbps*
  - *All lanes support short haul or long haul reach for each PHY speed*
  - *Configurable port count to up to eight 1x ports, two 4x ports, or 4 1x and 1 4x ports.*
  - *Lanes can be configured as individual non-redundant 1x ports, as part of a redundant 1x port, or as part of a 4x port*
  - *Supports standard 4 levels of priority*
  - *Error management support*
- **Interfaces - I^2C**
  - *Provides I^2C port for maintenance and error reporting*
  - *Master or Slave Operation*
  - *Master allows power-on configuration from external ROM*
  - *Master mode configuration with external image compressing and checksum*
- **Performance**
  - *20 Gbps of peak switching bandwidth*
  - *Non-blocking data flow architecture within each sRIO priority*
  - *Very low latency for all packet length and load condition*
  - *Internal queuing buffer and retransmit buffer*
  - *Standard receiver based physical layer flow control*
- **Added Features**
  - *Configurable for Cut Through or Store And Forward data flow*
  - *Device configurable through any of sRIO ports, I^2C, or JTAG*
  - *Packet Trace/Mirror/Filter. Per-port line rate copy or filter of all packets matching user compare value. Supports security, sniffing, and diagnostics.*
  - *Supports up to 10 simultaneous multicast masks*
  - *Broadcast support*
  - *Port Loopback Debug Feature*
  - *Software assisted error recovery, supporting hot swap*
  - *Ports may be individually turned off to reduce power*
  - *PMON counters for monitor and diagnostics. Per input port and output port counters*
  - *Serdes physical diagnostic registers*
  - *Embedded PRBS generation and detection with programmable polynomials support Bit Error Rate (BER) testing*
  - *0.13um technology*
  - *Low power dissipation*
- **Package: 324-ball grid array, 19mm x 19mm, 1.0mm ball pitch**

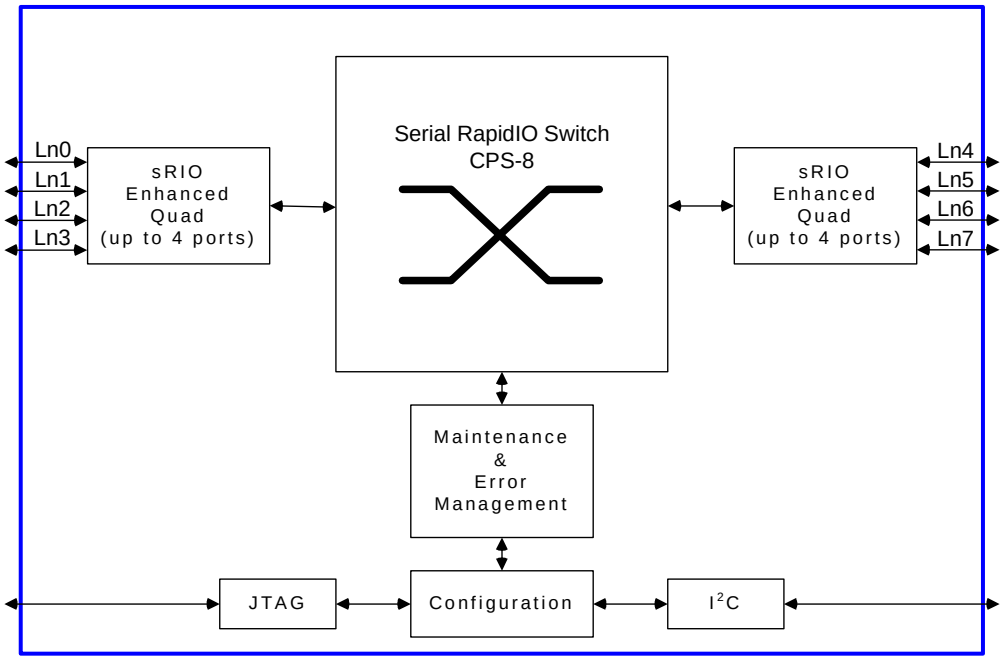
Functional Description

The CPS-8 is optimized for DSP cluster applications at board level. Its main function is to have a backplane interface which can connect to a backplane switch or directly to multiple RF cards. On the line card side it can also connect to multiple ports. It supports up to 8 ports which are configurable as line card, or backplane ports. It is an end-point free (switch) device in an sRIO network.

The CPS-8 receives packets from up to 8 ports. The CPS-8 offers full support for normal switching as well as enhanced functions:

1) Normal Switching: All packets are switched in accordance with standard serial RapidIO specifications, with packet destination IDs determining how the packet is routed.

Block Diagram



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Three major options exist within this category:

a. Multicast: If a Multicast ID is received, the CPS-8 performs a multicast as defined in the sRIO multicast registers.
b. Unicast: All other operations are performed as specified in sRIO.
c. Maintenance packets: As specified by sRIO.

The sRIO Switch supports a peak throughput of 20 Gbps which is the line rate for 8 ports in 1x configuration, each at 2.5 Gbps (3.125 Gbps minus the sRIO-defined 8b10b encoding), and switches dynamically in accordance with the packet headers and priorities.

2) Enhanced Functions

Enhanced features are provided for support of system debug. These features which are optional for the user consist of two major functions:

a. Packet Trace: The Packet Trace feature provides at-speed checking of the first 160 bits (header plus a portion of any payload) of every incoming packet against user-defined comparison register values. The trace feature is available on all serial RapidIO ports, each acting independently from one another. If the trace feature is enabled for a given port, every incoming packet is checked for a match against up to 4 comparison registers. In the event of a match, either of two possible user defined actions may take place:
   i) not only does the packet route normally through the switch to its appropriate destination port, but this same packet is replicated and sent to a "trace port." The trace port itself may be any of the standard serial RapidIO ports. The port used for the trace port is defined by the user through simple register configuration.
   ii) the packet is dropped.

   If there is no match, the packets route normally through the switch with no action taken.

   The Packet Trace feature can be used during system bring-up and prototyping to identify particular packet types of interest to the user. It might be used in security applications, where packets must be checked for either correct or incorrect tags in either of the header or payload. Identified (match) packets are then routed to the trace port for receipt by a host processor, which can perform an intervention at the software level.
b. Port Loopback: The CPS-8 offers internal loopback for each port that may be used for system debug of the high speed sRIO ports. By enabling loopback on a given port, packets sent to the port's receiver are immediately looped back at the physical layer to the transmitter - bypassing the higher logical or transport layers.
c. Broadcast: Each multicast mask can be configured so that the source port is included among the destination ports for that multicast operation.

The CPS-8 can be programmed through any one or combination of sRIO, I^2C, or JTAG. Note that any sRIO port may be used for programming. The CPS-8 can also configure itself on power-up by reading directly from ROM over I^2C in master mode.

CPS in Support of Baseband and Central Switch Boards, Cellular Base Station

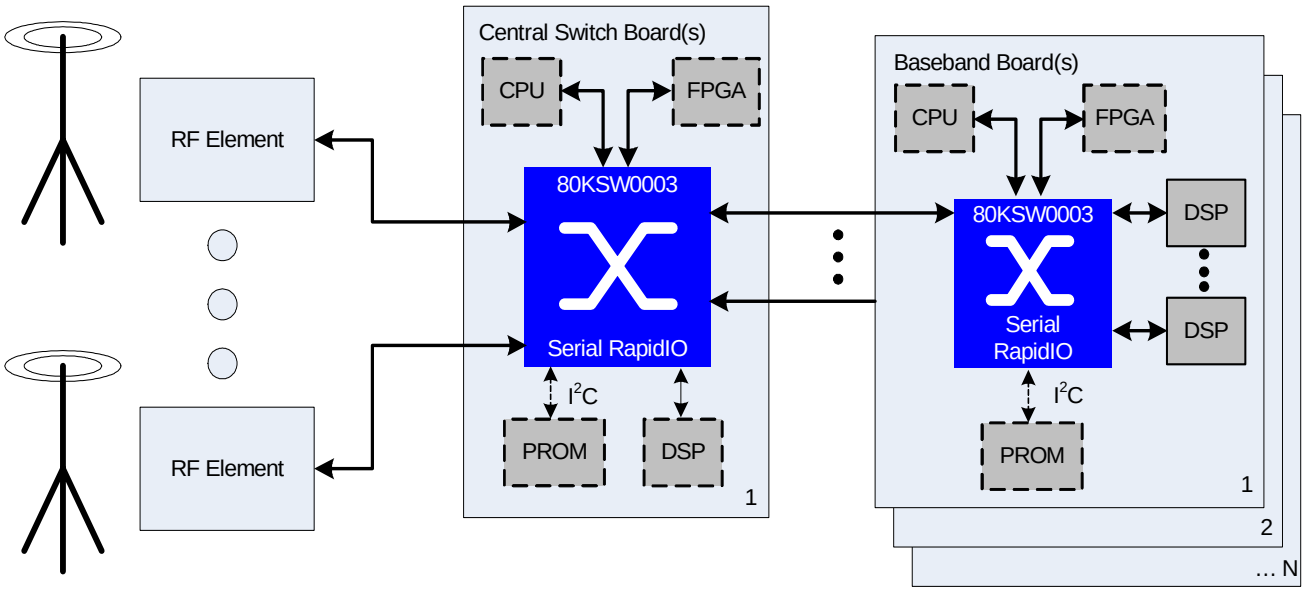

Figure 1 Application Overview

Note: The CPS-8 provides direct support for backplane connections using the serial RapidIO standard. The addition of an appropriate bridge (e.g., CPRI ↔ sRIO) allows for further backplane flexibility, accommodating designs based on a wide range of standards such as CPRI, OBSAI, GbE or PCIe.

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