TVS Diodes
Transient Voltage Suppressor Diodes

**ESD5V3U1U Series**
Uni-directional Ultra-Low Capacitance ESD / Transient Protection Diode

ESD5V3U1U-02LS
ESD5V3U1U-02LRH

Data Sheet
Revision 1.0, 2011-05-27
Final
Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.
# Revision History

<table>
<thead>
<tr>
<th>Page or Item</th>
<th>Subjects (major changes since previous revision)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 1.0, 2011-05-27</td>
<td></td>
</tr>
</tbody>
</table>

# Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, COMNEON™, C166™, CROSSAVE™, CanPAK™, CIPOS™, CoolMOS™, CoolSET™, CORECONTROL™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, EUPEC™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, I²RF™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PROFET™, PRO-SIL™, PRIMARION™, PrimePACK™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SMARTi™, SmartLEWIS™, TEMPFET™, thinQ!™, TriCore™, TRENCHSTOP™, X-GOLD™, XMM™, X-PMU™, XPOSYS™.

# Other Trademarks


Last Trademarks Update 2010-06-09
Table of Contents

Table of Contents .......................................................... 4
List of Figures ................................................................. 5
List of Tables ................................................................. 6
1 Uni-directional Ultra-Low Capacitance ESD / Transient Protection Diode .................. 7
1.1 Features ................................................................. 7
1.2 Application Examples .................................................. 7
2 Product Description ....................................................... 7
3 Characteristics ............................................................. 8
3.1 Electrical Characteristics at $T_A = 25^\circ$C, unless otherwise specified .............. 8
3.2 Typical Characteristics at $T_A=25^\circ$C, unless otherwise specified .................. 10
4 Application Information .................................................. 15
5 Ordering Information Scheme (Examples) .................................. 16
6 Package Information ....................................................... 17
6.1 PG-TSSLP-2-1 (mm)[3] ................................................ 17
6.2 PG-TSLP-2-7 (mm)[3] .................................................. 18
Terminology ........................................................................ 19
References ......................................................................... 20
List of Figures

Figure 1  Pin Configuration and Schematic Diagram .......................................................... 7
Figure 2  Definitions of Electrical Characteristics ............................................................... 8
Figure 3  Reverse current $I_R = f(T_A) \cdot V_R = 5.3$ V, from pin 1 to pin 2 ......................... 10
Figure 4  Line capacitance $C_L = f(f_R), f = 1$MHz, from pin 1 to pin 2 ............................ 10
Figure 5  Line capacitance $C_L = f(f)$, from pin 1 to pin 2 .............................................. 11
Figure 6  Line capacitance $C_L = f(T_A)$, from pin 1 to pin 2 ............................................ 11
Figure 7  Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 1 to pin 2[1] ............................... 12
Figure 8  Forward clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 2 to pin 1[1] ....................... 12
Figure 9  IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2 .................... 13
Figure 10 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2 .................... 13
Figure 11 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2 .................... 14
Figure 12 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2 .................... 14
Figure 13 Single line, uni-directional ESD / Transient protection[2] ..................................... 15
Figure 14 Ordering information scheme .......................................................... 16
Figure 15 PG-TSSL-2-1: Package overview .......................................................... 17
Figure 16 PG-TSSL-2-1: Footprint ........................................................................ 17
Figure 17 PG-TSSL-2-1: Packing .......................................................................... 17
Figure 18 PG-TSSL-2-1: Marking (example) ........................................................ 17
Figure 19 PG-TSLP-2-7: Package Overview .......................................................... 18
Figure 20 PG-TSLP-2-7: Footprint ........................................................................ 18
Figure 21 PG-TSLP-2-7: Packing .......................................................................... 18
Figure 22 PG-TSLP-2-7: Marking (example) ........................................................ 18
List of Tables

Table 1  Ordering Information .................................................. 7
Table 2  Maximum Rating at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified .................. 8
Table 3  DC Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified .................. 8
Table 4  RF Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified ................. 9
Table 5  ESD Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified ................. 9
1  Uni-directional Ultra-Low Capacitance ESD / Transient Protection Diode

1.1  Features

- ESD / Transient protection of high speed data lines exceeding
  - IEC61000-4-2 (ESD): ±20 kV (air / contact)
  - IEC61000-4-4 (EFT): 2.5 kV / 50 A (5/50 ns)
  - IEC61000-4-5 (surge): 3 A (8/20 μs)
- Maximum working voltage: $V_{RWM} = 5.3$ V
- Ultra low capacitance: $C_L = 0.4$ pF (typical)
- Low clamping voltage, low dynamic resistance $R_{DYN} = 0.6$ Ω (typical)
- Very small form factor down to 0.62 x 0.32 x 0.31 mm$^3$
- Pb-free (RoHS compliant) and halogen free package

1.2  Application Examples

- USB 2.0, Mobile HDMI Link, MDDI, MIPI, etc.
- HDMI, DisplayPort, DVI, Ethernet, Firewire, S-ATA

2  Product Description

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Configuration</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD5V3U1U-02LS</td>
<td>PG-TSSLP-2-1</td>
<td>1 line, uni-directional</td>
<td>L</td>
</tr>
<tr>
<td>ESD5V3U1U--02LRH</td>
<td>PG-TSLP-2-7</td>
<td>1 line, uni-directional</td>
<td>E5</td>
</tr>
</tbody>
</table>
3 Characteristics

Table 2 Maximum Rating at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD (air / contact) discharge$^{1)}$</td>
<td>$V_{ESD}$</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Peak pulse current ($t_p = 8/20 , \mu\text{s}$)</td>
<td>$I_{PP}$</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>$T_{OP}$</td>
<td>–</td>
<td>125</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{STG}$</td>
<td>–</td>
<td>150</td>
</tr>
</tbody>
</table>

1) $V_{ESD}$ according to IEC61000-4-2
2) $I_{PP}$ according to IEC61000-4-5

3.1 Electrical Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

![Diode_Characteristic_Curve_Unidirectional.vsd](image)

Figure 2 Definitions of Electrical Characteristics

Table 3 DC Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse working voltage</td>
<td>$V_{RWM}$</td>
<td>–</td>
<td>5.3</td>
<td>Pin 1 to Pin 2</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>$V_{BR}$</td>
<td>6</td>
<td>–</td>
<td>$I_{BR} = 1 , \text{mA}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_R$</td>
<td>–</td>
<td>100</td>
<td>$V_R = 5.3 , \text{V}$, from Pin 1 to Pin 2</td>
</tr>
</tbody>
</table>
### Table 4  RF Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line capacitance</td>
<td>$C_L$</td>
<td>$0.4$</td>
<td>$0.6$</td>
<td>$V_R = 0 , \text{V}, f = 1 , \text{MHz}$</td>
</tr>
<tr>
<td>Serie inductance</td>
<td>$L_S$</td>
<td>$0.2$</td>
<td>$0.4$</td>
<td>$V_{PP} = 30 , \text{A}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{PP} = 16 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{PP} = 30 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
</tbody>
</table>

1) Total capacitance line to ground

### Table 5  ESD Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping voltage</td>
<td>$V_{CL}$</td>
<td>$19$</td>
<td>$28$</td>
<td>$I_{pp} = 16 , \text{A}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td>Forward clamping voltage</td>
<td>$V_{FC}$</td>
<td>$10$</td>
<td>$17$</td>
<td>$I_{pp} = 16 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
<tr>
<td>Dynamic resistance</td>
<td>$R_{DYN}$</td>
<td>$0.6$</td>
<td>$0.5$</td>
<td>$I_{pp} = 30 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
</tbody>
</table>

1) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50 \, \Omega$, $t_p = 100\text{ns}$, $t_r = 300\text{ps}$, averaging window: $t_1 = 30 \, \text{ns}$ to $t_2 = 60 \, \text{ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{pp1} = 10 \, \text{A}$ and $I_{pp2} = 40 \, \text{A}$.
3.2 **Typical Characteristics** at $T_A=25^\circ\text{C}$, unless otherwise specified

**Figure 3** Reverse current $I_R = f(T_A)$, $V_R = 5.3 \text{ V}$, from pin 1 to pin 2

**Figure 4** Line capacitance $C_L = f(V_R)$, $f = 1\text{MHz}$, from pin 1 to pin 2
Figure 5  Line capacitance $C_L = f(f)$, from pin 1 to pin 2

Figure 6  Line capacitance $C_L = f(T_A)$, from pin 1 to pin 2
Figure 7  Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 1 to pin 2[1]

Figure 8  Forward clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 2 to pin 1[1]
Figure 9  IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

- $V_{CL\text{-max-peak}} = 82.2$ [V]
- $V_{CL\text{-30ns-peak}} = 17.3$ [V]

Figure 10  IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

- $V_{CL\text{-max-peak}} = -76.1$ [V]
- $V_{CL\text{-30ns-peak}} = -8.9$ [V]
Figure 11  IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

$V_{CL\text{-max-peak}} = 104.8$ [V]

$V_{CL\text{-30ns-peak}} = 24.1$ [V]

Figure 12  IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

$V_{CL\text{-max-peak}} = -105.1$ [V]

$V_{CL\text{-30ns-peak}} = -13.7$ [V]
4 Application Information

The protection diode should be placed very close to the location where the ESD or other transients can occur to keep loops and inductances as small as possible. Pin 2 should be connected directly to a ground plane on the board.

Figure 13 Single line, uni-directional ESD / Transient protection[2]
5 Ordering Information Scheme (Examples)

ESD 0P1 RF - XX YY

- Package
  XX = Pin number (i.e.: 02 = 2 pins; 03 = 3 pins)
  YY = Package family:
  LS = TSSLP
  LRH = TSLP

- For Radio Frequency Applications

- Line Capacitance \( C_L \) in pF: (i.e.: 0P1 = 0.1pF)

ESD 5V3 Un U - XX YY

- Package or Application
  XX = Pin number (i.e.: 02 = 2 pins; 03 = 3 pins)
  YY = Package family:
  LS = TSSLP
  LRH = TSLP
  S = SOT363
  U = SC74

- XX = Application family
  LC = Low Clamp
  HDMI

- Unipolar / Bipolar directional or Rail to Rail protection

- Number of protected lines (i.e.: 1 = 1 line; 4 = 4 lines)

- Capacitance: Standard (>10pF), Low (<10pF), Ultra-low (<1pF)

- Maximum working voltage \( V_{RWM} \) in V: (i.e.: 5V3 = 5.3V)

Figure 14 Ordering information scheme
6 Package Information

6.1 PG-TSSLP-2-1 (mm)[3]

Figure 15 PG-TSSLP-2-1: Package overview

Figure 16 PG-TSSLP-2-1: Footprint

Figure 17 PG-TSSLP-2-1: Packing

Figure 18 PG-TSSLP-2-1: Marking (example)
6.2 PG-TSLP-2-7 (mm)[3]

1) Dimension applies to plated terminal

Figure 19 PG-TSLP-2-7: Package Overview

Figure 20 PG-TSLP-2-7: Footprint

Figure 21 PG-TSLP-2-7: Packing

Figure 22 PG-TSLP-2-7: Marking (example)
**Terminology**

- $C_L$: Line capacitance
- DVI: Digital Visual Interface
- EFT: Electrical Fast Transient
- ESD: Electrostatic Discharge
- HDMI: High Definition Multimedia Interface
- IEC: International Electrotechnical Commission
- $I_{pp}$: Peak pulse current
- $I_R$: Reverse current
- $I_{RWM}$: Maximum Reverse working Current
- $L_S$: Serial inductance
- MDDI: Mobile Display Digital Interface
- MIPI: Mobile Industrial Processor Interface
- RoHS: Restriction of Hazardous Substances Directive
- S-ATA: Serial Advanced Technology Attachment
- $T_A$: Ambient temperature
- $T_{OP}$: Operation temperature
- $t_p$: Pulse duration
- $T_{stg}$: Storage temperature
- USB: Universal Serial Bus
- $V_{BR}$: Breakdown Voltage
- $V_{CL}$: Reverse clamping voltage
- $V_{ESD}$: Electrostatic discharge voltage
- $V_{FC}$: Forward Clamping Voltage
- $V_R$: Reverse voltage
- $V_{RWM}$: Maximum Reverse Working Voltage
References

[1] Infineon AG - Application Note AN210: Effective ESD Protection Design at System Level Using VF-TLP

[2] Infineon AG - Application Note AN140: ESD Protection for Digital High-Speed Interfaces (HDMI, FireWire, ...) using ESD5V3U1U)

[3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package