**DESCRIPTION**

The MP1484 is a monolithic synchronous buck regulator. The device integrates top and bottom 85mΩ MOSFETs that provide 3A of continuous load current over a wide operating input voltage of 4.75V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on and in shutdown mode, the supply current drops below 1μA.

The MP1484 is PIN compatible to the MP1482 2A/18V/Synchronous Step-Down Converter.

**FEATURES**

- 3A Continuous Output Current
- Wide 4.75V to 18V Operating Input Range
- Integrated 85mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 20V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Thermally Enhanced 8-Pin SOIC Package

**APPLICATIONS**

- FPGA, ASIC, DSP Power Supplies
- LCD TV
- Green Electronics/Appliances
- Notebook Computers

*MPS* and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

**TYPICAL APPLICATION**

![Efficiency vs Load Current](image)

**Efficiency vs Load Current**

- V_IN = 12V
- V_IN = 5V
- V_OUT = 3.3V
- L = 10μH

![Typical Application Circuit](image)
PACKAGE REFERENCE

<table>
<thead>
<tr>
<th>Top View</th>
</tr>
</thead>
<tbody>
<tr>
<td>BS</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>SS</td>
</tr>
<tr>
<td>8</td>
</tr>
</tbody>
</table>

EXPOSED PAD ON BACKSIDE CONNECT TO GND PIN

ABSOLUTE MAXIMUM RATINGS (1)
Supply Voltage $V_{IN}$....................... –0.3V to +24V
Switch Voltage $V_{SW}$....................... –1V to $V_{IN}$ + 0.3V
Boost Voltage $V_{BS}$....................... $V_{SW}$ – 0.3V to $V_{SW}$ + 6V
All Other Pins................................. –0.3V to +6V
Junction Temperature...............................150°C
Lead Temperature ....................................260°C
Storage Temperature .............–65°C to +150°C

Recommended Operating Conditions (2)
Input Voltage $V_{IN}$.................4.75V to 18V
Output Voltage $V_{OUT}$ ...............0.925V to 20V
Ambient Operating Temp .......... –20°C to +85°C

Thermal Resistance (3) $\theta_{JA}$ $\theta_{JC}$
SOIC8N(Exposed Pad) ........50 ...... 10... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1” square of 1 oz copper.

ELECTRICAL CHARACTERISTICS
$V_{IN}$ = 12V, $T_A$ = +25°C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown Supply Current</td>
<td>$V_{EN}$</td>
<td>$V_{EN}$ = 0V</td>
<td>0.3</td>
<td>3.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td></td>
<td>$V_{EN}$ = 2.0V, $V_{FB}$ = 1.0V</td>
<td>1.3</td>
<td>1.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Feedback Voltage</td>
<td>$V_{FB}$</td>
<td>4.75V ≤ $V_{IN}$ ≤ 18V</td>
<td>0.900</td>
<td>0.925</td>
<td>0.950</td>
<td>V</td>
</tr>
<tr>
<td>Feedback Overvoltage Threshold</td>
<td></td>
<td></td>
<td>1.1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Error Amplifier Voltage Gain (4)</td>
<td>$A_{EA}$</td>
<td></td>
<td>400</td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>Error Amplifier Transconductance (4)</td>
<td>$G_{EA}$</td>
<td>$\Delta I_C = \pm 10\mu A$</td>
<td>820</td>
<td></td>
<td>µA/V</td>
<td></td>
</tr>
<tr>
<td>High-Side/Low-Side Switch On-Resistance (4)</td>
<td></td>
<td></td>
<td>85</td>
<td></td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>High-Side Switch Leakage Current</td>
<td></td>
<td>$V_{EN}$ = 0V, $V_{SW}$ = 0V</td>
<td>0</td>
<td>10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Upper Switch Current Limit</td>
<td>Minimum Duty Cycle</td>
<td></td>
<td>3.8</td>
<td>5.3</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Lower Switch Current Limit</td>
<td>From Drain to Source</td>
<td></td>
<td>0.9</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>COMP to Current Sense Transconductance</td>
<td>$G_{CS}$</td>
<td></td>
<td>5.2</td>
<td></td>
<td>A/V</td>
<td></td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>$F_{osc1}$</td>
<td></td>
<td>300</td>
<td>340</td>
<td>380</td>
<td>KHz</td>
</tr>
<tr>
<td>Short Circuit Oscillation Frequency</td>
<td>$F_{osc2}$</td>
<td>$V_{FB}$ = 0V</td>
<td>110</td>
<td></td>
<td>KHz</td>
<td></td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>$D_{MAX}$</td>
<td>$V_{FB}$ = 1.0V</td>
<td>90</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Minimum On Time (4)</td>
<td>$T_{ON}$</td>
<td></td>
<td>220</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>EN Shutdown Threshold Voltage</td>
<td>$V_{EN}$ Rising</td>
<td></td>
<td>1.1</td>
<td>1.5</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>EN Shutdown Threshold Voltage Hysteresis</td>
<td></td>
<td></td>
<td>220</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS (continued)

\( V_{\text{IN}} = 12\,\text{V}, \, T_{\text{A}} = +25^\circ\text{C}, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN Lockout Threshold Voltage</td>
<td></td>
<td></td>
<td>2.2</td>
<td>2.5</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>EN Lockout Hysterisis</td>
<td></td>
<td></td>
<td>210</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Input Under Voltage Lockout Threshold</td>
<td></td>
<td>( V_{\text{IN}} ) Rising</td>
<td>3.80</td>
<td>4.05</td>
<td>4.40</td>
<td>V</td>
</tr>
<tr>
<td>Input Under Voltage Lockout Threshold Hysterisis</td>
<td></td>
<td></td>
<td>210</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Soft-Start Current</td>
<td></td>
<td>( V_{\text{SS}} = 0,\text{V} )</td>
<td>6</td>
<td></td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>Soft-Start Period</td>
<td></td>
<td>( C_{\text{SS}} = 0.1,\mu\text{F} )</td>
<td>15</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td></td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>( ^\circ\text{C} )</td>
</tr>
</tbody>
</table>

Note:

4) Guaranteed by design, not tested.

PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BS</td>
<td>High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01( \mu\text{F} ) or greater capacitor from SW to BS to power the high-side switch.</td>
</tr>
<tr>
<td>2</td>
<td>IN</td>
<td>Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75,\text{V} to 18,\text{V} power source. See Input Capacitor.</td>
</tr>
<tr>
<td>3</td>
<td>SW</td>
<td>Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground (Connect the exposed pad to Pin 4).</td>
</tr>
<tr>
<td>5</td>
<td>FB</td>
<td>Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925,\text{V}. See Setting the Output Voltage.</td>
</tr>
<tr>
<td>6</td>
<td>COMP</td>
<td>Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See Compensation Components.</td>
</tr>
<tr>
<td>7</td>
<td>EN</td>
<td>Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100,k\Omega pull up resistor for automatic startup.</td>
</tr>
<tr>
<td>8</td>
<td>SS</td>
<td>Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1,\mu\text{F} capacitor sets the soft-start period to 15,\text{ms}. To disable the soft-start feature, leave SS unconnected.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

C1 = 4.7μF, C2 = 2 x 10μF, L= 10μH, CSS= 0.1μF, TA = +25°C, unless otherwise noted.

Steady State Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

Steady State Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A

Startup through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

Shutdown Through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

Shutdown Through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

Load Transient Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A to 3A

Short Circuit Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V

Short Circuit Recovery Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V
OPERATION

FUNCTIONAL DESCRIPTION

The MP1484 regulates input voltages from 4.75V to 18V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The MP1484 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current (measured internally) to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the FB pin voltage exceeds 20% of the nominal regulation value of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

Figure 1—Functional Block Diagram
APPLICATIONS INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

\[ V_{FB} = V_{OUT} \frac{R2}{R1 + R2} \]

Thus the output voltage is:

\[ V_{OUT} = 0.925 \times \frac{R1 + R2}{R2} \]

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

\[ R1 = 10.81 \times (V_{OUT} - 0.925) \ (\text{kΩ}) \]

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ. Table 1 lists recommended resistance values of R1 and R2 for standard output voltages.

Table 1—Recommended Resistance Values

<table>
<thead>
<tr>
<th>VOUT</th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8V</td>
<td>9.53kΩ</td>
<td>10kΩ</td>
</tr>
<tr>
<td>2.5V</td>
<td>16.9kΩ</td>
<td>10kΩ</td>
</tr>
<tr>
<td>3.3V</td>
<td>26.1kΩ</td>
<td>10kΩ</td>
</tr>
<tr>
<td>5V</td>
<td>44.2kΩ</td>
<td>10kΩ</td>
</tr>
<tr>
<td>12V</td>
<td>121kΩ</td>
<td>10kΩ</td>
</tr>
</tbody>
</table>

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

\[ L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \]

Where \( V_{OUT} \) is the output voltage, \( V_{IN} \) is the input voltage, \( f_s \) is the switching frequency, and \( \Delta I_L \) is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

\[ I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \]

Where \( I_{LOAD} \) is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2—Diode Selection Guide

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Voltage/Current Rating</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>B130</td>
<td>30V, 1A</td>
<td>Diodes, Inc.</td>
</tr>
<tr>
<td>SK13</td>
<td>30V, 1A</td>
<td>Diodes, Inc.</td>
</tr>
<tr>
<td>MBRS130</td>
<td>30V, 1A</td>
<td>International Rectifier</td>
</tr>
</tbody>
</table>

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.
Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

\[ I_{C1} = I_{LOAD} \times \frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \]

The worst-case condition occurs at \( V_{IN} = 2V_{OUT} \), where \( I_{C1} = I_{LOAD}/2 \). For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1 \( \mu \)F, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

\[ \Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_s} \times \frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \]

Where \( C1 \) is the input capacitance value.

**Output Capacitor**

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Under typical application conditions, a minimum ceramic capacitor value of 20 \( \mu \)F is recommended on the output. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

\[ \Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} + \frac{1}{8 \times f_s \times C2} \]

Where \( C2 \) is the output capacitance value and \( R_{ESR} \) is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

\[ \Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \]

Where \( G_{EA} \) is the error amplifier transconductance.
The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

\[ f_{Z1} = \frac{1}{2\pi \times C3 \times R3} \]

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

\[ f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}} \]

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

\[ f_{P3} = \frac{1}{2\pi \times C6 \times R3} \]

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine R3 by the following equation:

\[ R3 = \frac{2\pi \times C2 \times f_C \times V_{OUT}}{G_{EA} \times G_{CS} \times V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_S \times V_{OUT}}{G_{EA} \times G_{CS} \times V_{FB}} \]

Where \( f_C \) is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero \( (f_{Z1}) \) below one-forth of the crossover frequency provides sufficient phase margin.

Determine C3 by the following equation:

\[ C3 > \frac{4}{2\pi \times R3 \times f_C} \]

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

\[ \frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2} \]

If this is the case, then add the second compensation capacitor (C6) to set the pole \( f_{P3} \) at the location of the ESR zero. Determine C6 by the equation:

\[ C6 = \frac{C2 \times R_{ESR}}{R3} \]

**External Bootstrap Diode**

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BS diode are:

- \( V_{OUT} \) is 5V or 3.3V; and
- Duty cycle is high: \( D = \frac{V_{OUT}}{V_{IN}} > 65\% \)

In these cases, an external BS diode is recommended from the output of the voltage regulator to BS pin, as shown in Fig.2

![Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency](image)

The recommended external BS diode is IN4148, and the BS cap is 0.1~1\( \mu \)F.
Figure 3—MP1484 with 3.3V Output, 2X10μF Ceramic Output Capacitor
PCB LAYOUT GUIDE

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 4 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET.

2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) Rout SW away from sensitive analog areas such as FB.

5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

Figure 4—MP1484 Typical Application Circuit and PCB Layout Guide
**PACKAGE INFORMATION**

**SOIC8N (EXPOSED PAD)**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**RECOMMENDED LAND PATTERN**

**NOTE:**

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

**NOTICE:** The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.