The Motorola DSP56L307, a member of the DSP56300 family of programmable Digital Signal Processors (DSPs), supports network applications with general filtering operations. The on-chip Enhanced Filter Coprocessor (EFCOP) executes filter algorithms in parallel with core operations to provide enhanced signal quality without affecting channel throughput or total number of channels supported, resulting in increased overall performance. Like the other family members, the DSP56L307 uses a high-performance, single clock cycle per instruction engine, a barrel shifter, 24-bit addressing, instruction cache, and Direct Memory Access (DMA) controller. The DSP56L307 offers 160 MIPS performance (290 MIPS using the EFCOP in filtering applications) using an internal 160 MHz clock, a 1.8 V core, and independent 3.3 V Input/Output (I/O).

![Figure 1 DSP56L307 Block Diagram](image-url)
FEATURES

- High-performance DSP56300 core:
  - 160 Million Instructions Per Second (MIPS) (290 MIPS using the EFCOP in filtering applications) with a 160 MHz clock at 1.8 V
  - Object code compatible with the DSP56000 core with highly parallel instruction set
  - Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
  - Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), on-chip instruction, cache controller, on-chip memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
  - Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
  - Phase Lock Loop (PLL) allows change of low-power Divide Factor (DF) without loss of lock
  - Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

- On-chip memories and off-chip memory expansion:
  - 64 K on-chip RAM total
  - Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

<table>
<thead>
<tr>
<th>Program RAM Size</th>
<th>Instruction Cache Size</th>
<th>X Data RAM Size*</th>
<th>Y Data RAM Size*</th>
<th>Instruction Cache</th>
<th>Switch Mode</th>
<th>MSW1</th>
<th>MSW0</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 K × 24 bits</td>
<td>0</td>
<td>24 K × 24 bits</td>
<td>24 K × 24 bits</td>
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<td>disabled</td>
<td>0/1</td>
<td>0/1</td>
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<tr>
<td>15 K × 24 bits</td>
<td>1024 × 24 bits</td>
<td>24 K × 24 bits</td>
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<td>disabled</td>
<td>0/1</td>
<td>0/1</td>
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<td>8 K × 24 bits</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>47 K × 24 bits</td>
<td>1024 × 24 bits</td>
<td>8 K × 24 bits</td>
<td>8 K × 24 bits</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>40 K × 24 bits</td>
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<td>12 K × 24 bits</td>
<td>12 K × 24 bits</td>
<td>disabled</td>
<td>enabled</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>39 K × 24 bits</td>
<td>1024 × 24 bits</td>
<td>12 K × 24 bits</td>
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<td>enabled</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
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<td>0</td>
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<tr>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>24 K × 24 bits</td>
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<td>20 K × 24 bits</td>
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<td>enabled</td>
<td>enabled</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

*Includes 4 K × 24-bit shared memory (that is, memory shared by the core and the EFCOP)
  - 192 x 24-bit bootstrap ROM
• Enhanced Filter Coprocessor (EFCOP), an on-chip 24 x 24-bit filtering and echo-cancellation coprocessor that runs in parallel to the DSP core

• Off-chip memory expansion:
  — Data memory expansion to two 256 K x 24-bit word memory spaces using the standard external address lines
  — Program memory expansion to one 256 K x 24-bit word memory space using the standard external address lines
  — External memory expansion port
  — Chip select logic for glueless interface to SRAMs

• On-chip peripherals:
  — 3.3 V I/O interface
  — Enhanced DSP56000-like 8-bit parallel Host Interface (HI08) supports a variety of buses (e.g., ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs
  — Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1), each with one receiver and three transmitters
  — Serial Communications Interface (SCI) with baud-rate generator
  — Triple timer module
  — Up to thirty-four programmable General-Purpose Input/Output (GPIO) pins, depending on which peripherals are enabled

• Reduced power dissipation:
  — Very low-power CMOS design
  — Wait and Stop low-power standby modes
  — Fully static design specified to operate down to 0 Hz (DC)
  — Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

• Packaging: 196-pin MAP-BGA

TARGET APPLICATIONS

DSP56L307 applications require high performance, low power, small packaging, and a large amount of on-chip memory—for example, wireless and wireline infrastructure applications, multi-channel wireless local loop systems, DSP resource boards, and high-speed modem banks. The EFCOP can accelerate general filtering applications, such as echo-cancellation applications, correlation, and general-purpose convolution-based algorithms.
PRODUCT DOCUMENTATION

The three manuals listed in Table 1. are required for a complete description of the DSP56L307 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center. For documentation updates, visit our Web site. See the contact information below.

Table 1.  DSP56L307 Documentation

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Order Number</th>
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<tbody>
<tr>
<td>DSP56300 Family Manual</td>
<td>Detailed description of the DSP56300 family processor core and instruction set</td>
<td>DSP56300FM/AD</td>
</tr>
<tr>
<td>DSP56L307 Technical Data</td>
<td>DSP56L307 features list and physical, electrical, timing, and package specifications</td>
<td>DSP56L307/D</td>
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