ISD8102 / ISD8104

2W Class-AB Audio Amplifier

with Chip Enable

Preliminary

2 Different Bonding Configurations:

i) ISD8102 - Headphone Sense IN (SE / Diff)

ii) ISD8104 - Differential Input pair

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1 GENERAL DESCRIPTION

The **ISD8102/ ISD8104 (bonding option)** is a general purpose analog audio amplifier, which is capable of driving a 4-ohm load with up to 2Wrms output power. This device includes current limiting and a chip enable pin with extremely low standby current and excellent pop-and-click suppression.

Also included is the ability to be configured with either single-ended or differential inputs. Internal resistors set the device to have default 20dB gain (ISD8102/ISD8104), and with external resistors any gain less than this can be achieved. The device is unity gain stable, including use with external feedback resistors and external capacitors as may be optionally used for implementing simple filtering functions.

ISD8102:

ISD8102 has a special function to choose SE/BTL outputs, which is useful in Headphone Sense Input applications, and its internal gain setting is 20dB. SE is used to drive the Headphone load; otherwise, BTL is used to drive the speaker load as low as 4Ω.

ISD8104:

ISD8104 can have Single-Ended / Differential inputs, and its internal gain setting is 20dB.

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2 FEATURES

- 2 Different Bonding Options
- Wide power supply range and excellent standby current
  - 2.0Vdc - 6.8Vdc operation
  - <1uA standby current
- High power output (capless BTL configuration)
  - Up to 2-W output into 4-ohm load (<10% distortion) with 5Vdc supply voltage
  - < 0.1% distortion at 600mW into 8-ohms with 5Vdc supply voltage
- Robust High Power Operation and Protection Features
  - Package option for SOP-8 with integrated metal thermal heatsink pad
  - Current limiting for over-current conditions
- Excellent pop-and-click performance
  - Low to inaudible pop/click using Chip Enable
- Single-Ended or Differential signal inputs
  - > 75dB common mode rejection in differential mode
  - > 70dB power supply noise rejection
- Very fast start-up time
  - Less than 1msec when using Chip Enable
- Suitable for a wide range of applications
- Less BOM cost / Easy PCB layout
- Package options: Pb-free SOP-8, SOP-8 (Ex-Pad)
- Temperature Range: -40°C to +85°C

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3 BLOCK DIAGRAM

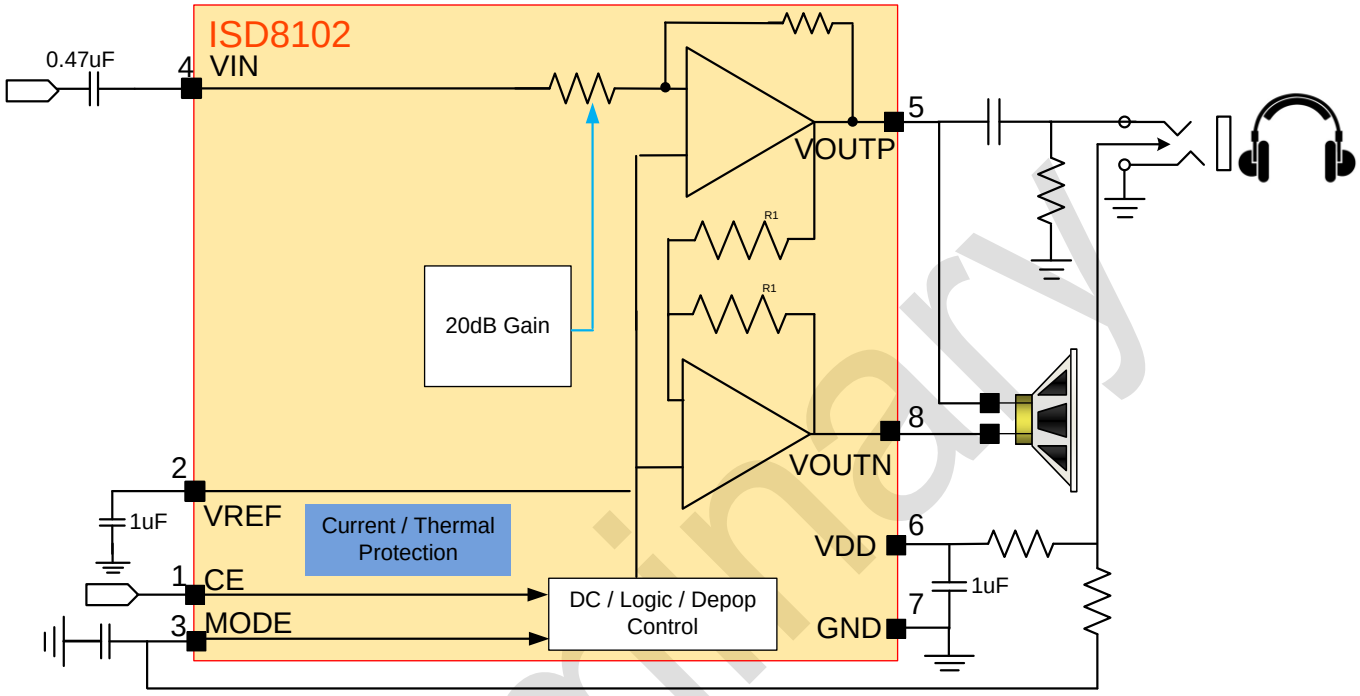

Figure 3-1 ISD8102 Headphone Configuration Block Diagram

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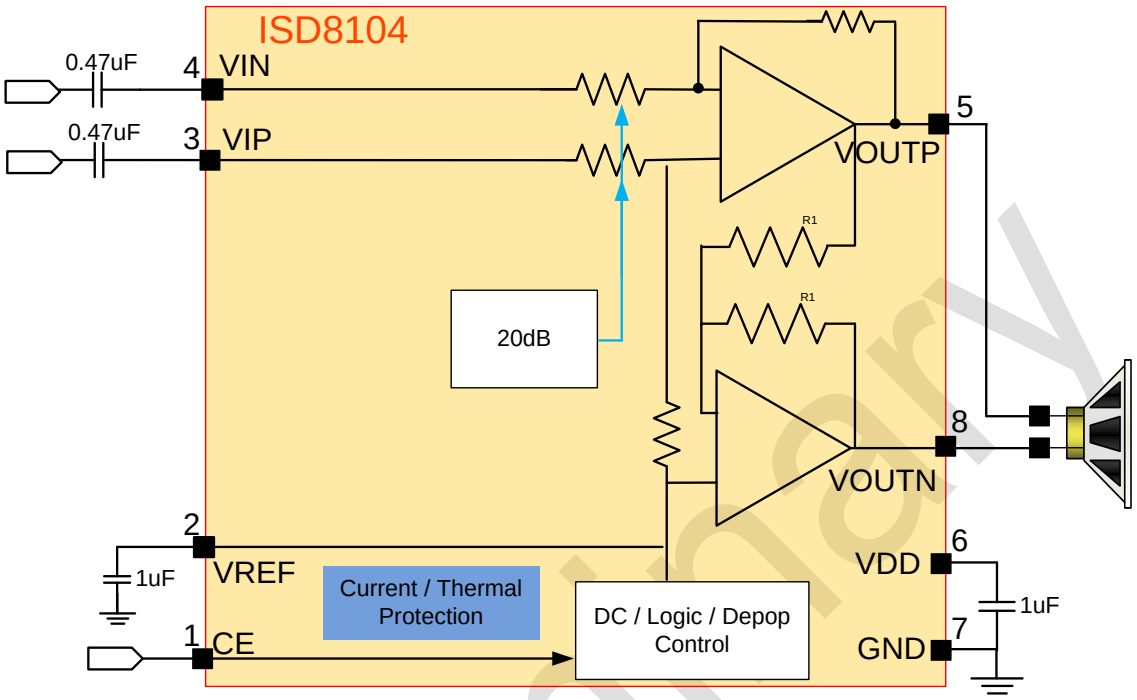

Figure 3-3 ISD8104 Differential Input Pair Block Diagram

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4 PINOUT CONFIGURATION: SOP- 8

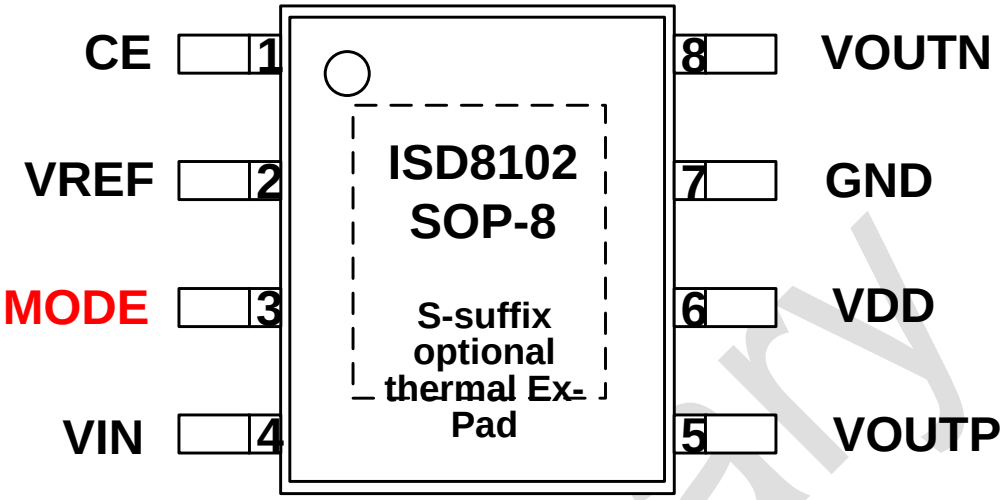

Figure 4-1 ISD8102 8-Lead SOP Pin Configuration

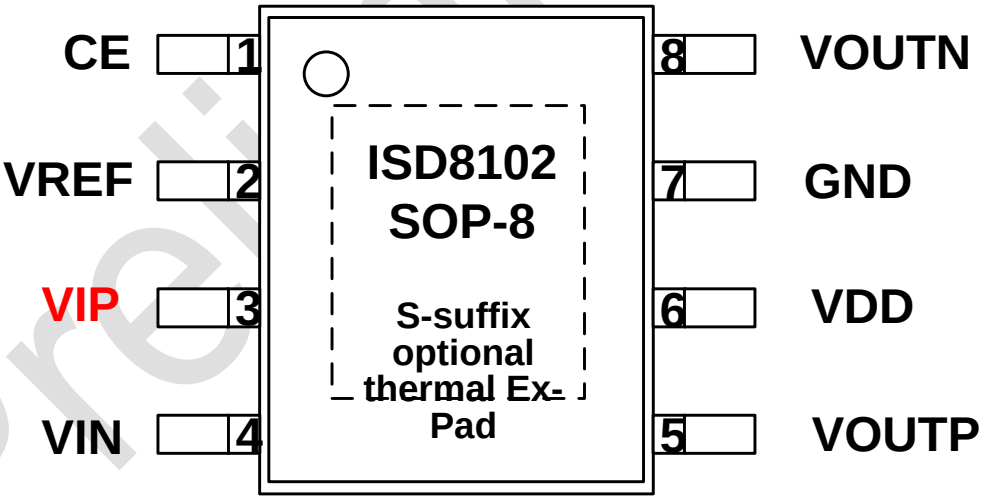

Figure 4-3 ISD8104 8-Lead SOP Pin Configuration

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5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	CE	I	Chip Enable
2	VREF	O	Internal Reference Voltage (1/2 Vdd)
3	MODE	I	Single-Ended / Differential Output Logic Control
4	VIN	I	Inverting Signal Input
5	VOUTP	O	Non-Inverting Speaker Output
6	VDD	I	Supply Voltage
7	GND	I	Ground
8	VOUTN	O	Inverting Speaker Output
9	Ex-Pad	I	Thermal Tab (must be connected to Vss, SOP-8 package, only)

Table 5-1 ISD8102 8-Lead SOP Pin Description

Pin Number	Pin Name	I/O	Function
1	CE	I	Chip Enable
2	VREF	O	Internal Reference Voltage (1/2 Vdd)
3	VIP	I	Non-Inverting Signal Input
4	VIN	I	Inverting Signal Input
5	VOUTP	O	Non-Inverting Speaker Output
6	VDD	I	Supply Voltage
7	GND	I	Ground
8	VOUTN	O	Inverting Speaker Output
9	Ex-Pad	I	Thermal Tab (must be connected to Vss, SOP-8 package, only)

Table 5-3 ISD8104 8-Lead SOP Pin Description

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6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range [1]	-40°C to +85°C
Supply voltage (V_{DD})	+2.0V to +6.8V
Ground voltage (V_{SS})	0V
Input voltage (V_{DD})	Vss to V_{DD}
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature) [1]	-40°C to +85°C
Supply voltage (V_{DD})	+2.0V to +6.8V
Ground voltage (V_{SS})	0V
Input voltage (V_{DD})	Vss to V_{DD}
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

Notes: [1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.2 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.0		6.8	V	
Operating Current	I_{DD}		3.6		mA	V_{DD}= 5V, no load
Standby Current	I_{SB}		0.1	<1	µA	V_{DD}= 5V
CE input resistance			20k		ohm	Internal pull-down @ 0dB
CE input current			120		µA	CE=2.3V, V_{DD}= 5V
CE threshold enabled	V_{ENL}		<0.9		V	All supply voltages
CE threshold standby	V_{ENH}		>1.5		V	All supply voltages
VREF Reference Voltage			V_{DD}/2		V	

Notes: [1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

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6.3 AC PARAMETERS

6.3.1 Analog Characteristics; Cref=1uF / Cvdd = 1uF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Audio Input Voltage Range			0.3 - 6.5		V	Vdd = 6.8Vdc
			0.3 – 3.4		V	Vdd = 3.7Vdc
			0.3 - 1.7		V	Vdd = 2.0Vdc
Inverting Input Impedance			TBD			Gain=20dB
Non-Inverting Input Impedance			TBD			Gain=20dB
Power Supply Rejection Ratio	PSRR		75dB			Vdd = 5Vdc
Common Mode Rejection Ratio	CMRR		70dB			Signal at INP = INV
Voltage Gain			20dB			Rinput = zero-ohms
Enable Time from power-on Vdd = CE (device always on)			n/a			determined by application circuit
Enable Time from Standby			0.5		msec	Single-ended
Enable Time from Standby			0.5		msec	Differential
Pop-and-Click from Standby [1]			<10		mV	Single Ended
Pop-and-Click from Standby [1]			<10		mV	Differential
Thermal Resistance			60		°C/W	SOP-8 (with Ex-Pad)
Thermal Resistance			150		°C/W	SOP-8

Notes: [1] Impulse voltage that is potentially audible. After impulse, there is a slow ramp from standby Vref to operating Vref, which is typically inaudible with Cref = 1uF

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6.3.2 Speaker Outputs

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
Signal-to-Noise Ratio	SNR		100		dB	0dB gain, 5Vdc
Load Impedance	$R_{L(SPK)}$		4		Ω	
Output Offset Voltage			8		mV	

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS (THD+N)
Output Power (BTL mode)	P_{BTL}		600		mW	<0.1% distortion
Load 4Ω	P_{BTL}		1600		mW	<1% distortion
Vdd=5Vdc / 0dB gain	P_{BTL}		2000		mW	<10% distortion

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	Units	Conditions (THD+N)
Output Power (BTL mode)	P_{BTL}		600		mW	<0.1% distortion
Load 8Ω	P_{BTL}		1200		mW	<1% distortion
Vdd=5Vdc / 0dB gain	P_{BTL}		1400		mW	<10% distortion

Notes: [1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

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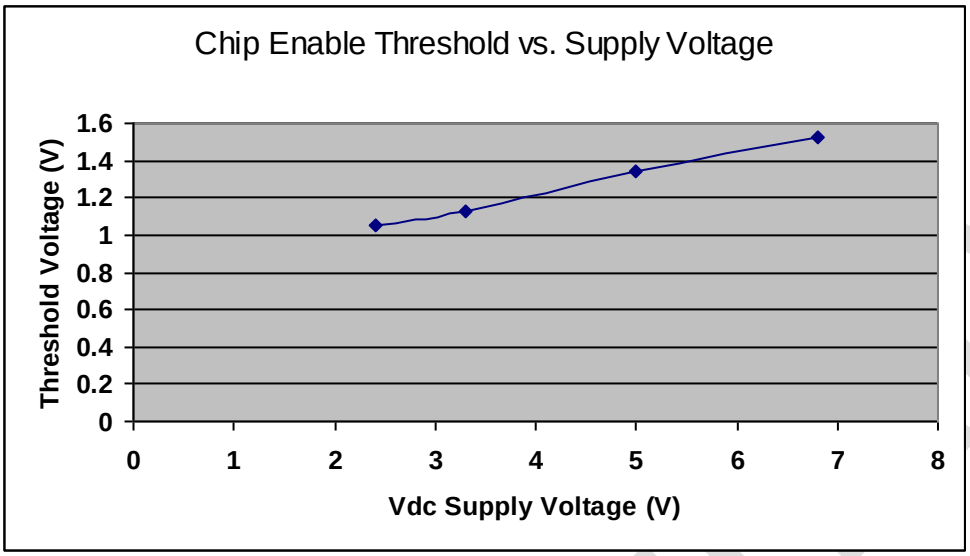
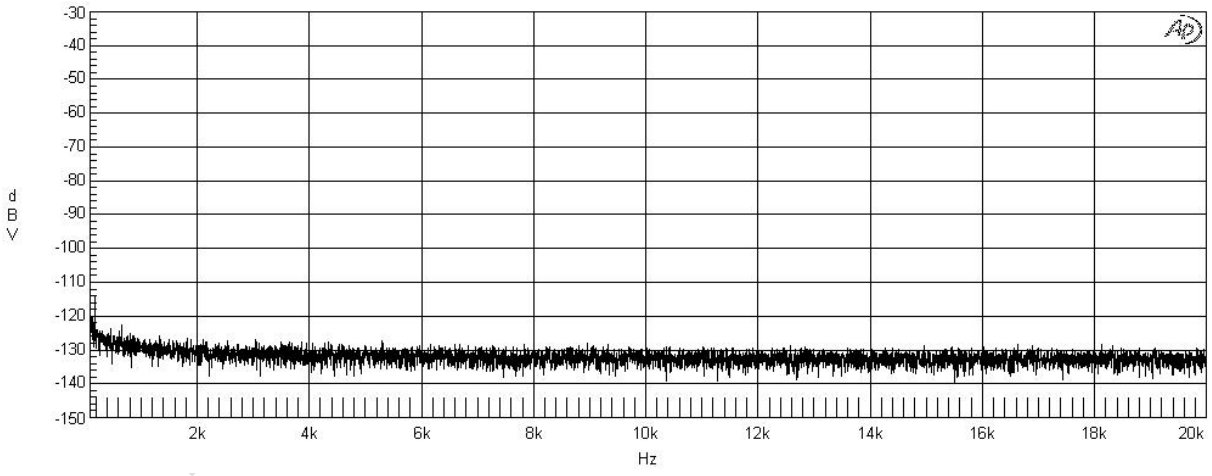
6.3.3 Chip Enable Threshold Voltage

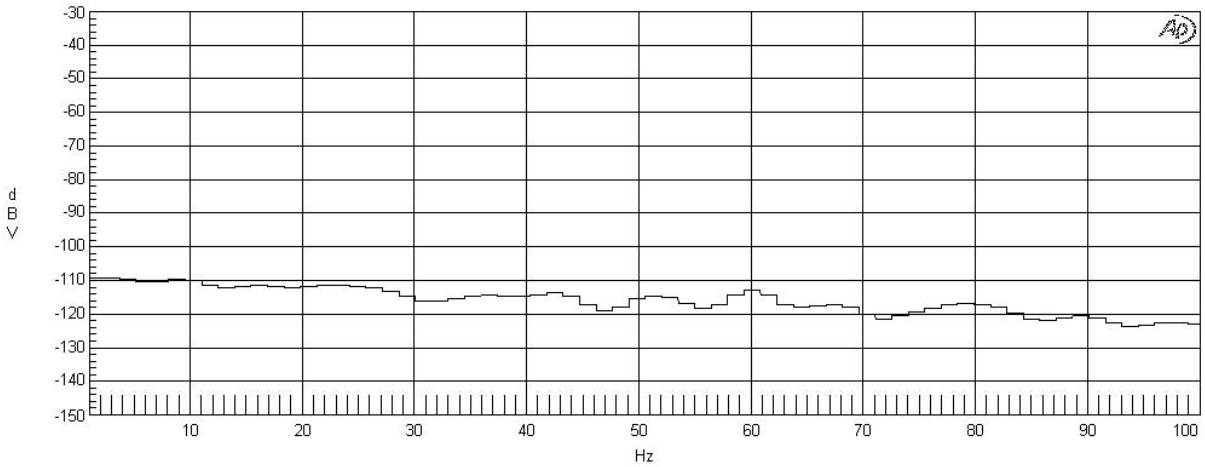


6.3.4 Output Noise Spectrum

Noise spectrum at Vdd = 5.0Vdc, Gain = 0dB, BW<22kHz



Noise Spectrum at Vdd = 5.0Vdc, Gain = 20dB, BW<22kHz



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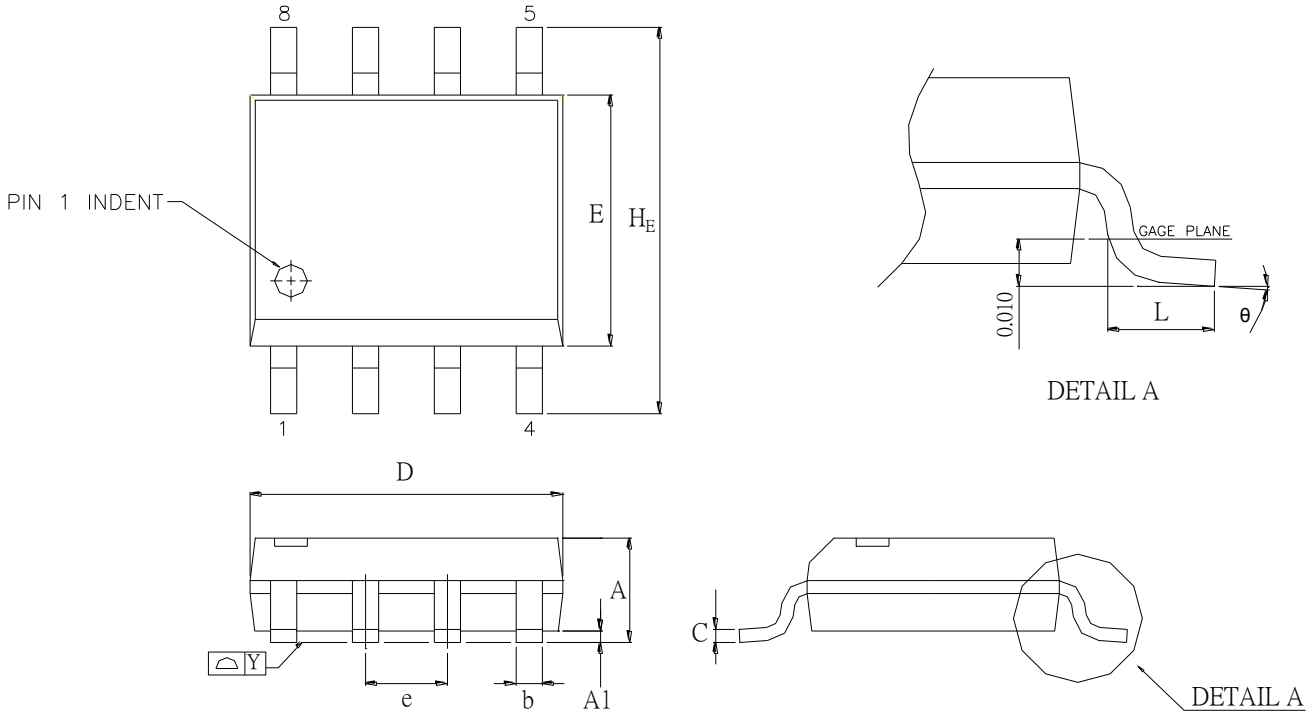
PACKAGE SPECIFICATION

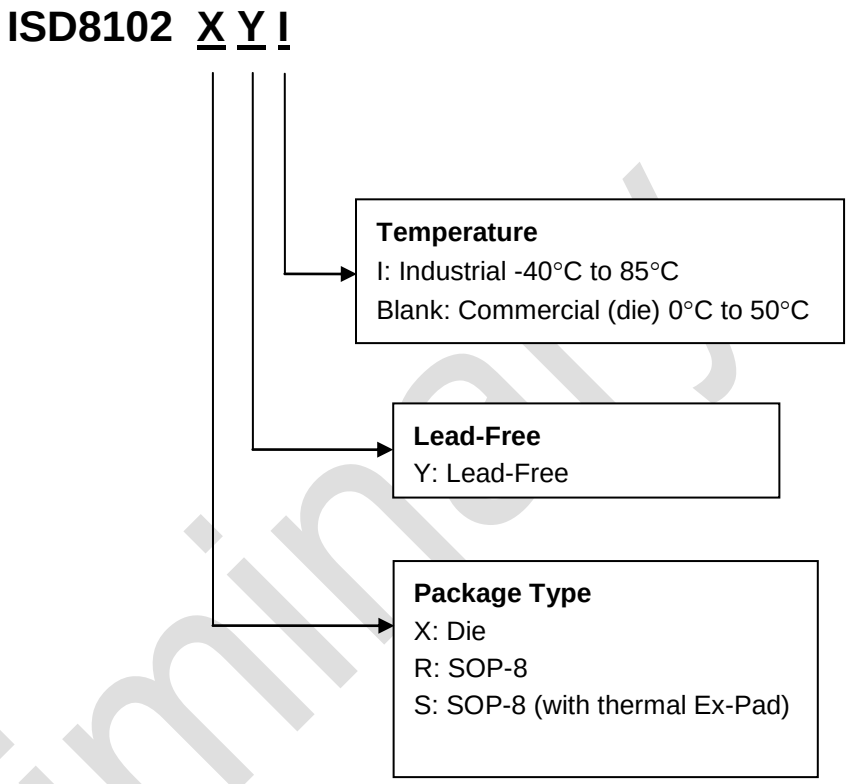
6.48 LEAD SOP- 8 (EX-PAD)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	–	1.75	0.053	–	0.069
A1	0.05	–	0.15	0.002	–	0.006
b	0.33	–	0.51	0.013	–	0.020
C	0.19	–	0.25	0.008	–	0.010
D	4.8	–	5.00	0.188	–	0.196
E	3.8	–	4.0	0.150	–	0.157
e	1.27 BASIC			0.050 BASIC		
H_E	5.8	–	6.20	0.228	–	0.244
Y	–	–	0.10	–	–	0.004
L	0.40	–	1.27	0.016	–	0.050
θ	0°	–	10°	0°	–	10°

ORDERING INFORMATION



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7 REVISION HISTORY

Version	Date	Description
0.0	Aug, 2010	Initial draft
0.1	Aug, 2010	Package Update
0.2	Oct, 2010	Internal Gain Spec Update

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