4-Bit Magnitude Comparator

The MC14585B 4–Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A < B, A = B, and A > B), and three outputs (A < B, A = B, and A > B). This device compares two 4–bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4–bits, units can be cascaded by connecting outputs (A > B), (A < B), and (A = B) to the corresponding inputs of the next significant comparator. Inputs (A < B), (A = B), and (A > B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

Features

- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421–BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded See Figure 3
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to VSS)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I _{in} , I _{out}	±10	mA
Power Dissipation per Package (Note 1)	P _D	500	mW
Ambient Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Lead Temperature (8–Second Soldering)	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Temperature Derating: Plastic "P and D/DW"
 Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS



PDIP-16 P SUFFIX CASE 648 

SOIC-16 D SUFFIX CASE 751B 

SOEIAJ-16 F SUFFIX CASE 966

A = Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G = Pb-Free Package

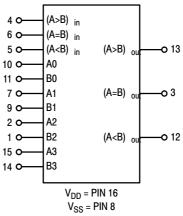
ORDERING INFORMATION

Device	Package	Shipping [†]
MC14585BCP	PDIP-16	25 Units / Rail
MC14585BCPG	PDIP-16 (Pb-Free)	25 Units / Rail
MC14585BD	SOIC-16	48 Units / Rail
MC14585BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14585BDR2	SOIC-16	2500/Tape & Reel
MC14585BDR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel
MC14585BFEL	SOEIAJ-16	2000/Tape & Reel
MC14585BFELG	SOEIAJ-16 (Pb-Free)	2000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN ASSIGNMENT 16 V_{DD} B2 [1 ● A2 [2 15 A3 (A = B)_{out} ☐ 3 14 B3 13 (A > B)_{out} $(A > B)_{in}$ 4 $(A < B)_{in} \square 5$ 12 $(A < B)_{out}$ (A = B)_{in} ☐ 6 11 B0 A1 🛮 7 10 🛮 A0 9 B1 V_{SS} [8

BLOCK DIAGRAM



TRUTH TABLE (x = Don't Care)

Inputs										
	Comp	aring		Cascading			Outputs			
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B	
A3 > B3	Х	Х	Х	х	Х	Х	0	0	1	
A3 = B3	A2 > B2	Х	х	х	х	х	0	0	1	
A3 = B3	A2 = B2	A1 > B1	х	х	х	х	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 > B0	х	х	х	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	Х	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	х	0	1	0	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	х	1	0	0	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	х	1	1	0	
A3 = B3	A2 = B2	A1 = B1	A0 < B0	Х	Х	Х	1	0	0	
A3 = B3	A2 = B2	A1 < B1	х	х	х	х	1	0	0	
A3 = B3	A2 < B2	Х	х	х	х	х	1	0	0	
A3 < B3	Х	Х	х	х	х	х	1	0	0	

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

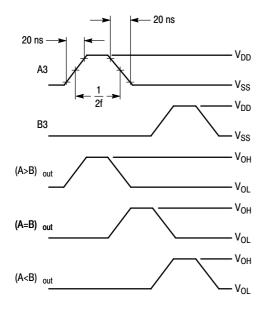
			- 5	5°C		25°C		125	5°C	
Characteristic	Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD} "1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
"1" Level $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	V _{IH}	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	_ _ _	Vdc
	I _{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	- - -	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - - -	- 1.7 - 0.36 - 0.9 - 2.4	- - - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current	I _{in}	15	_	±0.1	-	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	_	_	-	-	5.0	7.5	_	-	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15			$I_T = ($	D.6 μΑ/kHz) f 1.2 μΑ/kHz) f 1.8 μΑ/kHz) f	+ I _{DD}	•		μAdc

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH} , t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH} , t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH} , t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Turn–On, Turn–Off Delay Time t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 345 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$	t _{PLH} , t _{PHL}	5.0 10 15	- - -	430 180 130	860 360 260	ns

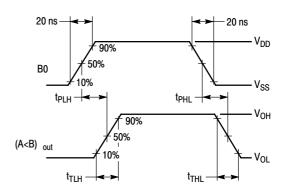
Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L – 50) Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

^{5.} The formulas given are for the typical characteristics only at 25°C.6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low. f in respect to a system clock.

Figure 1. Dynamic Power Dissipation Signal Waveforms



Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A<B) low.

Figure 2. Dynamic Signal Waveforms

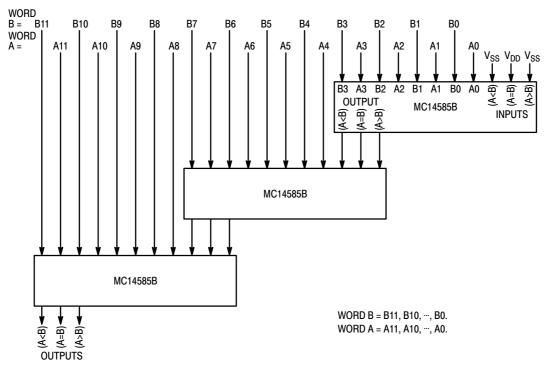
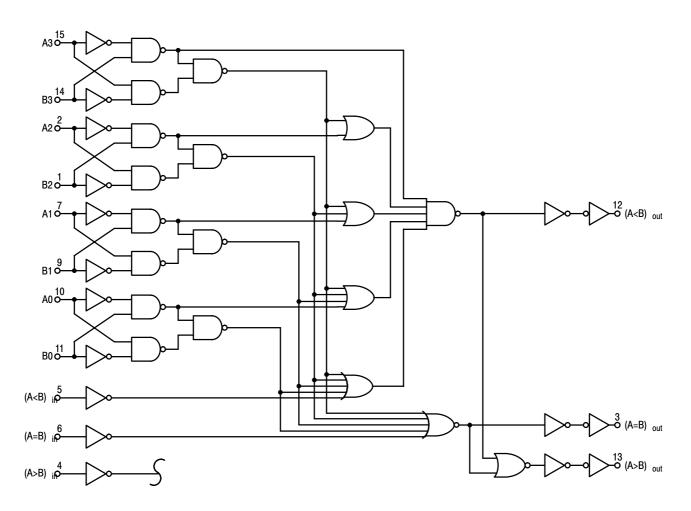


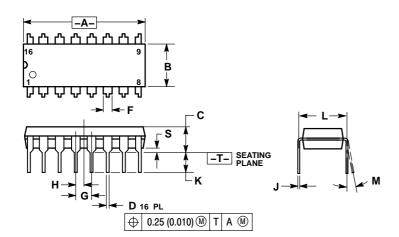
Figure 3. Cascading Comparators

LOGIC DIAGRAM



PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 **ISSUE T**

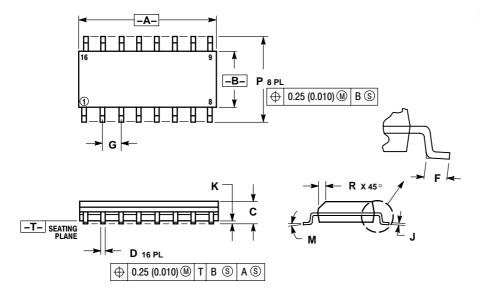


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE
- MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIM	ETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	0.050 BSC		BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
М	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

SOIC-16 CASE 751B-05 **ISSUE J**



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

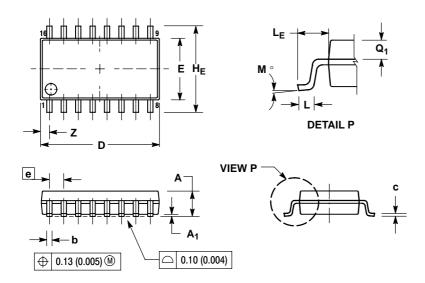
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- 4. MAXIMUM MOLLD PHOTHUSION 0.15 (0.000)
 PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL
 IN EXCESS OF THE D DIMENSION AT
 MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	1.27 BSC		BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ-16 CASE 966-01 **ISSUE A**



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT
- INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018)

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
Α ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27	1.27 BSC		BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LΕ	1.10	1.50	0.043	0.059
М	0 °	10°	0 °	10°
ď	0.70	0.90	0.028	0.035
Z		0.78		0.031

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice on semiconductor and are registered readerlands of semiconductor Components industries, Ltc (SCILLC) solicit esserves the inject to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative