ISL5829
NOT RECOMMENDED FOR NEW DESIGN NO RECOMMENDED REPLACE Center at contact our Technical Support Cent. 1 -888-INTERSIL or www.intersil.com/sc

DATASHEET

FN6020
Rev 1.00
Feb 2002

The ISL5829 is a dual 12-bit, 130/210+MSPS (Mega Samples Per Second), CMOS, high speed, low power, D/A (digital to analog) converter, designed specifically for use in high performance communication systems such as base transceiver stations utilizing 2.5 G or 3 G cellular protocols.
This device complements the ISL5x61 and ISL5x29 families of high speed converters, which include $8-, 10-$, 12-, and 14bit devices.

## Ordering Information

| PART <br> NUMBER | TEMP. <br> RANGE <br> $\left({ }^{\circ} \mathrm{C}\right)$ | PACKAGE | PKG. NO. | CLOCK <br> SPEED |
| :--- | :---: | :--- | :--- | :--- |
| ISL5829IN | -40 to 85 | 48 Ld LQFP | Q48.7x7A | 130 MHz |
| ISL5829/2IN | -40 to 85 | 48 Ld LQFP | Q48.7x7A | 210 MHz |
| ISL5829EVAL1 | 25 | Evaluation Platform |  | 210 MHz |

## Pinout



## Features

- Speed Grades

130M and 210+MSPS

- Low Power . . . . . 233mW with 20mA Output at 130MSPS
- Adjustable Full Scale Output Current. . . . . 2 mA to 20 mA
- Guaranteed Gain Matching $<0.14 \mathrm{~dB}$
- +3.3V Power Supply
- 3V LVCMOS Compatible Inputs
- Excellent Spurious Free Dynamic Range $(73 \mathrm{dBc}$ to Nyquist, $\mathrm{f} \mathrm{S}=130 \mathrm{MSPS}, \mathrm{fOUT}=10 \mathrm{MHz}$ )
- UMTS Adjacent Channel Power $=70 \mathrm{~dB}$ at 19.2 MHz
- EDGE/GSM SFDR $=90 \mathrm{dBc}$ at 11 MHz in 20 MHz Window
- Dual, 3.3V, Lower Power Replacement for AD9765


## Applications

- Cellular Infrastructure - Single or Multi-Carrier: IS-136, IS-95, GSM, EDGE, CDMA2000, WCDMA, TDS-CDMA
- BWA Infrastructure
- Quadrature Transmit with IF Range $0-80 \mathrm{MHz}$
- Medical/Test Instrumentation and Equipment
- Wireless Communication Systems


## Typical Applications Circuit



## Functional Block Diagram



## Pin Descriptions

| PIN NO. | PIN NAME | PIN DESCRIPTION |
| :---: | :---: | :---: |
| 11, 19, 26 | AGND | Analog ground. |
| 13, 24 | Avdd | Analog supply ( +2.7 V to +3.6 V ). |
| 28 | CLK | Clock input. |
| 27 | DGND | Connect to digital ground. |
| 10 | DVDD | Digital supply ( +2.7 V to +3.6 V ). |
| 20 | FSADJ | Full scale current adjust. Use a resistor to ground to adjust full scale output current. Full scale output current $=32 \times V_{\text {FSADJ }} / R_{\text {SET }}$. |
| 14, 23 | NC | Not internally connected. Recommend no connect. |
| 12, 25 | ICOMP, QCOMP | Compensation pin for internal bias generation. Each pin should be individually decoupled to AGND with a $0.1 \mu \mathrm{~F}$ capacitor. |
| $\begin{gathered} 1-6,29-40, \\ 43-48 \end{gathered}$ | ID11-ID0, QD11-QD0 | Digital data input ports. Bit 11 is most significant bit (MSB) and bit 0 is the least significant bit (LSB). |
| 15, 22 | IOUTA, QOUTA | Current outputs of the device. Full scale output current is achieved when all input bits are set to binary 1. |
| 16, 21 | IOUTB, QOUTB | Complementary current outputs of the device. Full scale output current is achieved on the complementary outputs when all input bits are set to binary 0 . |
| 17 | REFIO | Reference voltage input if Internal reference is disabled. The internal reference is not intended to drive an external load. Use $0.1 \mu \mathrm{~F}$ cap to ground when internal reference is enabled. |
| 18 | REFLO | Connect to analog ground to enable internal 1.2 V reference or connect to $\mathrm{AV} \mathrm{V}_{\mathrm{DD}}$ to disable internal reference. |
| 7, 8, 41, 42 | NC | No connect (NC). Not internally connected. No termination required, may be used for device migration to higher resolution DACs. |
| 9 | SLEEP | Connect to digital ground or leave floating for normal operation. Connect to $\mathrm{DV}_{\mathrm{DD}}$ for sleep mode. |


| e Maximum Ratings |  |
| :---: | :---: |
| Digital Supply Voltage DV ${ }_{\text {DD }}$ to DGND | +3.6V |
| Analog Supply Voltage AVDD to AGND | +3.6V |
| Grounds, AGND TO DGND | -0.3V to +0.3V |
| Digital Input Voltages (DATA, CLK, SLEEP) | $D V_{D D}+0.3 V$ |
| Reference Input Voltage Range. | $A V_{D D}+0.3 V$ |
| Analog Output Current (Iout) | 24 mA |

Digital Supply Voltage DV ${ }_{\text {DD }}$ to DGND . . . . . . . . . . . . . . . . . . +3.6 V
Analog Supply Voltage $\mathrm{AV}_{\text {DD }}$ to AGND . . . . . . . . . . . . . . . . . . +3.6 V
Grounds, AGND TO DGND . . . . . . . . . . . . . . . . . . . . -0.3V to +0.3V

Reference Input Voltage Range. . . . . . . . . . . . . . . . . AV $\mathrm{AV}_{\mathrm{DD}}+0.3 \mathrm{~V}$
Analog Output Current (IOUT) . . . . . . . . . . . . . . . . . . . . . . . . . 24mA

## Thermal Information

Thermal Resistance (Typical, Note 1) $\quad \theta_{\mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
LQFP Package. . . . . . . . . . . . . . . . . . . . . . . . . . . . . 70
Maximum Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . 150²ㅇ
Maximum Storage Temperature Range . . . . . . . . . . . $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . . 300 ${ }^{\circ} \mathrm{C}$

## Operating Conditions

Temperature Range $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
NOTE:

1. $\theta_{\mathrm{JA}}$ is measured with the component mounted on an evaluation PC board in free air.

| Electrical Specifications ${ }^{\text {a }}$ ( ${ }^{\text {P }}$ | $A V_{D D}=D V_{D D}=+3.3 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=$ Internal 1.2 V, IOUTFS $=20 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for All Typical Values |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | TEST CONDITIONS | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ TO $85^{\circ} \mathrm{C}$ |  |  | UNITS |
|  |  | MIN | TYP | MAX |  |
| SYSTEM PERFORMANCE |  |  |  |  |  |
| Resolution |  | 12 | - | - | Bits |
| Integral Linearity Error, INL | "Best Fit" Straight Line (Note 7) | -1.25 | $\pm 0.5$ | +1.25 | LSB |
| Differential Linearity Error, DNL | (Note 7) | -1 | $\pm 0.5$ | +1 | LSB |
| Offset Error, Ios | IOUTA (Note 7) | -0.006 |  | +0.006 | \% FSR |
| Offset Drift Coefficient | (Note 7) | - | 0.1 | - | $\begin{gathered} \mathrm{ppm} \\ \mathrm{FSR} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Full Scale Gain Error, FSE | With External Reference (Notes 2, 7) | -3 | $\pm 0.5$ | +3 | \% FSR |
|  | With Internal Reference (Notes 2, 7) | -3 | $\pm 0.5$ | +3 | \% FSR |
| Full Scale Gain Drift | With External Reference (Note 7) | - | $\pm 50$ | - | $\begin{gathered} \mathrm{ppm} \\ \mathrm{FSR} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
|  | With Internal Reference (Note 7) | - | $\pm 100$ | - | $\begin{gathered} \mathrm{ppm} \\ \mathrm{FSR} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Crosstalk | $\mathrm{f}_{\text {CLK }}=100 \mathrm{MSPS}, \mathrm{f}$ OUT $=10 \mathrm{MHz}$ | - | 83 | - | dB |
|  | $\mathrm{f}_{\text {CLK }}=100 \mathrm{MSPS}, \mathrm{fOUT}=40 \mathrm{MHz}$ | - | 74 | - | dB |
| Gain Matching Between Channels (DC Measurement) | As a percentage of Full Scale Range | -1.6 | 0.6 | +1.6 | \% FSR |
|  | In dB Full Scale Range | -0.14 | 0.05 | +0.14 | dB FSR |
| Full Scale Output Current, $\mathrm{I}_{\text {FS }}$ |  | 2 | 20 | 22 | mA |
| Output Voltage Compliance Range | (Note 3) | -1.0 | - | 1.25 | V |
| DYNAMIC CHARACTERISTICS |  |  |  |  |  |
| Maximum Clock Rate, f ${ }^{\text {CLK }}$ | ISL5829/2IN | 210 | 250 | - | MHz |
| Maximum Clock Rate, f ${ }_{\text {cLK }}$ | ISL5829IN | 130 | 150 | - | MHz |
| Output Rise Time | Full Scale Step | - | 1 | - | ns |
| Output Fall Time | Full Scale Step | - | 1 | - | ns |
| Output Capacitance |  | - | 5 | - | pF |
| Output Noise | IOUTFS $=20 \mathrm{~mA}$ | - | 50 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
|  | IOUTFS $=2 \mathrm{~mA}$ | - | 30 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |


| Electrical Specifications AV |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PARAMETER | TEST CONDITIONS | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ TO $85^{\circ} \mathrm{C}$ |  |  | UNITS |
|  |  | MIN | TYP | MAX |  |
| AC CHARACTERISTICS (Using Figure 13 with $\mathrm{R}_{\text {DIFF }}=50 \Omega$ and $\mathrm{R}_{\text {LOAD }}=50 \Omega$, Full Scale Output $=-2.5 \mathrm{dBm}$ ) |  |  |  |  |  |
| Spurious Free Dynamic Range, SFDR Within a Window | $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{fOUT}=80.8 \mathrm{MHz}, 30 \mathrm{MHz}$ Span ( ( otes 4, 7) | - | 72 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{fOUT}=40.4 \mathrm{MHz}, 30 \mathrm{MHz}$ Span ( Notes 4, 7) | - | 78 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{fOUT}=20.2 \mathrm{MHz}, 20 \mathrm{MHz}$ Span ( Notes 4, 7) | - | 84 | - | dBc |
| Spurious Free Dynamic Range, SFDR to Nyquist (fCLK/2) | $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=80.8 \mathrm{MHz}($ Notes 4, 7) | - | 54 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}$, fout $=40.4 \mathrm{MHz}($ Notes $4,7,9)$ | - | 65 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=200 \mathrm{MSPS}, \mathrm{fOUT}=20.2 \mathrm{MHz}, \mathrm{T}=25^{\circ} \mathrm{C}$ (Notes 4, 7) | 60 | 66 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=200 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}, \mathrm{T}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ (Notes 4, 7) | 58 | - | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=50.5 \mathrm{MHz}($ Notes 4, 7 ) | - | 57 | - | dBc |
|  | $\mathrm{fCLK}^{\text {= }}$ 130MSPS, fout $=40.4 \mathrm{MHz}($ Notes 4,7$)$ | - | 62 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}$, fout $=20.2 \mathrm{MHz}($ Notes 4, 7) | - | 69 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=10.1 \mathrm{MHz}, \mathrm{T}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ (Notes 4, 7) | 68 | 73 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{fout}=5.05 \mathrm{MHz}($ Notes 4, 7) | - | 77 | - | dBc |
|  | $\mathrm{fCLK}^{\text {= }}$ 100MSPS, fout $=40.4 \mathrm{MHz}($ Notes 4,7$)$ | - | 60 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}$, fout $=30.3 \mathrm{MHz}$ (Notes 4, 7) | - | 63 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}, \mathrm{f}$ OUT $=20.2 \mathrm{MHz}($ Notes 4, 7) | - | 70 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}$, fout $=10.1 \mathrm{MHz}($ Notes 4, 7, 9) | - | 73 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}, \mathrm{fOUT}=5.05 \mathrm{MHz}($ Notes 4, 7) | - | 76 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=50 \mathrm{MSPS}, \mathrm{f}$ OUT $=20.2 \mathrm{MHz}($ Notes 4, 7) | - | 66 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=50 \mathrm{MSPS}, \mathrm{fOUT}=10.1 \mathrm{MHz}($ Notes 4, 7) | - | 73 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=50 \mathrm{MSPS}$, fout $=5.05 \mathrm{MHz}$ (Notes 4, 7) | - | 77 | - | dBc |
| Spurious Free Dynamic Range, SFDR in a Window with Eight Tones | $\mathrm{f}_{\mathrm{CLK}}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=28.3 \mathrm{MHz}$ to $45.2 \mathrm{MHz}, 2.1 \mathrm{MHz}$ Spacing, 50 MHz Span (Notes 4, 7, 9) | - | 64 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=130 \mathrm{MSPS}$, fout $=17.5 \mathrm{MHz}$ to $27.9 \mathrm{MHz}, 1.3 \mathrm{MHz}$ Spacing, 35MHz Span (Notes 4, 7) | - | 67 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=80 \mathrm{MSPS}$, fout $=10.8 \mathrm{MHz}$ to $17.2 \mathrm{MHz}, 811 \mathrm{kHz}$ Spacing, 15MHz Span (Notes 4, 7) | - | 74 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=50 \mathrm{MSPS}$, fout $=6.7 \mathrm{MHz}$ to $10.8 \mathrm{MHz}, 490 \mathrm{kHz}$ Spacing, 10MHz Span (Notes 4, 7) | - | 75 | - | dBc |
| Spurious Free Dynamic Range, SFDR in a Window with EDGE or GSM | $\mathrm{f}_{\mathrm{CLK}}=78 \mathrm{MSPS}, \mathrm{fOUT}=11 \mathrm{MHz}$, in a 20 MHz Window, RBW $=30 \mathrm{kHz}$ (Notes 4, 7, 9) | - | 90 | - | dBc |
| Adjacent Channel Power Ratio, ACPR with UMTS | $\mathrm{f}_{\text {CLK }}=76.8 \mathrm{MSPS}, \mathrm{fout}=19.2 \mathrm{MHz}, \mathrm{RBW}=30 \mathrm{kHz}($ Notes 4, 7, 9) | - | 70 | - | dB |
| VOLTAGE REFERENCE |  |  |  |  |  |
| Internal Reference Voltage, $\mathrm{V}_{\text {FSADJ }}$ | Pin 20 Voltage with Internal Reference | 1.2 | 1.23 | 1.3 | V |
| Internal Reference Voltage Drift |  | - | $\pm 40$ | - | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Internal Reference Output Current Sink/Source Capability | Reference is not intended to drive an external load | - | 0 | - | $\mu \mathrm{A}$ |
| Reference Input Impedance |  | - | 1 | - | $\mathrm{M} \Omega$ |
| Reference Input Multiplying Bandwidth | (Note 7) | - | 1.0 | - | MHz |


| Electrical Specifications | $A V_{D D}=\mathrm{DV}_{\mathrm{DD}}=+3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}=$ Internal 1.2V, IOUTFS $=20 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for All Typical Values (Continued) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PARAMETER | TEST CONDITIONS | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ TO $85^{\circ} \mathrm{C}$ |  |  | UNITS |
|  |  | MIN | TYP | MAX |  |
| DIGITAL INPUTS D11-D0, CLK |  |  |  |  |  |
| Input Logic High Voltage with 3.3V Supply, $\mathrm{V}_{\mathrm{IH}}$ | (Note 3) | 2.3 | 3.3 | - | V |
| Input Logic Low Voltage with 3.3V Supply, VIL | (Note 3) | - | 0 | 1.0 | V |
| Sleep Input Current, $\mathrm{I}_{\mathrm{IH}}$ |  | -25 | - | +25 | $\mu \mathrm{A}$ |
| Input Logic Current, $\mathrm{IIH}_{\mathrm{IH}} \mathrm{IL}$ |  | -20 | - | +20 | $\mu \mathrm{A}$ |
| Clock Input Current, $\mathrm{I}_{\mathrm{IH}, \mathrm{IL}}$ |  | -10 | - | +10 | $\mu \mathrm{A}$ |
| Digital Input Capacitance, $\mathrm{C}_{\text {IN }}$ |  | - | 3 | - | pF |
| TIMING CHARACTERISTICS |  |  |  |  |  |
| Data Setup Time, tsu | See Figure 15 | - | 1.5 | - | ns |
| Data Hold Time, thLD | See Figure 15 | - | 1.5 | - | ns |
| Propagation Delay Time, $\mathrm{t}_{\text {PD }}$ | See Figure 15 | - | 1 | - | Clock <br> Period |
| CLK Pulse Width, tpW1, tPW2 | See Figure 15 (Note 3) | 2 | - | - | ns |
| POWER SUPPLY CHARACTERISTICS |  |  |  |  |  |
| AV DD Power Supply | (Note 8) | 2.7 | 3.3 | 3.6 | V |
| DV ${ }_{\text {DD }}$ Power Supply | (Note 8) | 2.7 | 3.3 | 3.6 | V |
| Analog Supply Current (lavdi) | 3.3 V , IOUTFS $=20 \mathrm{~mA}$ | - | 60 | 62 | mA |
|  | 3.3 V , IOUTFS $=2 \mathrm{~mA}$ | - | 24 | - | mA |
| Digital Supply Current (IDVDD) | 3.3 V (Note 5) | - | 11 | 15 | mA |
|  | 3.3 V (Note 6) | - | 17 | 21 | mA |
| Supply Current (IAVDD) Sleep Mode | 3.3V, IOUTFS = Don't Care | - | 5 | - | mA |
| Power Dissipation | 3.3 V , IOUTFS $=20 \mathrm{~mA}$ (Note 5) | - | 233 | 255 | mW |
|  | 3.3 V, IOUTFS $=20 \mathrm{~mA}$ (Note 6) | - | 253 | 274 | mW |
|  | 3.3 V , IOUTFS $=2 \mathrm{~mA}$ ( Note 5) | - | 115 | - | mW |
| Power Supply Rejection | Single Supply (Note 7) | -0.125 | - | +0.125 | \%FSR/V |

## NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through RSET (typically $625 \mu \mathrm{~A}$ ). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made with differential transformer coupled output and no external filtering. For multitone testing, the same pattern was used at different clock rates, producing different output frequencies but at the same ratio to the clock rate.
5. Measured with the clock at 130 MSPS and the output frequency at 10 MHz .
6. Measured with the clock at 200MSPS and the output frequency at 20 MHz .
7. See Definition of Specifications.
8. Recommended operation is from 3.0 V to 3.6 V . Operation below 3.0 V is possible with some degradation in spectral performance. Reduction in analog output current may be necessary to maintain spectral performance.
9. See Typical Performance plots.

Typical Performance ( +3.3 V Supply, Using Figure 13 with $\mathrm{R}_{\mathrm{DIFF}}=100 \Omega$ and $\mathrm{R}_{\text {LOAD }}=50 \Omega$ )


FIGURE 1. EDGE AT 11MHz, 78MSPS CLOCK $(91+d B c @ \Delta f=+6 M H z)$


FIGURE 3. GSM AT 11MHz, 78MSPS CLOCK
$(90+\mathrm{dBc} @ \Delta \mathrm{f}=+6 \mathrm{MHz}, 3 \mathrm{~dB}$ PAD)


FIGURE 5. FOUR EDGE CARRIERS AT $12.4-15.6 \mathrm{MHz}$, 800kHz SPACING, 78MSPS (71dBc - 20MHz WINDOW)


FIGURE 2. EDGE AT 11MHz, 78MSPS CLOCK (75dBc -NYQUIST, 6dB PAD)


FIGURE 4. GSM AT 11MHz, 78MSPS CLOCK
( 75 dBc - NYQUIST, 9dB PAD)


FIGURE 6. FOUR GSM CARRIERS AT $12.4-15.6 \mathrm{MHz}$, 78MSPS (73dBc - 20MHz WINDOW, 6dB PAD)

Typical Performance (+3.3V Supply, Using Figure 13 with $\mathrm{R}_{\mathrm{DIFF}}=100 \Omega$ and $\mathrm{R}_{\text {LOAD }}=50 \Omega$ ) (Continued)


FIGURE 7. UMTS AT 19.2MHz, 76.8MSPS (70dB 1stACPR, 70dB 2ndACPR)


FIGURE 9. ONE TONE AT 40.4MHz, 210MSPS CLOCK (61dBc - NYQUIST, 6dB PAD)


FIGURE 11. TWO TONES (CkHzF=6) AT 8.5MHz, 50MSPS CLOCK, 500 kHz SPACING ( $82 \mathrm{dBc}-10 \mathrm{MHz}$ WINDOW, 6dB PAD)


FIGURE 8. ONE TONE AT 10.1MHz, 80MSPS CLOCK (71dBc - NYQUIST, 6dB PAD)


FIGURE 10. EIGHT TONES (CREST FACTOR=8.9) AT 37 MHz , 210MSPS CLOCK, 2.1MHz SPACING (65dBc - NYQUIST)


FIGURE 12. FOUR TONES (CF=8.1) AT 14MHz, 80MSPS CLOCK, 800kHz SPACING (70dBc - NYQUIST, 6dB PAD)

## Definition of Specifications

Adjacent Channel Power Ratio, ACPR, is the ratio of the average power in the adjacent frequency channel (or offset) to the average power in the transmitted frequency channel.

Crosstalk, is the measure of the channel isolation from one DAC to the other. It is measured by generating a sinewave in one DAC while the other DAC is clocked with a static input, and comparing the output power of each DAC at the frequency generated.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be one LSB. A DNL specification of one LSB or less guarantees monotonicity.

EDGE, Enhanced Data for Global Evolution, a TDMA standard for cellular applications which uses 200 kHz BW, 8-PSK modulated carriers.

Full Scale Gain Drift, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from $\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$. It is defined as the maximum deviation from the value measured at room temperature to the value measured at either $\mathrm{T}_{\text {MIN }}$ or $\mathrm{T}_{\mathrm{MAX}}$. The units are ppm of FSR (full scale range) per ${ }^{\circ} \mathrm{C}$.
Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R ${ }_{\text {SET }}$ ).
Gain Matching, is a measure of the full scale amplitude match between the I and Q channels given the same input pattern. It is typically measured with all 1 s at the input to both channels, and the full scale output voltage developed into matching loads is compared for the I and Q outputs.

GSM, Global System for Mobile Communication, a TDMA standard for cellular applications which uses 200 kHz BW, GMSK modulated carriers.
Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Internal Reference Voltage Drift, is defined as the maximum deviation from the value measured at room temperature to the value measured at either $\mathrm{T}_{\text {MIN }}$ or $\mathrm{T}_{\text {MAX }}$. The units are ppm per ${ }^{\circ} \mathrm{C}$.

Offset Drift, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage at IOUTA through a known resistance as the temperature is varied from $\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\text {MAX }}$. It is defined as the maximum deviation from the value measured at room temperature to the value measured at either $\mathrm{T}_{\text {MIN }}$ or $\mathrm{T}_{\text {MAX }}$. The units are ppm of FSR (full scale range) per degree ${ }^{\circ} \mathrm{C}$.

Offset Error, is measured by setting the data inputs to all logic low (all 0 s ) and measuring the output voltage of IOUTA through
a known resistance. Offset error is defined as the maximum deviation of the IOUTA output current from a value of 0 mA .
Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

Power Supply Rejection, is measured using a single power supply. The nominal supply voltage is varied $\pm 10 \%$ and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3 dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the amplitude of the output waveform is $0.707(-3 \mathrm{~dB})$ of its original value.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Total Harmonic Distortion, THD, is the ratio of the RMS value of the fundamental output signal to the RMS sum of the first five harmonic components.

UMTS, Universal Mobile Telecommunications System, a W-CDMA standard for cellular applications which uses 3.84 MHz modulated carriers.

## Detailed Description

The ISL5829 is a dual 12-bit, current out, CMOS, digital to analog converter. The core of each DAC is based on the ISL5861. The maximum update rate is at least $210+$ MSPS and can be powered by a single power supply in the recommended range of +3.0 V to +3.6 V . Operation with clock rates higher than 210MSPS is possible; please contact the factory for more information. It consumes less than 125 mW of power per channel when using a +3.3 V supply, the maximum 20 mA of output current, and the data switching at 210MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain, worst-case transition points such as midscale and quarter scale transitions. By greatly reducing the amount of current switching at these major transitions, the overall glitch of the converter is dramatically reduced, improving settling time, transient problems, and accuracy.

## Digital Inputs and Termination

The ISL5829 digital inputs are formatted as offset binary and guaranteed to 3 V LVCMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the
lines driving the clock and the digital inputs are long $50 \Omega$ lines, then $50 \Omega$ termination resistors should be placed as close to the converter inputs as possible connected to the digital ground plane (if separate grounds are used). These termination resistors are not likely needed as long as the digital waveform source is within a few inches of the DAC. For pattern drivers with very high speed edge rates, it is recommended that the user consider series termination (50-200 ) prior to the DAC's inputs in order to reduce the amount of noise.

## Power Supply

Separate digital and analog power supplies are recommended. The allowable supply range is +2.7 V to +3.6 V . The recommended supply range is +3.0 to 3.6 V (nominally +3.3 V ) to maintain optimum SFDR. However, operation down to +2.7 V is possible with some degradation in SFDR. Reducing the analog output current can help the SFDR at +2.7 V . The SFDR values stated in the table of specifications were obtained with a +3.3 V supply.

## Ground Planes

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane.

## Noise Reduction

To minimize power supply noise, $0.1 \mu \mathrm{~F}$ capacitors should be placed as close as possible to the converter's power supply pins, $A V_{D D}$ and $D V_{D D}$. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for $D V_{D D}$ and to the analog ground for $A V_{D D}$. Additional filtering of the power supplies on the board is recommended.

## Voltage Reference

The internal voltage reference of the device has a nominal value of +1.23 V with a $\pm 40 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift coefficient over the full temperature range of the converter. It is recommended that a $0.1 \mu \mathrm{~F}$ capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin selects the reference. The internal reference can be selected if REFLO is tied low (ground). If an external reference is desired, then REFLO should be tied high (the analog supply voltage) and the external reference driven into REFIO. The full scale output current of the converter is a function of the voltage reference used and the value of $\mathrm{R}_{\text {SET }}$. I OUT should be within the 2 mA to 22 mA range, though operation below 2 mA is possible, with performance degradation.

If the internal reference is used, $\mathrm{V}_{\text {FSADJ }}$ will equal approximately 1.2 V . If an external reference is used, $\mathrm{V}_{\mathrm{FSADJ}}$ will equal the external reference. The calculation for IOUT (Full Scale) is:
$l_{\text {OUT }}($ Full Scale $)=\left(V_{\text {FSADJ }} / R_{\text {SET }}\right) \times 32$.

If the full scale output current is set to 20 mA by using the internal voltage reference ( 1.23 V ) and a $1.91 \mathrm{k} \Omega \mathrm{R}_{\mathrm{SET}}$ resistor, then the input coding to output current will resemble the following:

## TABLE 1. INPUT CODING vs OUTPUT CURRENT WITH INTERNAL REFERENCE (1.23V TYP) AND RSET=1.91K $\Omega$

| INPUT CODE (D11-D0) | IOUTA (mA) | IOUTB (mA) |
| :---: | :---: | :---: |
| 111111111111 | 20.6 | 0 |
| 100000000000 | 10.3 | 10.3 |
| 000000000000 | 0 | 20.6 |

## Analog Output

IOUTA and IOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -1.0 V to 1.25 V . R $\mathrm{R}_{\mathrm{OUT}}$ (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

## $\mathrm{V}_{\text {OUT }}=I_{\text {OUT }} \times$ R OUT .

The most effective method for reducing the power consumption is to reduce the analog output current, which dominates the supply current. The maximum recommended output current is 20 mA .

## Differential Output

IOUTA and IOUTB can be used in a differential-to-singleended arrangement to achieve better harmonic rejection. With $R_{\text {DIFF }}=50 \Omega$ and $R_{\text {LOAD }}=50 \Omega$, the circuit in Figure 13 will provide a $500 \mathrm{mV}(-2.5 \mathrm{dBm})$ signal at the output of the transformer if the full scale output current of the DAC is set to 20 mA (used for the electrical specifications table). Values of $R_{\text {DIFF }}=100 \Omega$ and $R_{\text {LOAD }}=50 \Omega$ were used for the typical performance curves to increase the output power and the dynamic range. The center tap in Figure 13 must be grounded.

In the circuit in Figure 14, the user is left with the option to ground or float the center tap. The DC voltage that will exist at either IOUTA or IOUTB if the center tap is floating is IOUT ${ }_{D C} \times$ $\left(R_{A} / / R_{B}\right) V$ because $R_{\text {DIFF }}$ is $D C$ shorted by the transformer. If the center tap is grounded, the DC voltage is 0 V . Recommended values for the circuit in Figure 14 are $R_{A}=R_{B}=50 \Omega$, $R_{\text {DIFF }}=100 \Omega$, assuming $R_{\text {LOAD }}=50 \Omega$. The performance of Figure 13 and Figure 14 is basically the same, however leaving the center tap of Figure 14 floating allows the circuit to find a more balanced virtual ground, theoretically improving the even order harmonic rejection, but likely
reducing the signal swing available due to the output voltage compliance range limitations.
$R_{E Q}=0.5 \times\left(R_{\text {LOAD }} / / R_{\text {DIFF }}\right)$
AT EACH OUTPUT


RLOAD REPRESENTS THE LOAD SEEN BY THE TRANSFORMER

FIGURE 13. OUTPUT LOADING FOR DATASHEET MEASUREMENTS
$R_{E Q}=0.5 \times\left(R_{\text {LOAD }} / / R_{\text {DIFF }} / / R_{A}\right)$, WHERE $R_{A}=R_{B}$


FIGURE 14. ALTERNATIVE OUTPUT LOADING

## Propagation Delay

The converter requires two clock rising edges for data to be represented at the output. Each rising edge of the clock captures the present data word and outputs the previous data. The propagation delay is therefore $1 / C L K$, plus $<2 n$ of processing. See Figure 15.

## Test Service

Intersil offers customer-specific testing of converters with a service called Testdrive. To submit a request, fill out the Testdrive form at www.intersil.com/testdrive. Or, send a request to the technical support center.

## Timing Diagram



FIGURE 15. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

## Thin Plastic Quad Flatpack Packages (LQFP)



Q48.7x7A (JEDEC MS-026BBC ISSUE B) 48 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

|  | INCHES |  | MILLIMETERS |  | SYMBOL |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | - | 0.062 | - | 1.60 | - |
| A1 | 0.002 | 0.005 | 0.05 | 0.15 | - |
| A2 | 0.054 | 0.057 | 1.35 | 1.45 | - |
| b | 0.007 | 0.010 | 0.17 | 0.27 | 6 |
| b1 | 0.007 | 0.009 | 0.17 | 0.23 | - |
| D | 0.350 | 0.358 | 8.90 | 9.10 | 3 |
| D1 | 0.272 | 0.280 | 6.90 | 7.10 | 4,5 |
| E | 0.350 | 0.358 | 8.90 | 9.10 | 3 |
| E1 | 0.272 | 0.280 | 6.90 | 7.10 | 4,5 |
| L | 0.018 | 0.029 | 0.45 | 0.75 | - |
| N | 48 |  | 48 |  | 7 |
| e | 0.020 BSC |  |  | $0.50 ~ B S C$ | - |

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions $D$ and $E$ to be determined at seating plane $-\mathrm{C}-$.
4. Dimensions D1 and E1 to be determined at datum plane $-\mathrm{H}-$.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm ( 0.010 inch ) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm ( 0.003 inch).
7. " N " is the number of terminal positions.

## © Copyright Intersil Americas LLC 2002. All Rights Reserved. <br> All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html
Intersil products are manufactured, assembled and tested utilizing IS09001 quality systems as noted
in the quality certifications found at www.intersil.com/en/support/qualandreliability.html
Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

