Single-chip Type with Built-in FET Switching Regulators

Flexible Step-down Switching Regulator with Built-in Power MOSFET

BD9876EFJ

● Description
Output 3.0A and below High Efficiency Rate Step-down Switching Regulator Power MOSFET Internal Type BD9876EFJ mainly used as secondary side Power supply, for example from fixed Power supply of 12V, 24V etc, Step-down Output of 1.2V/1.8V/3.3V/5V, etc, can be produced. This IC has external Coil/Capacitor down-sizing through 300kHz Frequency operation, inside Nch-FET SW for 45V “withstand-pressure” commutation and also, high speed load response through Current Mode Control is a simple external setting phase compensation system, through a wide range external constant, a compact Power supply can be produced easily.

● Features
1) Internal 200 mΩ Nch MOSFET
2) Output Current 3A
3) Oscillation Frequency 300kHz
4) Synchronizes to External Clock (200kHz ~ 500kHz)
5) Feedback Voltage 1.0V±1.0%
6) Internal Soft Start Function
7) Internal Over Current Protect Circuit, Low Input Error Prevention Circuit, Heat Protect Circuit
8) ON/OFF Control through EN Pin (Standby Current 0 A Typ.)
9) Package: HTSOP-J8 Package

● Applications
For Household machines in general that have 12V/24V Lines, etc.

● Absolute Maximum Rating

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC-GND Supply Voltage</td>
<td>VCC</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>BST-GND Voltage</td>
<td>VBST</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>BST-Lx Voltage</td>
<td>VBST</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>EN-GND Voltage</td>
<td>VEN</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>Lx-GND Voltage</td>
<td>VLX</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>FB-GND Voltage</td>
<td>VFB</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>VC-GND Voltage</td>
<td>VC</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>SYNC-GND Voltage</td>
<td>SYNC</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>High-side FET Drain Current</td>
<td>IDH</td>
<td>3.5</td>
<td>A</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Pd</td>
<td>3.76(1)</td>
<td>W</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>Topr</td>
<td>-40 ~ +105</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-55 ~ +150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>Tjmax</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) During mounting of 70×70×1.6mm 4layer board (Copper area: 70mm×70mm). Reduce by 30.08mW for every 1°C increase. (Above 25°C)

● Operating Conditions (Ta=25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>VCC</td>
<td>7</td>
<td>-</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>VOUT</td>
<td>1.0(2)</td>
<td>-</td>
<td>VCC×0.7</td>
<td>V</td>
</tr>
</tbody>
</table>

(2) Restricted by minimum on pulse typ. 200ns
**Electrical Characteristics** *(Unless otherwise specified, Ta=25°C, VCC=24V, Vo=5V, EN=3V)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limits</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td><strong>[Circuit Current]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stand-by current of VCC</td>
<td>Ist</td>
<td>-</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>VEN=0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit current of VCC</td>
<td>Icc</td>
<td>-</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>FB=1.2V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>[Under Voltage Lock Out (UVLO)]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Detect Voltage</td>
<td>Vuv</td>
<td>6.1</td>
<td>6.4</td>
<td>6.7</td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>Vuvhy</td>
<td>-</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td><strong>[Oscillator]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillating frequency</td>
<td>fosc</td>
<td>270</td>
<td>300</td>
<td>330</td>
</tr>
<tr>
<td>Max Duty Cycle</td>
<td>Dmax</td>
<td>85</td>
<td>91</td>
<td>97</td>
</tr>
<tr>
<td><strong>[Error Amp]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB threshold voltage</td>
<td>VFB</td>
<td>0.990</td>
<td>1.000</td>
<td>1.010</td>
</tr>
<tr>
<td>Input bias current</td>
<td>IFB</td>
<td>-1.0</td>
<td>0</td>
<td>1.0</td>
</tr>
<tr>
<td>Error amplifier DC gain</td>
<td>A\textsubscript{VEA}</td>
<td>700</td>
<td>7000</td>
<td>70000</td>
</tr>
<tr>
<td>Trans Conductance</td>
<td>G\textsubscript{EA}</td>
<td>110</td>
<td>220</td>
<td>440</td>
</tr>
<tr>
<td>Soft Start Time</td>
<td>Tsoft</td>
<td>7</td>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td><strong>[Current Sense Amp]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VC to switch current transconductance</td>
<td>G\textsubscript{CS}</td>
<td>5</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td><strong>[Output]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lx NMOS ON resistance</td>
<td>RonH</td>
<td>-</td>
<td>200</td>
<td>340</td>
</tr>
<tr>
<td>Lx pre-charge NMOS ON resistance</td>
<td>RonL</td>
<td>-</td>
<td>10</td>
<td>17</td>
</tr>
<tr>
<td>Over Current Detect Current</td>
<td>Iocp</td>
<td>3.5</td>
<td>6</td>
<td>-</td>
</tr>
<tr>
<td><strong>[CTL]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Pin Control voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>VENON</td>
<td>2</td>
<td>-</td>
<td>VCC</td>
</tr>
<tr>
<td>OFF</td>
<td>VENOFF</td>
<td>-0.3</td>
<td>-</td>
<td>0.8</td>
</tr>
<tr>
<td>EN Pin input current</td>
<td>REN</td>
<td>2.7</td>
<td>5.5</td>
<td>11</td>
</tr>
<tr>
<td><strong>[SYNC]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC Pin Control voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>VSYNCH</td>
<td>2.0</td>
<td>-</td>
<td>5.5</td>
</tr>
<tr>
<td>Low</td>
<td>VSYNCL</td>
<td>-0.3</td>
<td>-</td>
<td>0.8</td>
</tr>
<tr>
<td>SYNC Pin input current</td>
<td>REN</td>
<td>6</td>
<td>12</td>
<td>24</td>
</tr>
<tr>
<td>SYNC falling edge to LX rising edge delay</td>
<td>tdelay</td>
<td>200</td>
<td>400</td>
<td>600</td>
</tr>
</tbody>
</table>

* Not designed to withstand radiation.
### Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Lx</td>
<td>Terminal for inductor</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground pin</td>
</tr>
<tr>
<td>3</td>
<td>VC</td>
<td>Error amplifier output</td>
</tr>
<tr>
<td>4</td>
<td>FB</td>
<td>Inverting node of the trans conductance error amplifier</td>
</tr>
<tr>
<td>5</td>
<td>SYNC</td>
<td>Input pin of an external signal for the device synchronized by external signal</td>
</tr>
<tr>
<td>6</td>
<td>EN</td>
<td>Stand-by ON/OFF pin</td>
</tr>
<tr>
<td>7</td>
<td>BST</td>
<td>Voltage Supply pin for High Side FET Driver</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>Voltage input pin</td>
</tr>
</tbody>
</table>

![Fig.1 Pin Layout Diagram](image1.png)

### Block Diagram

![Fig.2 Block Diagram](image2.png)
● Block Description

1. Reference
   This Block generates Error Amp Standard Voltage. Standard Voltage is 1.0V.

2. REG
   This is a Gate Drive Voltage Generator and 5V Low Saturation regulator for internal Circuit Power supply.

3. OSC
   This is a precise wave Oscillation Circuit with Operation Frequency fixed to 300 kHz fixed (self-running mode).
   To implement the synchronization feature connect a square wave (Hi Level: higher than 2V Low Level: lower than 0.8V ) to the SYNC pin. The synchronization frequency range is 200 kHz to 500 kHz.
   After connecting the rising edge of LX will be synchronized to the falling edge of SYNC pin signal after 3 count.
   At the synchronization remove the external clock, the device transitions self-running mode after 7 microseconds.

4. Soft Start
   A Circuit that does Soft Start to the Output Voltage of DC/DC Comparator, and prevents Rush Current during Start-up.
   Soft Start Time is set at IC internal, after 10ms from starting-up EN Pin, Standard Voltage comes to 1.0V, and Output Voltage becomes set Voltage.

5. ERROR AMP
   This is an Error amplifier what detects Output Signal, and outputs PWM Control Signal.
   Internal Standard Voltage is set to 1.0V. Also, C and R are connected between the Output (VC) Pin GND of Error Amp as Phase compensation elements. (See P.11)

6. ICOMP
   This is a Voltage-Pulse Width Converter that controls Output Voltage in response to Input Voltage.
   This compares the Voltage added to the internal SLOPE waveform in response to the FET WS Current with Error amplifier Output Voltage, controls the width of Output Pulse and outputs to Driver.

7. Nch FET SW
   This is an internal commutation SW that converts Coil Current of DC/DC Comparator.
   It contains 45V“ with stand pressure” 200mΩ SW.
   Because the Current Rating of this FET is 3.5A included ripple current, please use at within 3.5A.
   The device has the circuit of over current protection for protecting the FET from over current.
   To detect OCP 2 times sequentially, the device will stop and after 13 msec restart.

8. UVLO
   This is a Low Voltage Error Prevention Circuit.
   This prevents internal circuit error during increase of Power supply Voltage and during decline of Power supply Voltage.
   It monitors VCC Pin Voltage and internal REG Voltage. And when VCC Voltage becomes 6.4V and below, it turns OFF all Output FET and turns OFF DC/DC Comparator Output, and Soft Start Circuit resets.
   Now this Threshold has Hysteresis of 200mV.

9. TSD
   This is a Heat Protect (Temperature Protect) Circuit.
   When it detects an abnormal temperature exceeding Maximum Junction Temperature (Tj=150°C), it turns OFF all Output FET, and turns OFF DC/DC Comparator Output. When Temperature falls, it has/with Hysteresis and automatically returns.

10. EN
    With the Voltage applied to EN Pin(6pin), IC ON/OFF can be controlled.
    When a Voltage of 2.0V or more is applied, it turns ON, at Open or 0V application, it turns OFF.
    About 550kΩ Pull-down Resistance is contained within the Pin.
● Detailed Description
  ◇ Synchronizes to External Clock
  The SYNC pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to SYNC pin. The square wave amplitude must transition lower than 0.8V and higher than 2.0V on the SYNC pin and have an on time greater than 100ns and an off time greater than 100ns. The synchronization frequency range is 200 kHz to 500 kHz. The rising edge of the LX will be synchronized to the falling edge of SYNC pin signal after SYNC input pulse 3 count. At the synchronization, the external clock is removed, the device transitions self-running mode after 7 microseconds.

Fig.3 Timing chart at Synchronization

◇ The case of not using the function of synchronization
  Although the SYNC pin is pulled down by resistor in this device, if the function of the synchronization is not used, it is recommended to connect SYNC pin to ground.

Fig.4 the method to disposal the SYNC pin without synchronization

◇ SOFT START
  The soft start time of BD9876EFJ is determined by the DCDC operating frequency (self-run mode 300 kHz ⇒ 10ms). If synchronization is used at the time of EN=ON, The soft start time is restricted by SYNC pin input pulse frequency. SYNC pin input pulse frequency is fosc_ex kHz, the soft start time is expressed by below equation.

$$T_{ss} = \frac{300}{f_{osc\_ex}} \times 10 \text{ [ms]}$$

www.rohm.com
© 2012 ROHM Co., Ltd. All rights reserved.
OCP operation
The device has the circuit of over current protection for protecting the FET from over current. To detect OCP 2 times sequentially, the device will stop and after 13 msec restart.

Fig.5 Timing chart at OCP operation

OCP operation at soft start
BD9876EFJ have the function to change the OCP reference voltage according to slope for soft start to prevent IC from abnormal current at higher input voltage. This function restricts the OCP threshold a half of the specification value (typ.3A).

Fig.6 the relation SS node voltage and OCP reference voltage.
Reference Data (Unless otherwise specified, Ta=25°C, VCC=24V, Vo=5V, EN=3V)

Fig.7. Standby Current Temperature Characteristics
Fig.8. Circuit Current Power supply Voltage Characteristics
Fig.9. Circuit Current Temperature Characteristics
Fig.10. UVLO Threshold Temperature Characteristics
Fig.11. Oscillation Frequency Temperature Characteristics
Fig.12. Max Duty Temperature Characteristics
Fig.13. FB Threshold Voltage Temperature Characteristics
Fig.14. FB Threshold Power supply Characteristics
Fig.15. FB Voltage - IVC Current Characteristics
Fig. 16. Soft Start Time Temperature Characteristics

Fig. 17. Nch FET ON Resistance Temperature Characteristics

Fig. 18. Pre-charge FET ON Resistance Temperature Characteristics

Fig. 19. OCP Detect Current Temperature Characteristics

Fig. 20. VC to SW current transconductance Temperature characteristics

Fig. 21. EN Threshold Temperature Characteristics
● Example of Reference Application Circuit (Input 24V, Output 5.0V/2.5A)

![Reference Application Circuit Diagram]

Fig.22 Reference Application Circuit

● Reference Application Data (Example of Reference Application Circuit)

![Graphs showing electric power conversion rate and frequency response characteristics]

Fig.23 Electric Power Conversion Rate  
Fig.24 Frequency Response Characteristics (Io=0.5A)  
Fig.25 Frequency Response Characteristics (Io=3.0A)

![Graphs showing load response characteristics]

Fig.26 Load Response Characteristics (Io=0A→3.0A)  
Fig.27 Load Response Characteristics (Io=3.0A→0A)

![Waveform graphs]

Fig.28 Startup Waveform  
Fig.29 Stop Waveform
● Evaluation Board Pattern (Reference)

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Fig.28 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad.

The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC. The LX pin should be routed to the cathode of the catch diode and to the output inductor. Since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

![Fig.30 Evaluation Board Pattern](image_url)
**Power Dissipation**

It is shown below reducing characteristics of power dissipation to mount 70mm×70mm×1.6mm² PCB. Junction temperature must be designed not to exceed 150°C.

**Power Dissipation Estimate**

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.

The device power dissipation includes:

1) Conduction loss: \( P_{\text{con}} = I_{\text{OUT}}^2 \times R_{\text{ONH}} \times V_{\text{OUT}} / V_{\text{CC}} \)
2) Switching loss: \( P_{\text{sw}} = 1.25 \times 10^{-9} \times V_{\text{CC}}^2 \times I_{\text{OUT}} \times f_{\text{sw}} \)
3) Gate charge loss: \( P_{\text{gch}} = 22.8 \times 10^{-9} \times f_{\text{sw}} \)
4) Quiescent current loss: \( P_{\text{q}} = 1.0 \times 10^{-3} \times V_{\text{CC}} \)

Where:

- \( I_{\text{OUT}} \) is the output current (A).
- \( R_{\text{ONH}} \) is the on-resistance of the high-side MOSFET (Ω).
- \( V_{\text{OUT}} \) is the output voltage (V).
- \( V_{\text{CC}} \) is the input voltage (V).
- \( f_{\text{sw}} \) is the switching frequency (Hz).

Therefore

\[
P_d = P_{\text{con}} + P_{\text{sw}} + P_{\text{gch}} + P_{\text{q}}
\]

For given \( T_j \), \( T_j = T_a + \theta_{ja} \times P_d \)

Where:

- \( P_d \) is the total device power dissipation (W).
- \( T_a \) is the ambient temperature (°C).
- \( T_j \) is the junction temperature (°C).
- \( \theta_{ja} \) is the thermal resistance of the package (°C).

---

Fig.31  Power Dissipation (70mm×70mm×1.6mm² 1layer PCB)
**Application Components Selection Method**

1. **Inductor**
   - Something of the shield Type that Fulfills the Current Rating (Current value $I_{peak}$ below), with low DCR (Direct Current Resistance element) is recommended.
   - Value of Inductor influences Inductor Ripple Current and becomes the cause of Output Ripple.
   - In the same way as the formula below, this Ripple Current can be made small as big as the $L$ value of Coil or as high as the Switching Frequency.

   \[ I_{peak} = I_{OUT} + \frac{\Delta I}{2} \cdots (1) \]

   \[ \Delta I = \frac{V_{CC} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{CC}} \times \frac{1}{f} \cdots (2) \]

   ( $IL$: Output Ripple Current, $f$: Switching Frequency)

   For design value of Inductor Ripple Current, please carry out design tentatively with about 20% ~ 50% of Maximum Input Current.

   ※ When current that exceeds Coil rating flows to the coil, the Coil causes a Magnetic Saturation, and there are cases wherein a decline in efficiency, oscillation of output happens. Please have sufficient margin and select so that Peak Current does not exceed Rating Current of Coil.

2. **Output Capacitor**
   - In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended.
   - Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage. Output ripple voltage is looked for using the following formula. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 600kHz frequency of this design, internal circuit limitations of the BD9675FJ limit the practical maximum crossover frequency to about 30kHz. In general, the crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

   \[ C_{OUT\_\text{min}} = \frac{1}{2\pi \times Rl \times f_{c\_\text{max}}} \cdots (3) \]

   Where: Rl is the output load resistance and $f_{c\_\text{max}}$ is the maximum crossover frequency. The output ripple voltage can be estimated by:

   \[ V_{pp} = \Delta I \times \frac{1}{2\pi \times f \times C_{OUT}} + \Delta I \times R_{ESR} \cdots (4) \]

   Please design in a way that it is held within Capacity Ripple Voltage.

3. **Output Voltage Setting**
   - ERROR AMP internal Standard Voltage is 1.0V. Output Voltage is determined as seen in (4) formula.

   \[ VOUT = \frac{R1 + R2}{R2} \cdots (5) \]

4. **Bootstrap Capacitor**
   - Please connect from 4700pF to 22000pF (Laminate Ceramic Capacitor) between BST Pin and Lx Pin.
(5) Catch Diode
The BD9876EFJ is designed to operate using an external catch diode between Lx and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the Lx pin, which is $V_{CC\ MAX} + 0.5\ V$. Peak current must be greater than $I_{OUT\ MAX}$ plus one half the peak-to-peak inductor current.

(6) Input Capacitor
The BD9876EFJ requires an input capacitor and depending on the application. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but low-ESR electrolytic capacitors may also suffice. The typical recommended value for the decoupling capacitor is $10\ uF$. Please place this capacitor as possible as close to the VCC pin. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{CC} = \frac{I_{OUT}}{f \times C_{VCC}} \times \frac{V_{OUT}}{V_{CC}} \times \left[1 - \frac{V_{OUT}}{V_{CC}}\right] \cdots (6)$$

Since the input capacitor ($C_{VCC}$) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C_{VCC}} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{CC}} \times \left(1 - \frac{V_{OUT}}{V_{CC}}\right)} \cdots (7)$$

The worst case condition occurs at $V_{CC} = 2V_{OUT}$, where

$$I_{C_{VCC\ max}} = \frac{I_{OUT}}{2} \cdots (8)$$

(7) About Adjustment of DC/DC Comparator Frequency Characteristics
Role of Phase compensation element $C_1$, $C_2$, $R_3$ (See P.7. Example of Reference Application Circuit)

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp. The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$\text{Adc} = R_l \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}} \cdots (9)$$

Here, $V_{FB}$ is Feedback Voltage ($1.0\ V$). $A_{EA}$ is Voltage Gain of Error amplifier (typ: 77dB), $G_{CS}$ is the Trans-conductance of Current Detect (typ: 10A/V), and $R_l$ is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with/through the output resistance of Phase compensation Capacitor ($C_1$) and Error amplifier.
The other one occurs with/through the Output Capacitor and Load Resistor.

These poles appear in the frequency written below.

$$f_{p1} = \frac{G_{EA}}{2\pi \times C_1 \times A_{EA}} \cdots (10)$$

$$f_{p2} = \frac{1}{2\pi \times C_{OUT} \times R_l} \cdots (11)$$

Here, $G_{EA}$ is the trans-conductance of Error amplifier (typ: 220 $\mu$A/V).

Here, in this Control Loop, one zero becomes important. With the zero which occurs because of Phase compensation Capacitor $C_1$ and Phase compensation Resistor $R_3$, the Frequency below appears.

$$f_{z1} = \frac{1}{2\pi \times C_1 \times R_3} \cdots (12)$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).

This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$f_{zESR} = \frac{1}{2\pi \times C_{OUT} \times RESR} \cdots (13)$$

(ESR zero)
In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain. This pole exists in the frequency shown below.

\[ fp_3 = \frac{1}{2\pi \times C2 \times R3} \quad \cdots (14) \]

(Pole that corrects ESR zero)

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes "0" is important. When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens. On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur. Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency.

Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency. Calculation of RC is done using the formula below.

\[ R3 = \frac{2\pi \times COUT \times fc \times VOUT}{G_{EA} \times GCS \times VFB} \quad \cdots (15) \]

Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (fs).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin. In an application that has a representative Inductance value (about several µH ~ 20µH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

\[ C1 > \frac{4}{2\pi \times R3 \times fc} \quad \cdots (16) \]

RC is Phase compensation Resistor.

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done. If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

\[ \frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2} \quad \cdots (17) \]

In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

\[ C2 = \frac{COUT \times RESR}{R3} \quad \cdots (18) \]
## I/O Equivalent Schematic

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Pin Name</th>
<th>Pin Equivalent Schematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Lx</td>
<td><img src="image1" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td><img src="image2" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>7</td>
<td>BST</td>
<td><img src="image3" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td><img src="image4" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>3</td>
<td>VC</td>
<td><img src="image5" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>4</td>
<td>FB</td>
<td><img src="image6" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>5</td>
<td>SYNC</td>
<td><img src="image7" alt="Pin Equivalent Schematic" /></td>
</tr>
<tr>
<td>6</td>
<td>EN</td>
<td><img src="image8" alt="Pin Equivalent Schematic" /></td>
</tr>
</tbody>
</table>
Notes for use

1. About Absolute Maximum Rating
   When the absolute maximum ratings of application voltage, operating temperature range, etc. was exceeded, there is possibility of deterioration and destruction. Also, the short Mode or open mode, etc. destruction condition cannot be assumed. When the special mode where absolute maximum rating is exceeded is assumed, please give consideration to the physical safety countermeasure for the fuse, etc.

2. About GND Electric Potential
   In every state, please make the electric potential of GND Pin into the minimum electrical potential. Also, include the actual excessive effect, and please do it such that the pins, excluding the GND Pin do not become the voltage below GND.

3. About Heat Design
   Consider the Power Dissipation (Pd) in actual state of use, and please make Heat Design with sufficient margin.

4. About short circuit between pins and erroneous mounting
   When installing to set board, please be mindful of the direction of the IC, phase difference, etc. If it is not installed correctly, there is a chance that the IC will be destroyed. Also, if a foreign object enters the middle of output, the middle of output and power supply GND, etc., even for the case where it is shorted, there is a change of destruction.

5. About the operation inside a strong electro-magnetic field
   When using inside a strong electro-magnetic field, there is a possibility of error, so please be careful.

6. Temperature Protect Circuit (TSD Circuit)
   Temperature Protect Circuit (TSD Circuit) is built-in in this IC. As for the Temperature Protect Circuit (TSD Circuit), because it a circuit that aims to block the IC from insistent careless runs, it is not aimed for protection and guarantee of IC. Therefore, please do not assume the continuing use after operation of this circuit and the Temperature Protect Circuit operation.

7. About checking with Set boards
   When doing examination with the set board, during connection of capacitor to the pin that has low impedance, there is a possibility of stress in the IC, so for every 1 process, please make sure to do electric discharge. As a countermeasure for static electricity, in the process of assembly, do grounding, and when transporting or storing please be careful. Also, when doing connection to the jig in the examination process, please make sure to turn off the power supply, then connect. After that, turn off the power supply then take it off.

8. About common impedance
   For the power supply and the wire of GND, lower the common impedance, then, as much as possible, make the ripple smaller (as much as possible make the wire thick and short, and lower the ripple from L·C), etc., then and please consider it sufficiently.

9. In the application, when the mode where the VCC and each pin electrical potential becomes reversed exists, there is a possibility that the internal circuit will become damaged. For example, during cases wherein the condition when charge was given in the external capacitor, and the VCC was shorted to GND, it is recommended to insert the bypass diode to the diode of the back current prevention in the VCC series or the middle of each Pin-VCC.

10. About High-side Nch FET
    Please use within 3.5A contained ripple current, because the absolute maximum rating of high-side Nch FET is 3.5A.

11. About over current detection
    The detecting current is the current flowing through high-side Nch FET. Output current containing ripple current, therefore the detecting current is the current of the output current containing ripple current.
(12) About IC Pin Input
This IC is a Monolithic IC, and between each element, it has P⁺ isolation for element separation and P board. With the N layer of each element and this, the P-N junction is formed, and the parasitic element of each type is composed.

For example, like the diagram below, when resistor and transistor is connected to Pin,
- When GND > (PinA) in Resistor, when GND > (PinA), when GND > (PinB) in Transistor (PNP),
  the P-N junction will operate as a parasitic diode.
- Also, during GND > (Pin B) in the Transistor (PNP), through the N layer of the other elements connected to the above-mentioned parasitic diode, the parasitic NPN Transistor will operate.

On the composition of IC, depending on the electrical potential, the parasitic element will become necessary. Through the operation of the parasitic element interference of circuit operation will arouse, and error, therefore destruction can be caused. Therefore please be careful about the applying of voltage lower than the GND (P board) in I/O Pin, and the way of using when parasitic element operating.

Fig.34 Example of simple structure of Bipolar IC
• Ordering part number

BD9876EFJ

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>B D</td>
<td>9 8 7 6</td>
<td>EFJ : HTSOP-J8</td>
</tr>
<tr>
<td>E F J</td>
<td>- E 2</td>
<td>E2: Embossed tape and reel</td>
</tr>
</tbody>
</table>

HTSOP-J8

<Tape and Reel information>

<table>
<thead>
<tr>
<th>Tape</th>
<th>Embossed carrier tape</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>2500pcs</td>
</tr>
</tbody>
</table>

Direction of feed

E2: The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.

1pin

Order quantity needs to be multiple of the minimum quantity.
Notice

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM’s products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.