Single-chip Type with Built-in FET Switching Regulator Series
Output 1.0A High-efficiency Step-down Switching regulators with Built-in Power MOSFET
BU90002GWZ, BU90003GWZ, BU90004GWZ, BU90005GWZ, BU90006GWZ,

●Description
The BU9000XGWZ are a high efficiency 6MHz synchronous step-down switching regulator with ultra low current PFM mode.
It provides up to 1.0A load current and an input voltage range from 3.0V to 5.5V, optimized for battery powered portable applications.
BU9000XGWZ has a mode control pin that allows the user to select Forced PWM(Pulse Width Modulation) mode or PFM(Pulse Frequency Modulation) and PWM auto change mode utilized power save operation at light load current.

●Features
1)  93% peak efficiency
2)  4 to 6 MHz switching frequency
3)  Input voltage VIN=2.3V to 5.5V(BU90003～BU90006), VIN=4.0V to 5.5V (BU90002)
4)  45uA typical quiescent current
5)  Fast transient response
6)  Automatic PFM/PWM operation
7)  Forced PWM operation
8)  Internal Soft Start
9)  Under voltage lockout
10) Over current protection
11) Thermal shutdown
12) Ultra small and low profile WLCSP (1.3mm × 0.9mm t=0.40mm MAX) (UCSP35L1 )

●Applications
Cell phones, Smart phones, Portable applications and Micro DC/DC modules, USB accessories

●Operating range

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Output voltage</th>
<th>Input voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>BU90002GWZ</td>
<td>3.30V</td>
<td>4.0V to 5.5V</td>
</tr>
<tr>
<td>BU90003GWZ</td>
<td>1.20V</td>
<td>2.3V to 5.5V</td>
</tr>
<tr>
<td>BU90004GWZ</td>
<td>1.80V</td>
<td>2.3V to 5.5V</td>
</tr>
<tr>
<td>BU90005GWZ</td>
<td>2.50V</td>
<td>2.3V to 5.5V</td>
</tr>
<tr>
<td>BU90006GWZ</td>
<td>3.00V</td>
<td>2.3V to 5.5V</td>
</tr>
</tbody>
</table>
### Absolute maximum ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum input power supply voltage</td>
<td>VIN</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Maximum voltage at EN, FB, LX, MODE</td>
<td>VEN, VFB, VLX, VMODE</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>Pd</td>
<td>0.39(*1)</td>
<td>W</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>Topr</td>
<td>-40 ~ +85</td>
<td>℃</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>Tstg</td>
<td>-55 ~ +125</td>
<td>℃</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>Tjmax</td>
<td>+125</td>
<td>℃</td>
</tr>
</tbody>
</table>

(*1) When mounted on the specified PCB (55mm x 63mm), Deducted by 3.9m W/c when used over Ta=25℃

### Operating conditions Ta=25℃, VIN=3.6V(BU90003GWZ~BU90006GWZ), VIN=5.0V(BU90002GWZ)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage accuracy</td>
<td>VOUTA</td>
<td>-2</td>
<td>-</td>
<td>+2 %</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-2</td>
<td>-</td>
<td>+3 %</td>
</tr>
<tr>
<td></td>
<td>IoutMax1</td>
<td>-</td>
<td>-</td>
<td>1.0 A</td>
</tr>
<tr>
<td></td>
<td>IoutMax2</td>
<td>-</td>
<td>-</td>
<td>0.8 A</td>
</tr>
<tr>
<td></td>
<td>IoutMax3</td>
<td>-</td>
<td>-</td>
<td>0.6 A</td>
</tr>
</tbody>
</table>

| Soft start | Tss | 65 | 120 | 240 | usec |
| Frequency control | fosc | 5.4 | 6.0 | 6.6 | MHz |
|                  |     | 4.8 | 5.4 | 6.0 | MHz |
|                  |     | 3.6 | 4.0 | 4.4 | MHz |

| Driver | PchFET on resistance | RonP1 | -  | 250 | 400 | mOhm | VIN=5.0V |
|        |                      | RonP2 | 300 | 450 | mOhm | VIN=3.6V |
|        | NchFET on resistance | RonN1 | -  | 220 | 350 | mOhm | VIN=5.0V |
|        |                      | RonN2 | 250 | 380 | mOhm | VIN=3.6V |

| Control | EN pin control voltage | Operation | VENH | 1.4 | - | VIN | V |
|         | Non Operation          | VENL       | 0    | - | 0.4 | V |
|         | MODE pin control voltage | Operation | VMODEH | 1.4 | - | VIN | V | Forced PWM |
|         | Non Operation          | VMODEL     | 0    | - | 0.4 | V | Automatic PFM/PWM |

| UVLO | Protect threshold voltage | Uvth | 1.95 | 2.05 | 2.15 | V |
|      | Hysteresis               | Uvhy  | 50   | 100  | 150  | mV |

| Current limit | Current limit threshold | ILIMIT | 1.5 | 1.7 | 1.9 | A |
|               | PMOS current detect, Open loop |

| Output discharge | Output discharge resistance | DRES | 55 | 110 | 220 | Ohm | EN=0V |

| Circuit current | Operating quiescent current | IINS | - | 45 | 65 | uA |
|                 | EN=H, MODE:L, VOUT=3.6V forced Not switching |

| Shutdown current | SHD | - | 0 | 1 | uA |
|                 | EN=0V |

On no design for durability against radiation
● Electrical characteristic curves (Reference data)

L: LQM21MPN1R0NG0 (2.0mm × 1.6mm × 1.0mm Murata)
COUT: GRM155R60J475M (1.0mm × 0.5mm × 0.5mm Murata)

BU90002GWZ (3.3V OUTPUT)

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Electrical characteristic curves (Reference data) – Continued

BU90002GWZ (3.3V OUTPUT)

Fig.7 PFM mode Operation
I<sub>out</sub>=100mA

Fig.8 Mode Change Response
MODE High to Low

Fig.9 Mode Change Response
MODE Low to High

Fig.10 Efficiency vs Load current
VIN=5V PWM/PFM Auto Mode

Fig.11 Load regulation
VIN=5V PWM/PFM Auto mode

Fig.12 Vout Ripple Voltage
VIN=5V PWM/PFM Auto Mode
Electrical characteristic curves (Reference data)
BU90003GWZ(1.2V OUTPUT)

**Fig. 13 Start up**

- **EN**: 2V/div
- **VOUT**: 500mV/div
- **IL**: 200mA/div

**Fig. 14 Shut down**

- **EN**: 2V/div
- **VOUT**: 1V/div

**Fig. 15 Load transient response 5mA to 200mA**

- **Vout**: 50mV/div
- **1.2V offset**: 200mA/div

**Fig. 16 Load transient response 50mA to 350mA**

- **Vout**: 50mV/div
- **1.2V offset**: 200mA/div

**Fig. 17 Load transient response 400mA to 1000mA**

- **Vout**: 20mV/div
- **ac coupled**: 500mA/div

**Fig. 18 PFM mode Operation iout=50mA**

- **Vout**: 20mV/div
- **ac coupled**: 500mA/div
Electrical characteristic curves (Reference data) – Continued

BU90003GWZ (1.2V OUTPUT)
● Electrical characteristic curves (Reference data)
BU90004GWZ (1.80V OUTPUT)

Fig. 24 Start up

Fig. 25 Shut down

Fig. 26 Load transient response 5mA to 200mA
\( \text{tr}=\text{tf}=100\text{ns}, \text{Mode :Low} \)

Fig. 27 Load transient response 50mA to 350mA
\( \text{tr}=\text{tf}=100\text{ns}, \text{Mode :Low} \)

Fig. 28 Load transient response 200mA to 600mA
\( \text{tr}=\text{tf}=100\text{ns}, \text{Mode :Low} \)

Fig. 29 PFM mode Operation \( I_{\text{out}}=50\text{mA} \)

EN 5V/div
VOUT 1V/div
IL 200mA/div

EN 5V/div
VOUT 1V/div
IOUT 200mA/div

Vout 50mV/div
ac coupled
IOUT 200mA/div

Vout 50mV/div
ac coupled
Vout 50mV/div
ac coupled
LX 2V/div
Electrical characteristic curves (Reference data) – Continued

BU90004GWZ (1.80V OUTPUT)

Fig. 30 PWM mode Operation Iout=100mA

Fig. 31 Mode Change Response
MODE High to Low

Fig. 32 Mode Change Response
MODE Low to High

Fig. 33 Efficiency vs Load current
VIN=3.6V PWM/PFM Auto Mode

Fig. 34 Load regulation
PWM/PFM Auto mode
Block diagram / Application circuit

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External dimensions

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Pin layout (BOTTOM VIEW)

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Pin number/Name/Functions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>VIN</td>
<td>Power supply input pin</td>
</tr>
<tr>
<td>A2</td>
<td>EN</td>
<td>Enable pin</td>
</tr>
<tr>
<td>A3</td>
<td>GND</td>
<td>GND pin</td>
</tr>
<tr>
<td>B1</td>
<td>MODE</td>
<td>Forced PWM mode pin</td>
</tr>
<tr>
<td>B2</td>
<td>LX</td>
<td>Inductor connection pin</td>
</tr>
<tr>
<td>B3</td>
<td>FB</td>
<td>Feedback voltage input pin</td>
</tr>
</tbody>
</table>
**Functional descriptions**
The BU9000XGWZ are a synchronous step-down DC/DC converter that achieves fast transient response from light load to heavy load by hysteretic PWM control system and current constant PFM control system.

**OPWM control**
BU9000XGWZ operates by hysteretic PWM control. This scheme ensures fast switching, high efficiency, and fast transient response.

When the output voltage is below the VREF voltage, the error comparator output is low to high and turning on P-channel MOSFET until above the VREF voltage and minimum on time.

**OPFM control**
At light load the regulator and MODE=low, the regulator operates with reduced switching frequency and improves the efficiency. During PFM operation, the output voltage slightly higher than typical output voltage.

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**Fig. Operation of PFM mode and PWM mode**
● Description of operations

1) Shutdown
If the EN input pin set to low (<0.4V), all circuit are shut down and the regulator is standby mode.  
Do not leave the EN pin floating.

2) Soft start function
The regulator has a soft start circuit that reduces in-rush current at start-up. Typical start up times with a 4.7uF output capacitor is 120usec.

3) Current limit
The BU9000XGWZ has a current limit circuit that protects itself and external components during overload condition.

4) UVLO
The BU9000XGWZ has a Under Voltage Lock Out circuit that turn off device when VIN>2.05V(typ.)

5) FORCED PWM MODE
Setting MODE pin high (>1.4V) places the regulator in forced PWM.

6) TSD
The BU9000XGWZ has a thermal shutdown feature to protect the device if the junction temperature exceeds 150°C. In thermal shutdown, the DRIVER is disabled.
● PC Board layout

The suggested PCB layout for the BU9000XGWZ are shown in Figure. The following guidelines should be used to ensure a proper layout.

1) The input capacitor CIN should be connect as closely possible to VIN pin and GND pin.

2) From the output voltage to the FB pin line should be as separate as possible.

3) COUT and L should be connected as closely as possible. The connection of L to the LX pin should be as short as possible.

![PCB layout diagram]

Fig. PCB layout

● External parts selection

1) Inductor selection

The inductance significantly depends on output ripple current. As shown by following equation, the ripple current decreases as the inductor and/or switching frequency increase.

\[ \Delta I_L = \frac{(VIN-VOUT) \times VOUT}{L \times VIN \times f} \]

f: switching frequency  L: inductance  \( \Delta I_L \): inductor current ripple

As a minimum requirement, the DC current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple as shown by the following equation.

\[ I_{L\text{PEAK}} = I_{OUT\text{MAX}} + \frac{\Delta I_L}{2} \]

Recommended inductor selection

- LQM21MPN1R0NG0 (2.0mm × 1.6mm × 1.0mm Murata)  \( I_{out} \leq 1A \)
- LQM21PN1R0NGC (2.0mm × 1.2mm × 1.0mm Murata)  \( I_{out} \leq 0.6A \)

2) Recommended input capacitor (CIN) selection

- GRM155R60J225M (1.0mm × 0.5mm × 0.5mm Murata)
- GRM188R60J475ME84 (1.6mm × 0.8mm × 0.8mm Murata)

3) Recommended output capacitor (COUT) selection

- GRM155R60G106ME44 (1.0mm × 0.5mm × 0.5mm Murata)
- GRM188R60J475ME84 (1.6mm × 0.8mm × 0.8mm Murata)
Caution of use

1) Absolute maximum ratings
   An excess in the absolute maximum rating, such as supply voltage, temperature range of operating conditions, etc.,
   can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open
   circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection
   devices, such as fuses.

2) GND voltage
   The potential of GND pin must be minimum potential in all condition. As an exception, the circuit design allows voltages
   up to -0.3 V to be applied to the IC pin.

3) Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating
   conditions.

4) Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any
   connection error or if pins are shorted together.

5) Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to
   malfunction.

6) Mutual impedance
   Power supply and ground wiring should reflect consideration of the need to lower mutual impedance and minimize
   ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating
   inductance and capacitance).

7) Thermal shutdown Circuit (TSD Circuit)
   This model IC has a built-in TSD circuit. This circuit is only to cut off the IC from thermal runaway, and has not been
   design to protect or guarantee the IC. Therefore, the user should not plan to activate this circuit with continued
   operation in mind.

8) Regarding input pin of the IC
   This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them
   isolated.

   P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic
   diode or transistor. For example, as shown in the figures below, the relation between each potential is as follows:
   
   When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
   
   When GND > Pin B, the P-N junction operates as a parasitic transistor.

   Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual
   interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes
   operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be
   used.
Ordering part number
TBD