STLC2500C

Bluetooth™ EDR Single Chip

Features

- The lowest power consumption by design and technology (see Table 1)
- World best EDR throughput (see Table 1)
- World most performing BT-WLAN coexistence support for several BT/WLAN coexistence algorithms (i.e. 2/3/4-wire PTA, in a very flexible and parametrical way to optimize voice and data quality over Bluetooth and WLAN)
- Superior voice quality
  - Pitch-Period Error Concealment (PPEC) for improved speech quality (in the vicinity of interference)
- Extended range
  - Tx output power up to 8 dBm
- Pre-calibrated RF
  - Auto calibration (VCO, filters), no RF calibration required in production
- Bluetooth™V2.0 + EDR compliant
  - Full EDR support and all BT1.2 errata
  - All EDR data rates and packet types
- Backward compatibility with legacy devices through extended V1.2 feature support
  - Adaptive Frequency Hopping (AFH)
  - Faster connections through interlaced scan
  - Extended SCO (eSCO) links
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection-Less (ACL) logical transport link
- Synchronous Connection Oriented (SCO) link for 2 simultaneous SCO channels at 64Kbps
- Clock support for all cellular standards: system clock input and low power clock
- ARM7TDMI CPU with 32-bit core and AMBA (AHB-APB) bus configuration
- Patch RAM capability

Description

The STLC2500C is a single chip ROM-based Bluetooth solution implemented in 0.13 μm ultra low power, ultra low leakage CMOS technology for mobile terminal applications requiring integration up to HCI level. Patch RAM is available, enabling multiple patches/upgrades. The STLC2500C offers multiple interface options. The radio has been designed specifically for single chip requirements for minimal consumption and BOM count.
Applications

- Mobile terminal platforms

Order codes

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Packing</th>
</tr>
</thead>
<tbody>
<tr>
<td>E-STLC2500C</td>
<td>WFBGA48</td>
<td>Tray</td>
</tr>
<tr>
<td>E-STLC2500CTR</td>
<td>WFBGA48</td>
<td>Tape-on-reel</td>
</tr>
</tbody>
</table>

Figure 1. Block diagram

Table 1. Technical specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td></td>
</tr>
<tr>
<td>Audio communication</td>
<td>HV3: 10.9mA, 3-EV3: 6.2mA</td>
</tr>
<tr>
<td>Data communication at maximum throughput</td>
<td>DH1: 22mA, 3-DH5: 35.4mA</td>
</tr>
<tr>
<td>Complete power down</td>
<td>1 µA</td>
</tr>
<tr>
<td>Data rate throughput at host interface in EDR mode</td>
<td>2.178 Mbps</td>
</tr>
</tbody>
</table>
## Revision history

Table 2. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>29-Jan-2006</td>
<td>1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>