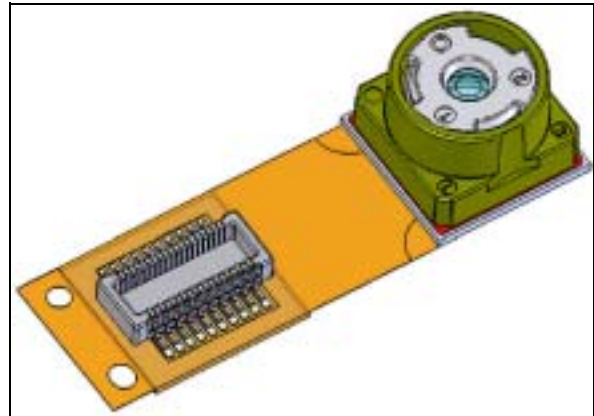


VGA Mobile Camera Module

DATA BRIEF

FEATURES

- 640H x 480V active pixels
- 3.6 μm pixel size, 1/6 inch optical format
- RGB Bayer color filter array
- Integrated 10-bit ADC
- Integrated digital image processing functions, including defect correction, lens shading correction, demosaicing, sharpening, gamma correction and color space conversion
- Embedded camera controller for automatic exposure control, automatic white balance control, black level compensation, 50/60 Hz flicker detection and cancelling, flashgun support
- Up to 30 fps progressive scan, subsampling and cropping to QVGA, QQVGA and subQCIF
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, RGB 565, RGB 444 or Bayer 10-bit output formats
- 8-bit parallel video interface, horizontal and vertical syncs, 24 MHz clock
- Two-wire serial control interface
- On-chip PLL, 6.5 to 27 MHz clock input
- Analog power supply, from 2.4 to 3.0 V
- Separate I/O power supply, 1.8 or 2.8 V levels
- Integrated power management with power switch, automatic power-on reset and power-safe pins
- Low power consumption, ultra low standby current
- Dual-element plastic lens, F# 2.8, 50° Horizontal field of view
- 7 x 7 x 4.5 mm fixed focus camera module with embedded passives
- 20-wire FPC attachment with board-to-board connector, 22 mm total length

**DESCRIPTION**

The VS6524 is a VGA resolution CMOS color digital camera featuring low size and low power consumption and targeting mobile applications. The VS6524 is manufactured in 0.18 μm ST CMOS imaging process. It integrates a high-sensitivity pixel array, a digital image processor and camera control functions.

The VS6524 is capable of streaming VGA video up to 30 fps, with ITU-R BT.656-4 YUV 4:2:2 frame format. It supports both 1.8 V and 2.8 V interface and requires a 2.4 to 3.0 V analog power supply. Typically, the VS6524 can operate as a 2.8 V single supply camera or as a 1.8 V / 2.5 V supply camera. The integrated PLL allows for low frequency system clock, and flexibility for successful EMC integration. This complete camera module is ready to connect to camera enabled baseband processors, back-end IC devices or PDA engines.

The VS6524 package uses the second generation of SmOP2 packaging technology where the sensor, passives and lens are assembled in a fully automated test and focus process, allowing high volume and low cost production.

APPLICATIONS

- Mobile phone
- PDA
- Videophone

Figure 1. Application Diagram

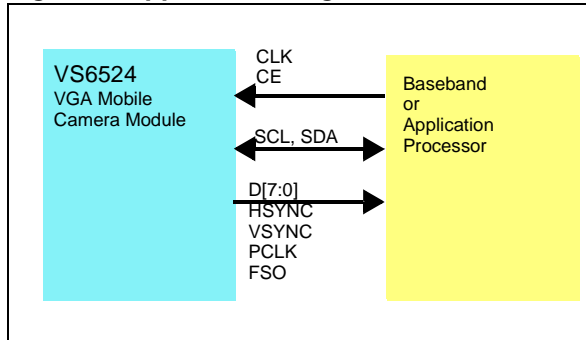


Figure 2. Block diagram

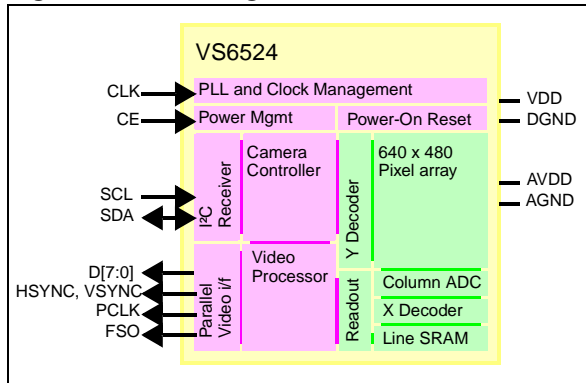


Table 1. Technical Specifications

Video Interface	8-bit parallel video, hsync, vsync ITU-R BT.656-4 compliant, 24 MHz max
Clock input	6.5 to 27 MHz square 13 MHz typ. (on-chip PLL)
Supply voltage	2.4 to 3.0 V analog
I/O voltage	1.8 or 2.8 V +/- 0.1 V CMOS levels
Power consumption	Streaming 30 fps: 30 mA max Power down: 10 µA max.
Lens	2-element, 50° HFOV, F# 2.8
Depth of field	20 cm to infinite
TV distortion	< 1%
Relative illumination	45% typ.
Package type	SmOP2
Package size	7.0 x 7.0 x 4.5 mm (wlh)
System attach	FPC with 20-pin B2B connector, Molex 55560- 0201 or equivalent ^a

a. Contact us for custom FPC designs and/or ZIF connector variants

Table 1. Technical Specifications

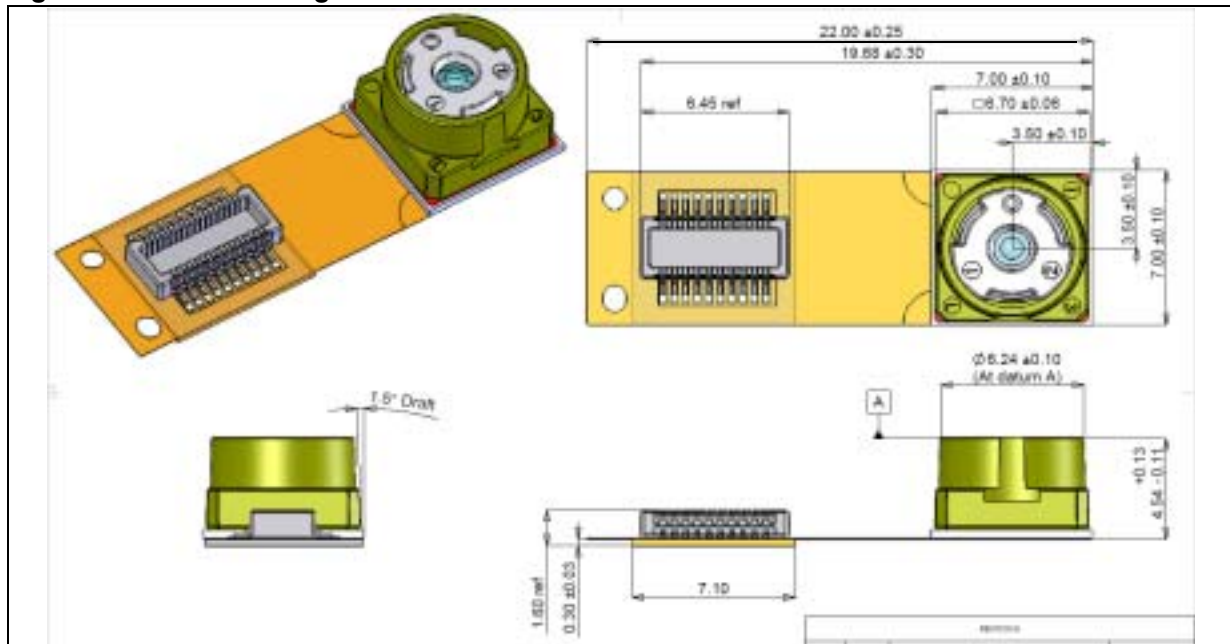
Active pixels	640H x 480V
Pixel size	3.6 x 3.6µm
Array size	2.38 x 1.77 mm
Color filter array	RGB Bayer
Exposure control	+120 dB
Analog gain	+24 dB (max)
Dynamic range	61 dB (typical)
Signal-to-noise Ratio	35 dB at 100 lux (typical)
Frame rate	1 to 30 Hz
Image format	VGA, QVGA, QQVGA, subQCIF Arbitrary cropping Horizontal/vertical flipping
Pixel format	YUV 4:2:2 RGB 565, RGB 444 Raw Bayer 10-bit

PART NUMBERING

Table 2. Order Codes

Part Number	Description
VS6524P02S	SmOP2 7.0 x 7.0 x 4.5 mm FPC attach, tray packing

Figure 3. Outline Drawing



REVISION HISTORY

Table 3. Revision History

Date	Revision	Description of Changes
February 2005	1	First Issue
February 2005	2	Same content, format/layout reviewed.

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