Silicon Labs’s Si4322 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 868 and 915 MHz bands. Used in conjunction with Silicon Labs’ FSK transmitters, the Si4322 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering is needed for operation.

The Si4322 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements. The receiver employs the Zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The Si4322 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.
DETAILED DESCRIPTION

General
The Si4322 FSK receiver is the counterpart of the Silicon Labs’ FSK transmitter. It covers the unlicensed frequency bands at 868 and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL’s high resolution allows for the use of multiple channels in any of the bands.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The Si4322 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

LNA
The LNA has 250 Ohm input impedance, which works well with the recommended antennas. (See Application Notes available from www.silabs.com/integration.)

If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, –6, –12, –18 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters
The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.

An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 15 kHz.

Data Filtering and Clock Recovery
The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

**Analog operation:** The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

**Digital operation:** The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

Data Validity Blocks
**RSSI**
A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

![Voltage on ARRSI pin vs. Input RF power](image)

<table>
<thead>
<tr>
<th>Power Level (dBm)</th>
<th>Voltage (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1 -65</td>
<td>1300</td>
</tr>
<tr>
<td>P2 -65</td>
<td>1000</td>
</tr>
<tr>
<td>P3 -100</td>
<td>600</td>
</tr>
<tr>
<td>P4 -100</td>
<td>300</td>
</tr>
</tbody>
</table>
DQD
The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bitrate, there should be four transitions during a single bit period in the I/Q signals. As the bitrate decreases in comparison to the deviation, more and more transitions will happen during a bitperiod.

AFC
By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:
- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator and Microcontroller Clock Output
The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. In normal operation it is divided from the reference 10 MHz. During sleep mode a low frequency (typical 32 kHz) output clock signal can be switched on. When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a programmable number (default is 128) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector
The low battery detector circuit monitors periodically (typ. 8 ms) the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer
The wake-up timer has very low current consumption (4 μA max) and can be programmed from 1 ms to several hours. It calibrates itself to the crystal oscillator at every startup and then at every 30 seconds with an accuracy of ±0.5%. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing. The periodic autocalibration feature can be turned off.

Event Handling
In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by setting the ex or en bits (in the Configuration Setting or Receiver Setting Command).

Si4322 generates an interrupt signal on several events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up). This signal can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller
An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 48 bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the fe bit to 1 in the Output and FIFO Mode Command. During FIFO read the crystal oscillator must be ON.
# PIN DEFINITIONS

Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SDI</td>
<td>SDI</td>
<td>DI</td>
<td>Data input of serial control interface</td>
</tr>
<tr>
<td>2</td>
<td>SCK</td>
<td>SCK</td>
<td>DI</td>
<td>Clock input of serial control interface</td>
</tr>
<tr>
<td>3</td>
<td>nSEL</td>
<td>nSEL</td>
<td>DI</td>
<td>Chip select input of serial control interface (active low)</td>
</tr>
<tr>
<td>4</td>
<td>SDO / FFIT</td>
<td>SDO</td>
<td>DO</td>
<td>Serial data out for Status Read Command.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FFIT</td>
<td>DO</td>
<td>Tristate with bushold cell if nSEL= H</td>
</tr>
<tr>
<td>5</td>
<td>nIRQ</td>
<td>nIRQ</td>
<td>DO</td>
<td>Interrupt request output (active low)</td>
</tr>
<tr>
<td>6</td>
<td>DATA / nFFS</td>
<td>DATA</td>
<td>DO</td>
<td>Received data output (FIFO not used)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nFFS</td>
<td>DI</td>
<td>FIFO select input</td>
</tr>
<tr>
<td>7</td>
<td>DCLK</td>
<td>DCLK</td>
<td>DO</td>
<td>Received data clock output (digital filter used, FIFO not used)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FFIT</td>
<td>DO</td>
<td>FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CFIL</td>
<td>AIO</td>
<td>External data filter capacitor connection (analog filter used)</td>
</tr>
<tr>
<td>8</td>
<td>CLK</td>
<td>CLK</td>
<td>DO</td>
<td>Clock output for the microcontroller</td>
</tr>
<tr>
<td>9</td>
<td>XTL / REF</td>
<td>XTL</td>
<td>AIO</td>
<td>Crystal connection (other terminal of crystal to VSS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>REF</td>
<td>DI</td>
<td>External reference input</td>
</tr>
<tr>
<td>10</td>
<td>nRES</td>
<td>nRES</td>
<td>DO</td>
<td>Reset output (active low)</td>
</tr>
<tr>
<td>11</td>
<td>VSS</td>
<td>VSS</td>
<td>S</td>
<td>Negative supply voltage</td>
</tr>
<tr>
<td>12</td>
<td>IN2</td>
<td>IN2</td>
<td>AI</td>
<td>RF differential signal input</td>
</tr>
<tr>
<td>13</td>
<td>IN1</td>
<td>IN1</td>
<td>AI</td>
<td>RF differential signal input</td>
</tr>
<tr>
<td>14</td>
<td>VDD</td>
<td>VDD</td>
<td>S</td>
<td>Positive supply voltage</td>
</tr>
<tr>
<td>15</td>
<td>ARSSI</td>
<td>ARSSI</td>
<td>AO</td>
<td>Analog RSSI output</td>
</tr>
<tr>
<td>16</td>
<td>VDI</td>
<td>VDI</td>
<td>DO</td>
<td>Valid Data Indicator output</td>
</tr>
</tbody>
</table>
GENERAL DEVICE SPECIFICATION

All voltages are referenced to $V_{ss}$, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>Positive supply voltage</td>
<td>-0.5</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Voltage on any pin</td>
<td>-0.5</td>
<td>$V_{dd}$+0.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{in}$</td>
<td>Input current into any pin except VDD and VSS</td>
<td>-25</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic discharge with human body model</td>
<td>1000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$T_{st}$</td>
<td>Storage temperature</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{ld}$</td>
<td>Lead temperature (soldering, max 10 s)</td>
<td></td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

Recommended Operating Range

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions: $T_{op} = 27 \, ^\circ\text{C}$; $V_{dd} = 2.7 \, \text{V}$)

DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions/Notes</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{dd}$</td>
<td>Supply current</td>
<td>868 MHz band</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{sb}$</td>
<td>Standby current</td>
<td>all blocks disabled</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{lb}$</td>
<td>Low battery voltage detector and wake-up timer current</td>
<td>crystal oscillator is ON</td>
<td></td>
<td>0.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{x}$</td>
<td>Idle current</td>
<td>programmable in 0.1 V steps</td>
<td>2.0</td>
<td>3.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{lb}$</td>
<td>Low battery detection threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{ba}$</td>
<td>Low battery detection accuracy</td>
<td></td>
<td>± 0.05</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{POR}$</td>
<td>$V_{dd}$ threshold required to generate a POR</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{POR,hyst}$</td>
<td>POR hysteresis</td>
<td>larger glitches on the $V_{dd}$ generate a POR even above the threshold $V_{POR}$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$SR_{Vdd}$</td>
<td>$V_{dd}$ slew rate</td>
<td>for proper POR generation</td>
<td>0.1</td>
<td></td>
<td></td>
<td>V/ms</td>
</tr>
<tr>
<td>$V_{il}$</td>
<td>Digital input low level</td>
<td></td>
<td></td>
<td>0.3*V_{dd}</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ih}$</td>
<td>Digital input high level</td>
<td></td>
<td>0.7*V_{dd}</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{il}$</td>
<td>Digital input current</td>
<td>$V_{il} = 0 , \text{V}$</td>
<td></td>
<td>-1</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{lh}$</td>
<td>Digital input current</td>
<td>$V_{lh} = V_{dd}, V_{dd} = 3.8 , \text{V}$</td>
<td></td>
<td>-1</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{ol}$</td>
<td>Digital output low level</td>
<td>$I_{ol} = 2 , \text{mA}$</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{oh}$</td>
<td>Digital output high level</td>
<td>$I_{oh} = -2 , \text{mA}$</td>
<td></td>
<td>$V_{dd}$-0.4</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
### AC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions/Notes</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{LO}$</td>
<td>Receiver frequency</td>
<td>868 MHz band, 20 kHz resolution 915 MHz band, 20 kHz resolution</td>
<td>801.92</td>
<td>881.92</td>
<td>878.06</td>
<td>MHz</td>
</tr>
<tr>
<td>BW</td>
<td>Receiver bandwidth</td>
<td>mode 1, mode 2, mode 3, mode 4, mode 5</td>
<td>120</td>
<td>180</td>
<td>240</td>
<td>300</td>
</tr>
<tr>
<td>BR</td>
<td>FSK bit rate</td>
<td>with internal digital filters</td>
<td></td>
<td></td>
<td>115.2</td>
<td>kbps</td>
</tr>
<tr>
<td>BRA</td>
<td>FSK bit rate</td>
<td>with analog filter</td>
<td></td>
<td></td>
<td>256</td>
<td>kbps</td>
</tr>
<tr>
<td>$P_{min}$</td>
<td>Receiver sensitivity</td>
<td>BER $10^{-3}$, BW = 134 kHz, BR = 9.6 kbps</td>
<td>-104</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>$\Delta f_{FSK}$</td>
<td>AFC locking range</td>
<td>$0.8^* \Delta f_{FSK}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIP3_{in}</td>
<td>Input IP3</td>
<td>in band interferers</td>
<td>-21</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>IIP3_{out}</td>
<td>Input IP3</td>
<td>out of band interferers $f_f_{LO} &gt; 4$ MHz</td>
<td>-18</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>CCR</td>
<td>Co-channel rejection</td>
<td>BER = $10^{-2}$ with continuous wave interferer in the channel</td>
<td>-4</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>BR_{1MHz}</td>
<td>Blocking ratio</td>
<td>BER = $10^{-7}$ with continuous wave interferer, BW = 134 kHz, BR = 9.6 kbps, $\Delta f_{FSK} = 80$ kHz, interferer offset 1 MHz</td>
<td>46</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>BR_{2MHz}</td>
<td>Blocking ratio</td>
<td>same as above, interferer offset 2 MHz</td>
<td>49</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>BR_{5MHz}</td>
<td>Blocking ratio</td>
<td>same as above, interferer offset 5 MHz</td>
<td>55</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>BR_{10MHz}</td>
<td>Blocking ratio</td>
<td>same as above, interferer offset 10 MHz</td>
<td>67</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$P_{max}$</td>
<td>Maximum input power</td>
<td>LNA: high gain</td>
<td>0</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Rin</td>
<td>RF input impedance real part (differential) (Note 1)</td>
<td>LNA gain (0, -12dB) LNA gain (-6, -18dB)</td>
<td>250</td>
<td>500</td>
<td></td>
<td>Ohm</td>
</tr>
<tr>
<td>Cin</td>
<td>RF input capacitance</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$R_{S_{in}}$</td>
<td>RSSI accuracy</td>
<td>+/-5</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$R_{S_f}$</td>
<td>RSSI range</td>
<td>46</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$C_{ARSSI}$</td>
<td>Filter capacitance for ARSSI</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>$R_{Step}$</td>
<td>RSSI programmable level steps</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$R_{Resp}$</td>
<td>DRSSI response time</td>
<td>until the RSSI output goes high after the input signal exceeds the pre-programmed limit, $C_{ARSSI} = 5nF$</td>
<td></td>
<td></td>
<td>500</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** See matching circuit parameters and antenna design guide for information, and Application Notes available from http://www.silabs.com.
### AC Characteristics (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions/Notes</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{ref}$</td>
<td>PLL reference frequency</td>
<td>(Note 2)</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{res}$</td>
<td>PLL frequency resolution</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{lock}$</td>
<td>PLL lock time</td>
<td>Frequency error &lt; 1kHz after 1 MHz step</td>
<td>30</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{start, P}$</td>
<td>PLL startup time</td>
<td>Initial calibration after power-up with running crystal oscillator</td>
<td>500</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{start, P}$</td>
<td>PLL startup time</td>
<td>Recalibration after receiver chain enable with running crystal oscillator</td>
<td>60</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$C_{cr}$</td>
<td>Crystal load capacitance, see crystal selection guide</td>
<td>Programmable in 0.5 pF steps, tolerance +/- 10%</td>
<td>8.5</td>
<td>16</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$t_{POR}$</td>
<td>Internal POR pulse width (Note 3)</td>
<td>After $V_{dd}$ has reached 90% of final value</td>
<td>50</td>
<td>100</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{px}$</td>
<td>Crystal oscillator startup time</td>
<td>Crystal ESR &lt; 100 Ω</td>
<td>5</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{clock}$</td>
<td>Wake-up timer clock period</td>
<td>Calibrated every 30 seconds (Note 4)</td>
<td>0.995</td>
<td>1</td>
<td>1.005</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{wake-up}$</td>
<td>Programmable wake-up time</td>
<td></td>
<td>1</td>
<td></td>
<td>$8.4 \times 10^8$</td>
<td>ms</td>
</tr>
<tr>
<td>$C_{in, D}$</td>
<td>Digital input capacitance</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$t_{r, f}$</td>
<td>Digital output rise/fall time</td>
<td>15 pF pure capacitive load</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f, clock}$</td>
<td>Clock output rise/fall time</td>
<td>10 pF pure capacitive load</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$f_{clock, slow}$</td>
<td>Slow clock frequency</td>
<td>Tolerance +/- 1 kHz</td>
<td>32</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

**Note 2:** Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

**Note 3:** During this period, commands are not accepted by the chip.

**Note 4:** Autocalibration can be turned off.
CONTROL INTERFACE

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don’t care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control registers.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

Timing Specification

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum value [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{CH} )</td>
<td>Clock high time</td>
<td>25</td>
</tr>
<tr>
<td>( t_{CL} )</td>
<td>Clock low time</td>
<td>25</td>
</tr>
<tr>
<td>( t_{SS} )</td>
<td>Select setup time (nSEL falling edge to SCK rising edge)</td>
<td>10</td>
</tr>
<tr>
<td>( t_{SH} )</td>
<td>Select hold time (SCK falling edge to nSEL rising edge)</td>
<td>10</td>
</tr>
<tr>
<td>( t_{SHI} )</td>
<td>Select high time</td>
<td>25</td>
</tr>
<tr>
<td>( t_{DS} )</td>
<td>Data setup time (SDI transition to SCK rising edge)</td>
<td>5</td>
</tr>
<tr>
<td>( t_{DH} )</td>
<td>Data hold time (SCK rising edge to SDI transition)</td>
<td>5</td>
</tr>
<tr>
<td>( t_{OD} )</td>
<td>Data delay time</td>
<td>10</td>
</tr>
</tbody>
</table>

Timing Diagram

---

---
Control Commands

<table>
<thead>
<tr>
<th>Control Word</th>
<th>Related Parameters/Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration Setting Command</td>
<td>frequency band, crystal oscillator load capacitance, baseband filter bandwidth, etc.</td>
</tr>
<tr>
<td>Frequency Setting Command</td>
<td>frequency of the local oscillator</td>
</tr>
<tr>
<td>Receiver Setting Command</td>
<td>VDI source, LNA gain, RSSI threshold</td>
</tr>
<tr>
<td>Wake-up Timer Command</td>
<td>wake-up time period</td>
</tr>
<tr>
<td>Extended Wake-up Timer Command</td>
<td>wake-up time period finer adjustment</td>
</tr>
<tr>
<td>Low Battery Detector and Clock Divider Command</td>
<td>LBD voltage and microcontroller clock division ratio</td>
</tr>
<tr>
<td>AFC Control Command</td>
<td>AFC parameters</td>
</tr>
<tr>
<td>Data Rate Command</td>
<td>bit rate</td>
</tr>
<tr>
<td>Data Filter Command</td>
<td>data filter type, clock recovery parameters, POR level selection, autosleep mode</td>
</tr>
<tr>
<td>Output and FIFO Command</td>
<td>FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable</td>
</tr>
<tr>
<td>Extended Features Command</td>
<td>low frequency output clock, wake-up timer extra functions, long FIFO extra functions</td>
</tr>
<tr>
<td>Status Read Command</td>
<td>receiver status read</td>
</tr>
</tbody>
</table>

Note: In the following tables the POR column shows the default values of the command registers after power-on.

Configuration Setting Command

<table>
<thead>
<tr>
<th>bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>bs</td>
<td>eb</td>
<td>et</td>
<td>ex</td>
<td>x3</td>
<td>x2</td>
<td>x1</td>
<td>x0</td>
<td>i2</td>
<td>i1</td>
<td>i0</td>
<td>dc</td>
<td>938Ah</td>
</tr>
</tbody>
</table>

bs  Frequency Band [MHz]

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>868</td>
</tr>
<tr>
<td>1</td>
<td>915</td>
</tr>
</tbody>
</table>

i2  i1  i0  Baseband Bandwidth [kHz]

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>reserved</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>340</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>270</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>200</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>134</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>reserved</td>
</tr>
</tbody>
</table>

x3  x2  x1  x0  Crystal Load Capacitance [pF]

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8.5</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>9.0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>9.5</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>10.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>....</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>15.5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>16.0</td>
</tr>
</tbody>
</table>

Bits eb and et control the operation of the low battery detector and wake-up timer, respectively. They are enabled when the corresponding bit is set.

If ex is set the crystal is active during non-active mode.

When dc bit is set it disables the clock output.
Frequency Setting Command

| bit | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  | POR |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
|     | 1  | 0  | 1  | 0  | f11| f10| f9 | f8 | f7 | f6 | f5 | f4 | f3 | f2 | f1 | f0  | AD57h|

The 12-bit Frequency Setting Command \(<f11 : f0>\) has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency \(f_0\) can be calculated as:

\[ f_0 = 8 \times 10 \text{MHz} \times (C + F/4000) \]

Receiver Setting Command

<table>
<thead>
<tr>
<th>bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>d1</td>
<td>d0</td>
<td>g1</td>
<td>g0</td>
<td>r2</td>
<td>r1</td>
<td>r0</td>
<td>en</td>
<td>C080h</td>
<td></td>
</tr>
</tbody>
</table>

Bit 7-6 \(<d1 : d0>\): Select the VDI (valid data indicator) signal:

- d1 0 0: Digital RSSI Out (DRSSI)
- d1 0 1: Data Quality Detector Output (DQD)
- d1 1 0: Clock recovery lock
- d1 1 1: Always

Bit 5-4 \(<g1 : g0>\): Set the LNA gain:

<table>
<thead>
<tr>
<th>g1</th>
<th>g0</th>
<th>G_{LNA} (dB relative to max. G)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>-6</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-12</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-18</td>
</tr>
</tbody>
</table>

Bit 3-1 \(<r2 : r0>\): Control the threshold of the RSSI detector:

<table>
<thead>
<tr>
<th>r2</th>
<th>r1</th>
<th>r0</th>
<th>RSSI_setth [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-103</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-97</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>-91</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-85</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-79</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-73</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-67</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-61</td>
</tr>
</tbody>
</table>

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

\[ \text{RSSI}_{\text{th}} = \text{RSSI}_{\text{setth}} + G_{\text{LNA}} \]

Bit 0 \(<\text{en}>\): Enables the whole receiver chain and crystal oscillator when set. Enable/disable of the wake-up timer and the low battery detector are not affected by this setting.
Wake-Up Timer Command

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>r3</td>
<td>r2</td>
<td>r1</td>
<td>r0</td>
<td>m7</td>
<td>m6</td>
<td>m5</td>
<td>m4</td>
<td>m3</td>
<td>m2</td>
<td>m1</td>
<td>m0</td>
</tr>
</tbody>
</table>

The wake-up time period can be calculated by \( M < m_{13 : m_0} > , \ R < r_{3 : r_0} > \) and \( D < d_{1 : d_0} > : \)

\[
T_{\text{wake-up}} = M \times 2^{R-D} \text{ ms}
\]

Note: The wake-up timer generates interrupts continuously at the programmed interval while the et bit is set.

Extended Wake-Up Timer Command

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td>d1</td>
<td>d0</td>
<td>m13</td>
<td>m12</td>
<td>m11</td>
<td>m10</td>
<td>m9</td>
<td>m8</td>
<td>C300h</td>
</tr>
</tbody>
</table>

These bits can be used for further fine adjustment of the wake-up timer. The explanation of the bits can be found above.

Low Battery Detector and Microcontroller Clock Divider Command

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td>d2</td>
<td>d1</td>
<td>d0</td>
<td>elfc</td>
<td>t3</td>
<td>t2</td>
<td>t1</td>
<td>t0</td>
<td>C213h</td>
</tr>
</tbody>
</table>

The 4-bit value \( T \) of \( t_3-t_0 \) determines the threshold voltage of the threshold voltage \( V_{lb} \) of the detector:

\[
V_{lb} = 2.0 \text{ V} + T \times 0.1 \text{ V}
\]

Bit 4 \(<\text{elfc}>\): Enables low frequency (32 kHz) microcontroller output clock during sleep mode.

Clock divider configuration (valid only if the crystal oscillator is on):

<table>
<thead>
<tr>
<th>d2</th>
<th>d1</th>
<th>d0</th>
<th>Clock Output Frequency [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1.25</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.66</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2.5</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>3.33</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>10</td>
</tr>
</tbody>
</table>

AFC Command

<table>
<thead>
<tr>
<th>Bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>a1</td>
<td>a0</td>
<td>rl1</td>
<td>rl0</td>
<td>st</td>
<td>fi</td>
<td>oe</td>
<td>en</td>
<td>C687h</td>
</tr>
</tbody>
</table>

Bit 0 \(<\text{en}>\): Enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 \(<\text{oe}>\): Enables the output (frequency offset) register

Bit 2 \(<\text{fi}>\): Switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 \(<\text{st}>\): Strobe edge. When st goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.
Bit 5-4 $<r1:r0>$: Limit the value of the frequency offset register to the following values:

<table>
<thead>
<tr>
<th>$r1$</th>
<th>$r0$</th>
<th>Max dev [fres]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>No restriction</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>± 4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>± 2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>± 1</td>
</tr>
</tbody>
</table>

fres:
- 868MHz band: 20 kHz
- 915MHz band: 20 kHz

Bit 7-6 $<a1:a0>$: Automatic operation mode selector:

<table>
<thead>
<tr>
<th>$a1$</th>
<th>$a0$</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Auto off (Strobe is controlled by uC)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Runs only once after each power-up</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Keep the f offset only during receiving (VDI=high)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Keep the f offset value</td>
</tr>
</tbody>
</table>

In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register), the AFC circuit is automatically enabled when VDI indicates a potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

There are three operation modes, example from the possible application:

1. $(a1=0, a0=1)$ The circuit measures the frequency offset only once after power up. This way, the extended TX/RX maximum distance can be achieved. In the final application when the user is inserted the battery the circuit measures and compensates the frequency offset caused by the crystal tolerances. This method enables to use cheaper quartz in the application and provide quite good protection against locking in an interferer.

2a. $(a1=1, a0=0)$ The circuit measures automatically the frequency offset during an initial low data rate pattern – easier to receive – (i.e. 00110011) of the package and change the receiving frequency according that. The further part of the package can be received by the corrected frequency settings.

2b. $(a1=1, a0=0)$ The transmitter must transmit the first part of the packet with a step higher deviation and later it is possible to reduce it. In both cases (2a and 2b) when the VDI indicates poor receiving conditions (VDI goes low) the output register is automatically cleared. It is suggested to use when one receiver receives signal from more than one transmitter.

3. $(a1=1, a0=1)$ It is similar to the 2a and 2b modes, but 3 is suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is held independently of the state of VDI signal.
### Data Filter Command

<table>
<thead>
<tr>
<th>bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>al</td>
<td>ml</td>
<td>dsfi</td>
<td>sf</td>
<td>ewi</td>
<td>f2</td>
<td>f1</td>
<td>f0</td>
<td>C462h</td>
<td></td>
</tr>
</tbody>
</table>

Bit 7 <al>: Clock recovery (CR) auto lock control if set.
It means that the CR start in fast mode after locking it automatically switches to slow mode.

Bit 6 <ml>: Clock recovery lock control
1: fast mode, fast attack and fast release - 0: slow mode, slow attack and slow release
Using the slower one requires more accurate bit timing (see Data Rate Command).

Bit 5 <dsfi>: Disables autosleep on FIFO interrupt if set to 1.

Bit 4 <sf>: Selects the type of the data filter:

<table>
<thead>
<tr>
<th>sf</th>
<th>Filter Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Digital</td>
</tr>
<tr>
<td>1</td>
<td>Analog RC filter</td>
</tr>
</tbody>
</table>

Digital: this is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the Data Rate Command.

Analog RC filter: the demodulator output is fed to the DCK pin over a 10 kOhm resistor. The filter characteristic is set by the external capacitor connected to this pin and VSS. (Suggested value for 9600 bps is 1.8 nF).

Bit 3 <ewi>: Enables the automatic wake-up on any interrupt event.

Bit 2-0 <f0:f2>: DQD threshold parameter.

**Note:** To let the DQD report "good signal quality" the threshold parameter should be less than 4 in the case when the bit rate is close to the deviation. At higher deviation/bitrate settings higher threshold parameter can report "good signal quality" as well.

### Data Rate Command

<table>
<thead>
<tr>
<th>bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>cs</td>
<td>r6</td>
<td>r5</td>
<td>r4</td>
<td>r3</td>
<td>r2</td>
<td>r1</td>
<td>r0</td>
<td>C813h</td>
<td></td>
</tr>
</tbody>
</table>

The expected bit rate of the received data stream is determined by the 7-bit value R (bits r6 to r0) and the 1 bit cs.

BR = \( \frac{10 \text{MHz}}{29 \cdot (R+1)} \cdot \left(1 + cs \cdot 7 \right) \)

In the receiver set R according the next function:

R = \( \left( \frac{10 \text{MHz}}{29 \cdot (1 + cs \cdot 7)} \right) / \text{BR} - 1 \)

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: \( \Delta BR / BR < 1/(29 \cdot N_{up}) \)
Clock recovery in fast mode: \( \Delta BR / BR < 3/(29 \cdot N_{up}) \)

BR is the bit rate set in the receiver and \( \Delta BR \) is bit rate difference between the transmitter and the receiver. \( N_{up} \) is the maximal number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

\( \Delta BR \) is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or Vdd condition.

e.g. Supposing a maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.
**Output and FIFO Mode Command**

<table>
<thead>
<tr>
<th>bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>f3</td>
<td>f2</td>
<td>f1</td>
<td>f0</td>
<td>s1</td>
<td>s0</td>
<td>ff</td>
<td>fe</td>
<td>CE87h</td>
</tr>
</tbody>
</table>

Bit 7-4 \(<f3 : f0>\): FIFO IT level. The FIFO generates IT when the number of the received data bits reaches this level.

Bit 3-2 \(<s1 : s0>\): Select the input of the FIFO fill start condition:

<table>
<thead>
<tr>
<th>s1</th>
<th>s0</th>
<th>VDI</th>
<th>Sync. Word</th>
<th>Always</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>VDI</td>
<td>Sync. Word</td>
<td>Always</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>VDI</td>
<td>Sync. Word</td>
<td>Always</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>VDI</td>
<td>Sync. Word</td>
<td>Always</td>
</tr>
</tbody>
</table>

**Note:**

VDI (Valid Data Indicator) see further details in Receiver Control Word, Synchron word in microcontroller mode is 2DD4h.

Bit 1 \(<ff>\): Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0 \(<fe>\): Enables the 48-bit deep FIFO mode. To clear the counter of the FIFO, it has to be set to zero.

**Note:**

To restart the synchron word reception, bit 1 should be cleared and set.

This action will initialize the FIFO and clear its content.

Bit 0 modifies the function of DATA pin and DCLK pin. The DATA pin will become input (nFFS) if \(fe\) is set to 1. If the chip is used in FIFO mode, do not allow this to be a floating input.
Extended Features Command:

<table>
<thead>
<tr>
<th>bit</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>POR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>B0CAh</td>
</tr>
</tbody>
</table>

Bit 7 <exp>: Enables low power mode for the crystal oscillator.
Bit 6 <ctls>: Clock tail selection bit. Setting this bit selects 512 bit long clock tail instead of the default 128 bit length.
Bit 4 <dcal>: Disables the wake-up timer autocalibration.
Bit 3-2 <bw1:bw0>: Select the bandwidth of the PLL.

<table>
<thead>
<tr>
<th>bw1</th>
<th>bw0</th>
<th>PLL bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>15 kHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>30 kHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>60 kHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>120 kHz</td>
</tr>
</tbody>
</table>

Bit 1-0 <f5:f4>: Upper two bits for selecting the 48 bit FIFO IT level together with the f3-f0 bits in the Output and FIFO Mode Command.
Status Read Command

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the Si4322 identifies it as a read command. So as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:

**Status Register Read Sequence with FIFO Read Example**

![Diagram of status register read sequence with FIFO read example]

Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (FIFO IT - LBD) to clear the FFOV, WK-UP, and LBD bits. During the FIFO access the f_{SCK} cannot be higher than f_{ref}/4, where f_{ref} is the crystal oscillator frequency. If the FIFO is read in this mode the nFFS input must be connected to logic high level.

Definitions of the bits in the above timing diagram:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFIT</td>
<td>The number of data bits in the FIFO has reached the preprogrammed limit</td>
</tr>
<tr>
<td>FFOV</td>
<td>FIFO overflow</td>
</tr>
<tr>
<td>WK-UP</td>
<td>Wake-up timer overflow</td>
</tr>
<tr>
<td>LBD</td>
<td>Low battery detect, the power supply voltage is below the preprogrammed limit</td>
</tr>
<tr>
<td>FFEM</td>
<td>FIFO is empty</td>
</tr>
<tr>
<td>DRSSI</td>
<td>The strength of the incoming signal is above the preprogrammed limit</td>
</tr>
<tr>
<td>DQD</td>
<td>Data Quality Detector detected a good quality signal</td>
</tr>
<tr>
<td>CRL</td>
<td>Clock recovery lock</td>
</tr>
<tr>
<td>ATGL</td>
<td>Toggling in each AFC cycle</td>
</tr>
<tr>
<td>ASAME</td>
<td>AFC measured twice the same result</td>
</tr>
<tr>
<td>OFFS(6)</td>
<td>MSB of the measured frequency offset (sign of the offset value)</td>
</tr>
<tr>
<td>OFFS(4) - OFFS(0)</td>
<td>Offset value to be added to the value of the selected center frequency</td>
</tr>
</tbody>
</table>
FIFO Buffered Data Read

In this operating mode, incoming data are clocked into a 48 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

For further details see the Receiver Setting Command and the Output and FIFO Command.

Polling Mode:
The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:
The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

FIFO Read Example with FFIT Polling:

During FIFO access the f_{SCK} cannot be higher than f_{ref}/4, where f_{ref} is the crystal oscillator frequency.

Power Saving Modes
The different operating modes of the chip depend on the following control bits:

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>eb or et</th>
<th>en</th>
<th>ex</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Configuration Setting Command)</td>
<td>(Receiver Setting Command)</td>
<td>(Configuration Setting Command)</td>
</tr>
<tr>
<td>Active</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Idle</td>
<td>X</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Sleep</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Standby</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
**Dual Clock Output**

When the chip is switched into idle mode, the 10 MHz crystal oscillator starts. After oscillation ramp-up a 1 MHz clock signal is available on the CLK pin. This (fast) clock frequency can be reprogrammed during operation with the Low Battery and Microcontroller Clock Divider Command (page 11). During startup and in sleep or standby mode (crystal oscillator disabled), the CLK output is pulled to logic low.

On the same pin a low frequency clock signal can be obtained if the elfc bit is set in the Low Battery and Microcontroller Clock Divider Command. The clock frequency is 32 kHz which is derived from the low-power RC oscillator of the wake-up timer. In order to use this slow clock the wake-up timer should be enabled by setting the et bit in the Configuration Setting Command (page 9) even if the wake-up timer itself is not used.

Slow clock feature can be enabled by entering into sleep mode (page 17). Driving the output will increase the sleep mode supply current. Actual worst-case value can be determined when the exact load and min/max operating conditions are defined. After power-on reset the chip goes into sleep mode and the slow frequency clock appears on the CLK pin.

Switching back into fast clock mode can be done by setting the ex or en bits in the appropriate commands. It is important to leave bit dc in the Configuration Setting Command at its default state (0) otherwise there will be no clock signal on the CLK pin.

Switching between the fast and slow clock modes is glitch-free in a sense that either state of the clock lasts for at least a half cycle of the fast clock. During switching the clock can be logic low once for an intermediate period i.e. for any time between the half cycle of the fast and the slow clock.

The clock switching synchronization circuit detects the falling edges of the clocks. One consequence is a latency of 0 to \( T_{\text{slow}} + T_{\text{fast}} \) from the occurrence of a clock change request (entering into sleep mode or interrupt) until the beginning of the intermediate length \( T_x \) half cycle. The other is that both clocks should be up and running for the change to occur. Changing from fast to slow clock, it is automatically ensured by entering into the sleep mode in the appropriate way provided that the wake-up timer is continuously enabled. As the crystal oscillator is normally stopped while the slow clock is used, when changing back to fast clock the crystal oscillator startup time has to pass first before the above mentioned latency period starts. The startup condition is detected internally, so no software timing is necessary.

**Wake-Up Timer Calibration**

By default the wake-up timer is calibrated each time it is enabled by setting the et bit in the Configuration Setting Command. After timeout the timer restarts automatically and can be stopped by resetting the et bit. If the timer is programmed to run for longer periods, at app. every 30 seconds it performs additional self-calibration.

This feature can be disabled to avoid sudden changes in the actual wake-up time period. A suitable software algorithm can then compensate for the gradual shift caused by temperature change.

Bit dcal in the Extended Features Command (page 15) controls the automatic calibration feature. It is reset to 0 at power-on and the automatic calibration is enabled. This is necessary to compensate for process tolerances. After one calibration cycle further (re)calibration can be disabled by setting this bit to 1.
RX-TX ALIGNMENT PROCEDURES
RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES
The crystal oscillator of the Si4322 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (fLO). Therefore fLO is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C0.

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.
## PACKAGE INFORMATION

### 16-pin TSSOP

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions in mm</th>
<th>Dimensions in Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.20</td>
<td>0.047</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>0.002</td>
</tr>
<tr>
<td>A2</td>
<td>0.80</td>
<td>0.031</td>
</tr>
<tr>
<td>b</td>
<td>0.30</td>
<td>0.012</td>
</tr>
<tr>
<td>b1</td>
<td>0.22</td>
<td>0.009</td>
</tr>
<tr>
<td>c</td>
<td>0.16</td>
<td>0.004</td>
</tr>
<tr>
<td>c1</td>
<td>0.19</td>
<td>0.004</td>
</tr>
<tr>
<td>D</td>
<td>4.90</td>
<td>0.193</td>
</tr>
<tr>
<td>e</td>
<td>0.65 BSC.</td>
<td>0.026 BSC.</td>
</tr>
<tr>
<td>E</td>
<td>6.40 BSC.</td>
<td>0.252 BSC.</td>
</tr>
<tr>
<td>E1</td>
<td>4.30</td>
<td>0.169</td>
</tr>
<tr>
<td>L</td>
<td>0.50</td>
<td>0.024</td>
</tr>
<tr>
<td>L1</td>
<td>1.00 REF.</td>
<td>0.39 REF.</td>
</tr>
<tr>
<td>R</td>
<td>0.09</td>
<td>0.004</td>
</tr>
<tr>
<td>R1</td>
<td>0.09</td>
<td>0.004</td>
</tr>
<tr>
<td>S1</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>S2</td>
<td>12 REF.</td>
<td>12 REF.</td>
</tr>
<tr>
<td>S3</td>
<td>12 REF.</td>
<td>12 REF.</td>
</tr>
</tbody>
</table>
This page has been intentionally left blank.
### ORDERING INFORMATION

**Si4322 Universal ISM Band FSK Receiver**

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>ORDERING NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si4322 16-pin TSSOP die</td>
<td>Si4322-IC CC16 Rev A0</td>
</tr>
<tr>
<td></td>
<td>see Silicon Labs</td>
</tr>
</tbody>
</table>

**Demo Boards and Development Kits**

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>ORDERING NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISM Chipset Development Kit</td>
<td>IA ISM – DK3</td>
</tr>
</tbody>
</table>

**Related Resources**

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>ORDERING NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antenna Selection Guide</td>
<td>IA ISM – AN1</td>
</tr>
<tr>
<td>Antenna Development Guide</td>
<td>IA ISM – AN2</td>
</tr>
<tr>
<td>Si4222 Universal ISM Band FSK Transmitter</td>
<td>see <a href="http://www.silabs.com/integration">http://www.silabs.com/integration</a> for details</td>
</tr>
</tbody>
</table>

*Note: Volume orders must include chip revision to be accepted.*

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