bq29700 Cost-Effective Voltage and Current Protection Integrated Circuit for Single-Cell Li-Ion/Li-Polymer Batteries

ECCN: EAR99

1 Features

- Input Voltage Range Pack+: VSS – 0.3 V to 12 V
- FET Drive:
  - CHG and DSG FET Drive Output
- Voltage Sensing Across External FETs for Overcurrent Protection (OCP) Is Within ± 5 mV (Typical)
- Fault Detection
  - Overcharge Detection (OVP)
  - Over-Discharge Detection (UVP)
  - Charge Overcurrent Detection (OCC)
  - Discharge Overcurrent Detection (OCD)
  - Load Short-Circuit Detection (SCP)
- Zero Voltage Charging for Depleted Battery
- Factory Programmed Fault Protection Thresholds
  - Fault Detection Voltage Thresholds
  - Fault Trigger Timers
  - Fault Recovery Timers
- Modes of Operation Without Battery Charger Enabled
  - NORMAL Mode I_{CC} = 4 µA
  - Shutdown I_q = 100 nA
- Operating Temperature Range T_A = –40°C to 85°C
- Package:
  - 6-Pin DSE (1.5 mm × 1.5 mm × 0.75 mm)

2 Applications

- Tablet PC
- Mobile Handset
- Handheld Data Terminals

3 Description

The bq29700 battery cell protection device provides an accurate monitor and trigger threshold for overcurrent protection during high discharge/charge current operation or battery overcharge conditions. The bq29700 device provides the protection functions for Li-Ion/Li-Polymer cells, and monitors across the external power FETs for protection due to high charge or discharge currents. In addition, there is overcharge and depleted battery monitoring and protection. These features are implemented with low current consumption in NORMAL mode operation.

Device Information

<table>
<thead>
<tr>
<th>ORDER NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq29700DSE</td>
<td>WSON (6)</td>
<td>1.5 mm × 1.5 mm</td>
</tr>
</tbody>
</table>

4 Simplified Schematic

![Simplified Schematic](image)

OCD Detection Accuracy Versus Temperature

![OCD Detection Accuracy](image)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
# Table of Contents

1 Features .................................................................. 1
2 Applications ........................................................... 1
3 Description ............................................................. 1
4 Simplified Schematic ............................................... 1
5 Revision History ...................................................... 2
6 Terminal Configuration and Functions ....................... 3
   6.1 Terminal Descriptions ........................................ 3
7 Specifications .......................................................... 4
   7.1 Absolute Maximum Ratings ................................ 4
   7.2 Handling Ratings .............................................. 4
   7.3 Recommended Operating Conditions .................... 4
   7.4 Thermal Information .......................................... 5
   7.5 DC Characteristics ........................................... 5
   7.6 Programmable Fault Detection Thresholds ............ 5
   7.7 Programmable Fault Detection Timer Ranges ........ 6
8 Typical Characteristics ............................................. 7
9 Parameter Measurement Information ......................... 10
   9.1 Timing Charts .................................................. 10
   9.2 Test Circuits .................................................... 12
9.3 Test Circuit Diagrams ............................................ 14
10 Detailed Description ............................................... 15
   10.1 Overview ....................................................... 15
   10.2 Functional Block Diagram .................................. 15
   10.3 Feature Description ......................................... 15
   10.4 Device Functional Modes .................................. 16
11 Applications and Implementation ............................. 19
   11.1 Application Information .................................... 19
   11.2 Typical Application ........................................ 19
12 Power Supply Recommendations .............................. 22
13 Layout ............................................................... 22
   13.1 Layout Guidelines .......................................... 22
   13.2 Layout Example ............................................. 22
14 Device and Documentation Support .......................... 23
   14.1 Trademarks ................................................... 23
   14.2 Electrostatic Discharge Caution ......................... 23
   14.3 Export Control Notice ..................................... 23
   14.4 Glossary ..................................................... 23
15 Mechanical, Packaging, and Orderable Information ...... 23

# 5 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 2014</td>
<td>*</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
6 Terminal Configuration and Functions

(DSE) 6 TERMINAL

<table>
<thead>
<tr>
<th>Terminal Number</th>
<th>Terminal Label</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>NC</td>
<td>No Connection (electrically open, do not connect to BAT or VSS)</td>
</tr>
<tr>
<td>2</td>
<td>COUT</td>
<td>O</td>
<td>Gate Drive Output for Charge FET</td>
</tr>
<tr>
<td>3</td>
<td>DOUT</td>
<td>O</td>
<td>Gate Drive Output for Discharge FET</td>
</tr>
<tr>
<td>4</td>
<td>VSS</td>
<td>P</td>
<td>Ground terminal</td>
</tr>
<tr>
<td>5</td>
<td>BAT</td>
<td>P</td>
<td>VDD terminal</td>
</tr>
<tr>
<td>6</td>
<td>V–</td>
<td>I/O</td>
<td>Input terminal for charger negative voltage</td>
</tr>
</tbody>
</table>

6.1 Terminal Descriptions

6.1.1 Supply Input: BAT
This terminal is the input supply for the device and is connected to the positive terminal of the battery pack. There is a 0.1-µF input capacitor to ground for filtering noise.

6.1.2 Cell Negative Connection: VSS
This terminal is an input to the device for cell negative ground reference. Internal circuits associated with cell voltage measurements and overcurrent protection input to differential amplifier for either Vds sensing or external sense resistor sensing will be referenced to this node.

6.1.3 Voltage Sense Node: V–
This is a sense node used for measuring several fault detection conditions, such as overcurrent charging or overcurrent discharging configured as Vds sensing for protection. This input, in conjunction with VSS terminal, forms the differential measurement for the stated fault detection conditions. A 2.2-k resistor is connected between this input terminal and Pack– terminal of the system in the application.

6.1.4 Discharge FET Gate Drive Output: DOUT
This terminal is an output to control the discharge FET. The output is driven from an internal circuitry connected to the BAT supply. This output will transition from high to low when a fault is detected, and requires the DSG FET to turn OFF. A high impedance resistor of 5 MΩ is connected from DOUT to VSS for gate capacitance discharge when the FET is turned OFF.

6.1.5 Charge FET Gate Drive Output: COUT
This terminal is an output to control the charge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the CHG FET to turn OFF. A high impedance resistor of 5 MΩ is connected from COUT to Pack– for gate capacitance discharge when FET is turned OFF.
## 7 Specifications

### 7.1 Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Supply Control/Input</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage: BAT</td>
<td>–0.3</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>V– Terminal (Pack–)</td>
<td>BAT – 28</td>
<td>BAT + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>DOUT (Discharge FET Output), GDSG (Discharge FET Gate Drive)</td>
<td>VSS – 0.3</td>
<td>BAT + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>COUT (Charge FET Output), GCHG (Charge FET Gate Drive)</td>
<td>BAT – 28</td>
<td>BAT + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature: T(_{\text{FUNC}})</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 Handling Ratings

<table>
<thead>
<tr>
<th>T(_{\text{stg}})</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature Range</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>V(_{\text{ESD}})((^{(1)}))</td>
<td>–2</td>
<td>2</td>
<td>kV</td>
</tr>
<tr>
<td>Charged Device Model (CDM) ESD stress voltage((^{(2)}))</td>
<td>–500</td>
<td>500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Terminals listed as 1000 V may have higher performance.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Terminals listed as 250 V may have higher performance.

### 7.3 Recommended Operating Conditions\(^{(1)}\)

<table>
<thead>
<tr>
<th>Supply Control/Input</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive Input Voltage: BAT</td>
<td>–0.3</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>Negative Input Voltage: V–</td>
<td>BAT – 25</td>
<td>BAT</td>
<td>V</td>
</tr>
<tr>
<td>Discharge FET Control: DOUT</td>
<td>VSS</td>
<td>BAT</td>
<td>V</td>
</tr>
<tr>
<td>Charge FET Control: COUT</td>
<td>BAT – 25</td>
<td>BAT</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature: T(_{\text{Amb}})</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature: T(_{\text{S}})</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering 10 s)</td>
<td>300</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance Junction to Ambient, (\theta_{\text{JA}})((^{(1)}))</td>
<td>250</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC package Thermal Metrics application report, SPRA953.
7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>DSE (12 Terminals)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{JA}, \text{High K}}$</td>
<td>190.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{JC}(\text{top})}$</td>
<td>94.9</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{JB}}$</td>
<td>149.3</td>
<td></td>
</tr>
<tr>
<td>$\psi_{\text{JT}}$</td>
<td>6.4</td>
<td></td>
</tr>
<tr>
<td>$\psi_{\text{JB}}$</td>
<td>152.8</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{JC}(\text{bottom})}$</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPR953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, $\psi_{\text{JT}}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\text{JA}}$, using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, $\psi_{\text{JB}}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\text{JA}}$, using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 DC Characteristics

Typical Values stated where $T_A = 25^\circ\text{C}$ and BAT = 3.6 V. Min/Max values stated where $T_A = –40^\circ\text{C}$ to 85°C, and BAT = 3.0 V to 4.2 V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{BAT}}$</td>
<td>Device Operating Range</td>
<td>BAT – VSS</td>
<td>1.5</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{NORMAL}}$</td>
<td>Current Consumption in NORMAL Mode</td>
<td>BAT = 3.8 V, V– = 0 V</td>
<td>4</td>
<td>5.5</td>
<td>μA</td>
</tr>
</tbody>
</table>
| $I_{\text{Power
down}}$ | Current Consumption in Power Down Mode | BAT = V– = 1.5 V | 0.1 | μA |
| $V_{\text{OL}}$ | Charge FET Low Output | $I_{\text{OL}} = 30$ μA, BAT = 3.8 V | 0.4 | 0.5 | V |
| $V_{\text{OH}}$ | Charge FET High Output | $I_{\text{OH}} = –30$ μA, BAT = 3.8 V | 3.4 | 3.7 | V |
| $V_{\text{OL}}$ | Discharge FET Low Output | $I_{\text{OL}} = 30$ μA, BAT = 2.0 V | 0.2 | 0.5 | V |
| $V_{\text{OH}}$ | Discharge FET High Output | $I_{\text{OH}} = –30$ μA, BAT = 3.8 V | 3.4 | 3.7 | V |
| $R_{\text{V–-D}}$ | Resistance between V– and VBAT | $V_{\text{BAT}} = 1.8$ V, V– = 0 V | 100 | 300 | 550 | kΩ |
| $I_{\text{V–-S}}$ | Current sink on V– to VSS | $V_{\text{BAT}} = 3.8$V | 8 | 24 | μA |
| $V_{\text{short}}$ | Short detection voltage | $V_{\text{BAT}} = 3.8$ V and $R_{\text{PackN}} = 2.2$ kΩ | $V_{\text{BAT}} – 1$ V | V |
| $V_{\text{OCHG}}$ | 0-V battery charging starter voltage | 0-V battery charging function allowed | 1.7 | V |
| $V_{\text{BINH}}$ | 0-V battery charging inhibit voltage | 0-V battery charging function disallowed | 0.75 | V |

7.6 Programmable Fault Detection Thresholds

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>RANGE</th>
<th>ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over-charge detection voltage ($V_{\text{OVP}}$)</td>
<td>3.85 V to 4.6 V in 50-mV steps</td>
<td>±10 mV at $T_A = 25^\circ\text{C}$</td>
</tr>
<tr>
<td>Overcharge release hysteresis voltage ($V_{\text{OVP–Hys}}$)</td>
<td>100 mV and (VSS – V–) &gt; OCC (min) for release</td>
<td>±20 mV at $T_A = 0^\circ\text{C}$ to 60°C</td>
</tr>
<tr>
<td>Over-discharge detection voltage ($V_{\text{UVP}}$)</td>
<td>2.0 V to 2.80 V in 50 mV steps</td>
<td>±50 mV at $T_A = 25^\circ\text{C}$</td>
</tr>
</tbody>
</table>
Programmable Fault Detection Thresholds (continued)

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>RANGE</th>
<th>ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over-discharge release hysteresis voltage (V_{UVP+Hys})</td>
<td>100 mV and (BAT – V–) &gt; 1 V for release</td>
<td>±50 mV at T_A = 25°C</td>
</tr>
<tr>
<td>Discharging overcurrent detection voltage (V_{OCC})</td>
<td>90 mV to 200 mV in 5-mV steps</td>
<td>±10 mV (Typ) at T_A = 25°C</td>
</tr>
<tr>
<td>Release of V_{OCC}</td>
<td>Release when BAT – V– &gt; 1 V</td>
<td>1 V (Typ)</td>
</tr>
<tr>
<td>Charging overcurrent detection voltage (V_{OCC})</td>
<td>–45 mV to –155 mV in 5-mV steps</td>
<td>±10 mV at T_A = 25°C</td>
</tr>
<tr>
<td>Release of V_{OCC}</td>
<td>Release when VSS – V ≥ OCC (min)</td>
<td>40 mV (Typ)</td>
</tr>
<tr>
<td>Short Circuit detection voltage (V_{SCC})</td>
<td>Select, 300 mV, 400 mV, 500 mV, and 600 mV</td>
<td>±100 mV at T_A = 25°C</td>
</tr>
<tr>
<td>Release of Short Circuit detection voltage (V_{SCCR})</td>
<td>Release when BAT – V ≥ 1 V</td>
<td>1 V (Typ)</td>
</tr>
</tbody>
</table>

7.7 Programmable Fault Detection Timer Ranges

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>RANGE</th>
<th>ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over-charge (t_{OVPD}) detection delay time</td>
<td>Select from 0.25 s, 1.0 s, 1.25 s, 4.5 s</td>
<td>±20%</td>
</tr>
<tr>
<td>Over-discharge (t_{UVPD}) detection delay time</td>
<td>Select from 20 ms, 96 ms, 125 ms, 144 ms</td>
<td>±20%</td>
</tr>
<tr>
<td>Discharging overcurrent (t_{OCDD}) detection delay time</td>
<td>Select from 8 ms, 16 ms, 20 ms, 48 ms</td>
<td>±20%</td>
</tr>
<tr>
<td>Charging overcurrent (t_{OCCD}) detection delay time</td>
<td>Select from 4 ms, 6 ms, 8 ms, 16 ms</td>
<td>±20%</td>
</tr>
<tr>
<td>Short Circuit detection delay time (t_{SCCD})</td>
<td>250 µs fixed</td>
<td>±50%</td>
</tr>
</tbody>
</table>
8 Typical Characteristics

**Figure 1.** 1.5-V $I_{BAT}$ Vs. Temperature

**Figure 2.** 3.9-V $I_{BAT}$ Vs. Temperature

**Figure 3.** Internal Oscillator Frequency Vs. Temperature

**Figure 4.** 0-V Charging Allowed Vs. Temperature

**Figure 5.** 0-V Charging Disallowed Vs. Temperature

**Figure 6.** OVP Detection Accuracy Vs. Temperature

$V_{BAT} = 3.9$ V

$V_{BAT} = 1.5$ V

$F_{OSC}$, Setting = 1.255 kHz

$V_{(B)} - $ VSS Voltage (V)

$V_{BAT}$, Setting = 0 V

OVP, Setting = 4.275 V

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Typical Characteristics (continued)

Figure 7. OVP Detection Delay Time Vs. Temperature

Figure 8. UVP Detection Accuracy Vs. Temperature

Figure 9. UVP Detection Delay Time Vs. Temperature

Figure 10. OCC Detection Accuracy Vs. Temperature

Figure 11. OCC Detection Delay Time Vs. Temperature

Figure 12. OCD Detection Accuracy Vs. Temperature
Typical Characteristics (continued)

![Graph 1: OCD Detection Delay Time Vs. Temperature](image1)

![Graph 2: SCC Detection Accuracy Vs. Temperature](image2)

![Graph 3: Power On Reset Vs. Temperature](image3)

![Graph 4: COUT Vs. Temperature with \(I_{oh} = -30\ \mu A\)](image4)

![Graph 5: DOUT Vs. Temperature with \(I_{oh} = -30\ \mu A\)](image5)

**Figure 13. OCD Detection Delay Time Vs. Temperature**

**Figure 14. SCC Detection Accuracy Vs. Temperature**

**Figure 15. Power On Reset Vs. Temperature**

**Figure 16. COUT Vs. Temperature with \(I_{oh} = -30\ \mu A\)**

**Figure 17. DOUT Vs. Temperature with \(I_{oh} = -30\ \mu A\)**
9 Parameter Measurement Information

9.1 Timing Charts

Figure 18. 1. Overcharge Detection, Over-Discharge Detection
Figure 19. Discharge Overcurrent Detection
9.2 Test Circuits

The following tests are referenced as follows: The COUT and DOUT outputs are “H,” which are higher than the threshold voltage of the external logic level FETs and regarded as ON state. Conversely, “L” is less than the turn ON threshold for external NMOS FETs and regarded as OFF state. The COUT terminal is with respect to V–, and the DOUT terminal is with respect to VSS.

1. **Overcharge detection voltage and overcharge release voltage (Test Circuit 1):**

   The overcharge detection voltage ($V_{OVP}$) is measured between the BAT and VSS terminals, respectively. Once $V_1$ is increased, the over-detection is triggered, and the delay timer expires, the COUT terminal transitions from a high to low state and then reduces the $V_1$ voltage to check for the overcharge hysteresis parameter ($V_{OVP-Hys}$). This delta voltage between overcharge detection voltages ($V_{OVP}$) and the overcharge release occurs when the CHG FET drive output goes from low to high.

2. **Over-discharge detection voltage and over-discharge release voltage (Test Circuit 2):**

   Over-discharge detection ($V_{UVP}$) is defined as the voltage between BAT and VSS at which the DSG drive output goes from high to low by reducing the $V_1$ voltage. $V_1$ is set to 3.5 V and gradually reduced while $V_2$ is set to 0 V. The over-discharge release voltage is defined as the voltage between BAT and VSS at which the DOUT drive output transition from low to high when $V_1$ voltage is gradually increased from a $V_{UVP}$ condition. The overcharge hysteresis voltage is defined as the delta voltage between $V_{UVP}$ and the instance at which the DOUT output drive goes from low to high.

3. **Discharge overcurrent detection voltage (Test Circuit 2):**

   The discharge overcurrent detection voltage ($V_{OCD}$) is measured between V– and VSS terminals and triggered when the $V_2$ voltage is increased above $V_{OCD}$ threshold with respect to VSS. This delta voltage once satisfied will trigger an internal timer $t_{OCDD}$ before the DOUT output drive transitions from high to low.

4. **Load short circuit detection voltage (Test Circuit 2):**

   Load short-circuit detection voltage ($V_{SCC}$) is measured between V– and VSS terminals and triggered when the $V_2$ voltage is increased above $V_{SCC}$ threshold with respect to VSS within 10 µs. This delta voltage, once satisfied, triggers an internal timer $t_{SCCD}$ before the DOUT output drive transitions from high to low.

5. **Charge overcurrent detection voltage (Test Circuit 2):**

   The charge overcurrent detection voltage ($V_{OCC}$) is measured between VSS and V– terminals and triggered when the $V_2$ voltage is increased above $V_{OCC}$ threshold with respect to V–. This delta voltage, once satisfied, triggers an internal timer $t_{OCCD}$ before the COUT output drive transitions from high to low.

6. **Operating current consumption (Test Circuit 2):**

   The operating current consumption $I_{NORMAL}$ is the current measured going into the BAT terminal under the following conditions: $V_1 = 3.9$ V and $V_2 = 0$ V.

7. **Power down current consumption (Test Circuit 2):**

   The operating current consumption $I_{POWER\_DOWN}$ is the current measured going into the BAT terminal under the following conditions: $V_1 = 1.5$ V and $V_2 = 1.5$ V.

8. **Resistance between V– and BAT terminal (Test Circuit 3):**

   Measure the resistance ($R_{V-D}$) between V– and BAT terminals by setting the following conditions: $V_1 = 1.8$ V and $V_2 = 0$ V.

9. **Current sink between V– and VSS (Test Circuit 3):**

   Measure the current sink $I_{V-S}$ between V– and VSS terminals by setting the following condition: $V_1 = 4$ V.

10. **COUT current source when activated High (Test Circuit 4):**

    Measure $I_{COUT}$ current source on the COUT terminal by setting the following conditions: $V_1 = 3.9$ V, $V_2 = 0$ V and $V_3 = 3.4$ V.

11. **COUT current sink when activated Low (Test Circuit 4):**

    Measure $I_{COUT}$ current sink on COUT terminal by setting the following conditions: $V_1 = 4.5$ V, $V_2 = 0$ V and $V_3 = 0.5$ V.
Test Circuits (continued)

12. **DOUT current source when activated High (Test Circuit 4):**

   Measure $I_{DOUT}$ current source on DOUT terminal by setting the following conditions: $V1 = 3.9 \, \text{V}$, $V2 = 0 \, \text{V}$ and $V3 = 3.4 \, \text{V}$.

13. **DOUT current sink when activated Low (Test Circuit 4):**

   Measure $I_{DOUT}$ current sink on DOUT terminal by setting the following conditions: $V1 = 2.0 \, \text{V}$, $V2 = 0 \, \text{V}$ and $V3 = 0.4 \, \text{V}$.

14. **Overcharge detection delay (Test Circuit 5):**

   The overcharge detection delay time $t_{OVPD}$ is the time delay before the COUT drive output transitions from high to low once the voltage on V1 exceeds the $V_{OVP}$ threshold. Set $V2 = 0 \, \text{V}$ and then increase V1 until BAT input exceeds the $V_{OVP}$ threshold and to check the time for when COUT goes from high to low.

15. **Over-discharge detection delay (Test Circuit 5):**

   The over-discharge detection delay time $t_{UVPD}$ is the time delay before the DOUT drive output transitions from high to low once the voltage on V1 decreases to $V_{UVP}$ threshold. Set $V2 = 0 \, \text{V}$ and then decrease V1 until BAT input reduces to the $V_{UVP}$ threshold and to check the time of when DOUT goes from high to low.

16. **Discharge overcurrent detection delay (Test Circuit 5):**

   The discharge overcurrent detection delay time $t_{OCDD}$ is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0 V to 0.35 V, with $V1 = 3.5 \, \text{V}$ and V2 starts from 0 V and increases to trigger threshold.

17. **Load short circuit detection delay (Test Circuit 5):**

   The load short-circuit detection delay time $t_{SCCD}$ is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0 V to $V1 - 1 \, \text{V}$, with $V1 = 3.5 \, \text{V}$ and V2 starts from 0 V and increases to trigger threshold.

18. **Charge overcurrent detection delay (Test Circuit 5):**

   The charge overcurrent detection delay time $t_{OCCD}$ is the time for COUT drive output to transition from high to low after the voltage on V2 is decreased from 0 V to $-0.3 \, \text{V}$, with $V1 = 3.5 \, \text{V}$ and V2 starts from 0 V and decreases to trigger threshold.

19. **0-V battery charge starting charger voltage (Test Circuit 2):**

   The 0-V charge for start charging voltage $V_{0CHA}$ is defined as the voltage between BAT and $V-$ terminals at which COUT goes high when voltage on V2 is gradually decreased from a condition of $V1 = V2 = 0 \, \text{V}$.

20. **0-V battery charge inhibition battery voltage (Test Circuit 2):**

   The 0-V charge inhibit for charger voltage $V_{0INH}$ is defined as the voltage between BAT and VSS terminals at which COUT should go low as V1 is gradually decreased from $V1 = 2 \, \text{V}$ and $V2 = -4 \, \text{V}$. 
9.3 Test Circuit Diagrams

Figure 20. Test Circuit 1

Figure 21. Test Circuit 2

Figure 22. Test Circuit 3

Figure 23. Test Circuit 4

Figure 24. Test Circuit 5
10 Detailed Description

10.1 Overview
This bq297xy device is a primary protector for a single-cell Li-Ion/Li-Polymer battery pack. The device uses a minimum number of external components to protect for overcurrent conditions due to high discharge/charge currents in the application. In addition, it monitors and helps to protect against battery pack overcharging or depletion of energy in the pack. The bq297xy device is capable of having an input voltage of 8 V from a charging adapter and can tolerate a voltage of BAT – 25 V across the two input terminals. In the condition when a fault is triggered, there are timer delays before the appropriate action is taken to turn OFF either the CHG or DSG FETs. There is also a timer delay for the recovery period once the threshold for recovery condition is satisfied. These parameters are fixed once they are programmed. There is also a feature called zero voltage charging that enables depleted cells to be charged to a acceptable level before the battery pack can be used for normal operation. Zero voltage charging is allowed if the charger voltage is above 1.7 V.

10.2 Functional Block Diagram

10.3 Feature Description
The bq297xy family of devices measures voltage drops across several input terminals for monitoring and detection of the following faults: OCC, OCD, OVP, and UVP. An internal oscillator initiates a timer to the fixed delays associated with each parameter once the fault is triggered. Once the timer expires due to a fault condition, the appropriate FET drive output (COUT or DOUT) is activated to turn OFF the external FET. The same method is applicable for the recovery feature once the system fault is removed and the recovery parameter is satisfied, then the recovery timer is initiated. If there are no reoccurrences of this fault during this period, the appropriate gate drive is activated to turn ON the appropriate external FET.
10.4 Device Functional Modes

10.4.1 Normal Operation

This device monitors the voltage of the battery connected between BAT terminal and VSS terminal and the differential voltage between V– terminal and VSS terminal to control charging and discharging. The system is operating in NORMAL mode when the battery voltage range is between the over-discharge detection threshold ($V_{UVP}$) and the overcharge detection threshold ($V_{OVP}$), and the V– terminal voltage is within the range for charge overcurrent threshold ($V_{OCC}$) to over-discharge current threshold ($V_{OCD}$) when measured with respect to VSS. If these conditions are satisfied, the device turns ON the drive for COUT and DOUT FET control.

**CAUTION**

When the battery is connected for the first time, the discharging circuit may not be enabled. In this case, short the V– terminal to the VSS terminal.

Alternatively, connect the charger between the Pack+ and Pack– terminals in the system.

10.4.2 Overcharge Status

This mode is detected when the battery voltage measured is higher than the overcharge detection threshold ($V_{OVP}$) during charging. If this condition exists for a period greater than the overcharge detection delay ($t_{OVPD}$) or longer, the COUT output signal is driven low to turn OFF the charging FET to prevent any further charging of the battery.

The overcharge condition is released if one of the following conditions occurs:

- If the V– terminal is higher than the overcharge detection voltage ($V_{OCC\_Min}$), the device releases the overcharge status when the battery voltage drops below the overcharge release voltage ($V_{OVP\_Hys}$).
- If the V– terminal is higher than or equal to the over-discharge detection voltage ($V_{OCD}$), the device releases the overcharge status when the battery voltage drops below the overcharge detection voltage ($V_{OVP}$).

The discharge is initiated by connecting a load after the overcharge detection. The V– terminal rises to a voltage greater than VSS due to the parasitic diode of the charge FET conducting to support the load. If the V– terminal voltage is higher than or equal to the discharge overcurrent detection threshold ($V_{OCD}$), the overcurrent condition status is released only if the battery voltage drops lower than or equal to the overcharge detection voltage ($V_{OVP}$).

**CAUTION**

1. If the battery is overcharged to a level greater than overcharge detection ($V_{OVP}$) and the battery voltage does not drop below the overcharge detection voltage ($V_{OVP}$) with a heavy load connected, the discharge overcurrent and load short-circuit detection features do not function until the battery voltage drops below the overcharge detection voltage ($V_{OVP}$). The internal impedance of a battery is in the order of tens of mΩ, so application of a heavy load on the output should allow the battery voltage to drop immediately, enabling discharge overcurrent detection and load short-circuit detection features after an overcharge release delay.

2. When a charger is connected after an overcharge detection, the overcharge status does not release even if the battery voltage drops below the overcharge release threshold. The overcharge status is released when the V– terminal voltage exceeds the overcurrent detection voltage ($V_{OCD}$) by removing the charger.
Device Functional Modes (continued)

10.4.3 Over-Discharge Status

If the battery voltage drops below the over-discharge detection voltage \( V_{UVP} \) for a time greater than \( t_{UVPD} \) the discharge control output, DOUT is switched to a low state and the discharge FET is turned OFF to prevent further discharging of the battery. This is referred to as an over-discharge detection status. In this condition, the V– terminal is internally pulled up to BAT by the resistor \( R_{V-D} \). When this occurs, the voltage difference between V– and BAT terminals is 1.3 V or lower, and the current consumption of the device is reduced to power-down level \( I_{STANDBY} \). The current sink \( I_{V-S} \) is not active in power-down state or over-discharge state. The power-down state is released when a charger is connected and the voltage delta between V– and BAT terminals is greater than 1.3 V.

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is lower than −0.7 V, the device releases the over-discharge state and allows the DOUT terminal to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection voltage \( V_{UVP} \).

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is higher than −0.7 V, the device releases the over-discharge state and allows the DOUT terminal to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection release hysteresis voltage \( V_{UVP +Hys} \).

10.4.4 Discharge Overcurrent Status (Discharge Overcurrent, Load Short-Circuit)

When a battery is in normal operation and the V– terminal is equal to or higher than the discharge overcurrent threshold for a time greater than the discharge overcurrent detection delay, the DOUT terminal is pulled low to turn OFF the discharge FET and prevent further discharge of the battery. This is known as the discharge overcurrent status. In the discharge overcurrent status, the V– and VSS terminals are connected by a constant current sink \( I_{V-S} \). When this occurs and a load is connected, the V– terminal is at BAT potential. If the load is disconnected, the V– terminal goes to VSS (BAT/2) potential.

This device detects the status when the impedance between Pack+ and Pack– (see Figure 2) increases and is equal to the impedance that enables the voltage at the V– terminal to return to BAT – 1 V or lower. The discharge overcurrent status is restored to the normal status.

Alternatively, by connecting the charger to the system, the device returns to normal status from discharge overcurrent detection status, because the voltage at the V– terminal drops to BAT – 1 V or lower.

The resistance \( R_{V-D} \) between V– and BAT is not connected in the discharge overcurrent detection status.

10.4.5 Charge Overcurrent Status

When a battery is in normal operation status and the voltage at V– terminal is lower than the charge overcurrent detection due to high charge current for a time greater than charge overcurrent detection delay, the COUT terminal is pulled low to turn OFF the charge FET and prevent further charging to continue. This is known as charge overcurrent status.

The device is restored to normal status from charge overcurrent status when the voltage at the V– terminal returns to charge overcurrent detection voltage or higher by removing the charger from the system.

The charge overcurrent detection feature does not work in the over-discharge status.

The resistance \( R_{V-D} \) between V– and BAT and the current sink \( I_{V-S} \) is not connected in the charge overcurrent status.

10.4.6 0-V Charging Function (Available)

This feature enables recharging a connected battery that has very low voltage due to self-discharge. When the 0-V battery charge starting charger voltage \( V_{0CHG} \) or higher voltage is applied to Pack+ and Pack– connections by the charger, the COUT terminal gate drive is fixed by the BAT terminal voltage.

Once the voltage between the gate and the source of the charging FET becomes equal to or greater than the turn ON voltage due to the charger voltage, the charging FET is ON and the battery is charged with current flow through the charging FET and the internal parasitic diode of the discharging FET. Once the battery voltage is equal to or higher than the over-discharge release voltage, the device enters normal status.
Device Functional Modes (continued)

**CAUTION**

1. Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the 0-V battery charger function.
2. The 0-V battery charge feature has a higher priority than the charge overcurrent detection function. In this case, the 0-V charging will be allowed and the battery charges forcibly, which results in charge overcurrent detection being disabled if the battery voltage is lower than the over-discharge detection voltage.

### 10.4.7 0-V Charging Function (Unavailable)

This feature inhibits recharging a battery that has an internal short circuit of a 0-V battery. If the battery voltage is below the charge inhibit voltage $V_{0INH}$ or lower, the charge FET control gate is fixed to the Pack–voltage to inhibit charging. When battery is equal to $V_{0INH}$ or higher, charging can be performed.

**CAUTION**

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to enable or inhibit the 0-V battery charger function.

### 10.4.8 Delay Circuit

The detection delay timers are based from an internal clock with a frequency of 10 kHz.

If the over-discharge current is detected, but remains below the over-discharge short circuit detection threshold, the over-discharge detection conditions must be valid for a time greater than or equal to over-discharge current delay $t_{OCCD}$ time before the DOUT goes low to turn OFF the discharge FET. However, during any time the discharge overcurrent detection exceeds the short circuit detection threshold for a time greater than or equal to load circuit detection delay $t_{SCCD}$, the DOUT terminal goes low in a faster delay for protection.
11 Applications and Implementation

11.1 Application Information
The bq297xy devices are a family of primary protectors used for protection of the battery pack in the application. The application drives two low-side NMOS FETs that are controlled to provide energy to the system loads or interrupt the power in the event of a fault condition.

11.2 Typical Application

![Typical Application Schematic, bq297xy](image)

**NOTE:** The 5-M resistor for an external gate-source is optional.

**Figure 25. Typical Application Schematic, bq297xy**

11.2.1 Design Requirements

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE at Ta = 25°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>4.5 V to 7 V</td>
</tr>
<tr>
<td>Maximum operating discharge current</td>
<td>7 A</td>
</tr>
<tr>
<td>Maximum Charge Current for battery pack</td>
<td>4.5 A</td>
</tr>
<tr>
<td>Overvoltage Protection (OVP)</td>
<td>4.275 V</td>
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<tr>
<td>Overvoltage detection delay timer</td>
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<tr>
<td>Overvoltage Protection (OVP) release voltage</td>
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<tr>
<td>Undervoltage Protection (UVP)</td>
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<tr>
<td>Undervoltage detection delay timer</td>
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<tr>
<td>Undervoltage Protection (UVP) release voltage</td>
<td>3.1 V</td>
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<tr>
<td>Charge Overcurrent detection (OCC) voltage</td>
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<td>Discharge Overcurrent Detection (OCD) voltage</td>
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<td>Discharge Overcurrent Detection (OCD) delay timer</td>
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<td>Load Short Circuit Detection SCC) voltage, BAT to –V ≤ threshold</td>
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<tr>
<td>Load Short Circuit Detection (SCC) delay timer</td>
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<tr>
<td>Load Short Circuit release voltage, BAT to –V ≥ Threshold</td>
<td>1 V</td>
</tr>
</tbody>
</table>
11.2.2 Detailed Design Procedure

**NOTE**

The external FET selection is important to ensure the battery pack protection is sufficient and complies to the requirements of the system.

- **FET Selection:** Because the maximum desired discharge current is 7A, ensure that the Discharge Overcurrent circuit does not trigger until the discharge current is above this value.
- The total resistance tolerated across the two external FETs (CHG + DSG) should be 100 mV/7A = 14.3 mΩ.
- Based on the information of the total ON resistance of the two switches, determine what would be the Charge Overcurrent Detection threshold, 14.3 mΩ × 4.5A = 65 mV. Selecting a device with a 70-mV trigger threshold for Charge Overcurrent trigger is acceptable.
- The total Rds ON should factor in any worst-case parameter based on the FET ON resistance, de-rating due to temperature effects and minimum required operation, and the associated gate drive (Vgs). Therefore, the FET choice should meet the following criteria:
  - Vdss = 25 V
  - Each FET Rds ON = 7.5 mΩ at Tj = 25°C and Vgs = 3.5 V
  - Imax > 50 A to allow for short Circuit Current condition for 350 µs (max delay timer). The only limiting factor during this condition is Pack Voltage/(Cell Resistance + (2 × FET_RdsON) + Trace Resistance).
  - Use the CSD16406Q3 FET for the application.
  - An RC filter is required on the BAT for noise, and enables the device to operate during sharp negative transients. The 330-Ω resistor also limits the current during a reverse connection on the system.
  - It is recommended to place a high impedance 5-MΩ across the gate source of each external FET to deplete any charge on the gate-source capacitance.
11.2.3 Application Performance Plots

**Figure 26. UVP Recovery**

Orange Line (Channel 1) = Power Up Ramp on BAT Terminal
Turquoise Line (Channel 2) = DOUT Gate Drive Output
DOUT goes from low to high when UVP Recovery = UVP Set
Threshold +100 mV

**Figure 27. UVP Set Condition**

Orange Line (Channel 1) = Power Down Ramp on BAT Terminal
Turquoise Line (Channel 2) = DOUT Date Drive Output
DOUT goes from high to low when UVP threshold = UVP set
Threshold + set delay time

**Figure 28. Initial Power Up, DOUT**

Orange Line (Channel 1) = Power Up Ramp on BAT Terminal
Turquoise Line (Channel 2) = DOUT Gate Drive Output

**Figure 29. Initial Power Up, COUT**

Orange Line (Channel 1) = Power Up Ramp on BAT Terminal
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from high to low when OVP threshold = OVP set
Threshold + set delay time

**Figure 30. OVP Set Condition**

Orange Line (Channel 1) = Power Up Ramp on BAT Terminal
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from high to low when OVP threshold = OVP set
Threshold + set delay time

**Figure 31. OVP Recovery Condition**

Orange Line (Channel 1) = Decrease Voltage on BAT terminal
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from low to high when OVP Recovery = OVP Set
Threshold −100 mV
12 Power Supply Recommendations

The recommended power supply for this device is a maximum 8-V operation on the BAT input terminal.

13 Layout

13.1 Layout Guidelines

The following are the recommended layout guidelines:
1. Ensure the external power FETs are adequately compensated for heat dissipation with sufficient thermal heat spreader based on worst-case power delivery.
2. The connection between the two external power FETs should be very close to ensure there is not an additional drop for fault sensing.
3. The input RC filter on the BAT terminal should be close to the terminal of the IC.

13.2 Layout Example

\[ \text{Figure 32. bq297xy Board Layout} \]
14 Device and Documentation Support

14.1 Trademarks
All trademarks are the property of their respective owners.

14.2 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.3 Export Control Notice
Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

14.4 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms and definitions.

15 Mechanical, Packaging, and Orderable Information
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tbody>
<tr>
<td>BQ29700DSER</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSE</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
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<td>Samples</td>
</tr>
</tbody>
</table>

1. The marketing status values are defined as follows:
   - **ACTIVE**: Product device recommended for new designs.
   - **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE**: TI has discontinued the production of the device.

2. Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
   - **TBD**: The Pb-Free/Green conversion plan has not been defined.
   - **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
   - **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
   - **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

3. MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

5. Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

6. Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal*

<table>
<thead>
<tr>
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<th>Package Drawing</th>
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<th>SPQ</th>
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<th>B0 (mm)</th>
<th>K0 (mm)</th>
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Image 1: TAPE AND REEL INFORMATION

Image 2: TAPE DIMENSIONS

Image 3: REEL DIMENSIONS

Image 4: QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Image 5: PACKAGE MATERIALS INFORMATION

www.ti.com 8-Apr-2014
## TAPE AND REEL BOX DIMENSIONS

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<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. This package is lead-free.
DSE (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note E)

Solder Mask Opening
(Note C)

0.14x45'

0.85

0.05

All around

0.30

0.40

1.90

4x0,50

4x0,50

1.85

0.45

6x0,70

6x0,23

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note E)

Solder Mask Opening
(Note C)

0.75

0.12

0.05

0.28

All around

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.
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