CLC012 Adaptive Cable Equalizer for ITU-T G.703 Data Recovery

Check for Samples: CLC012

FEATURES

• Automatic Equalization of Coaxial and Twisted Pair Cables
• Loss of Signal Detect and Output Mute
• Output Eye Monitor
• Single Supply Operation: +5V or −5.2V
• Single-Ended or Differential Input
• Low Cost

APPLICATIONS

• ITU-T G.703 Serial Data Recovery
• Serial Digital Data Routing and Distribution
• Serial Digital Data Equalization and Reception
• Data Recovery Equalization: ATM, CAD Networks, Medical, Set Top Terminals, Industrial Video Networks

KEY SPECIFICATIONS

• Low Jitter: 180ps_{pp} @ 270 Mbps Through 200 Meters of Belden 8281 Coaxial Cable
• High Data Rates: < 50 Mbps to > 650 Mbps
• Excellent Input Return Loss: 19 dB @ 270 MHz
• Low Supply Current: 68 mA
• Equalizes up to 300+ Meters of Belden 8281 or 120 Meters of Cat 5 UTP Cable

DESCRIPTION

TJ's CLC012 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The CLC012 simplifies the task of high-speed data recovery with a one-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40 dB at 200 MHz. This corresponds to 300 meters of Belden 8281 or 120 meters of Category 5 UTP (unshielded twisted pair).

The CLC012 provides superior jitter performance: 180ps_{pp} for 270 Mbps data that has passed through 200 meters of Belden 8281 cable. This exceptional performance provides wide error margin in digital data links. The equalizer operates on a single supply with a power consumption of only 290 mW. The small 14-pin SOIC package allows for high-density placement of components for multi-channel applications such as routers. The equalizer operates over a wide range of data rates from less than 50 Mbps to rates in excess of 650 Mbps.

The equalizer is flexible in allowing either single-ended or differential input drive. Its high common mode rejection provides excellent immunity to interference from noise sources. On-chip quantized feedback eliminates baseline wander.

Additional features include a Loss of Signal output and an output mute pin which, when tied together, mute the output when no signal is present. A buffered eye monitor output is provided, for viewing the equalized signal prior to the comparator. Differential AEC pins allow the user to set the internal adaptive loop time constant with one external capacitor.
Typical Application

Connection Diagram

Before Equalization: 622Mbps 200m of Belden 8281 Coaxial Cable

After Equalization: 622Mbps 200m of Belden 8281 Coaxial Cable

Figure 1. Pinout 14-Pin SOIC (D)
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ($V_{CC} - V_{EE}$)</td>
<td>$-0.3V, +6.5V$</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$+150°C$</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65°C$ to $+150°C$</td>
</tr>
<tr>
<td>Lead Temperature (Soldering 4 sec.)</td>
<td>$+260°C$</td>
</tr>
<tr>
<td>ESD Rating (Soldering 4 sec.)</td>
<td>$\geq 500V$</td>
</tr>
<tr>
<td>$\theta_JA$ 14-Pin SOIC (AJE)</td>
<td>$95°C/W$</td>
</tr>
<tr>
<td>MTTF (based on limited life test data)</td>
<td>$4.8 \times 10^7$ hours</td>
</tr>
</tbody>
</table>

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Human body model, 1.5 kΩ in series with 100 pF; based on limited test data.

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ($V_{CC} - V_{EE}$)</td>
<td>4.5V to 5.5V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$-40°C$ to $+85°C$</td>
</tr>
<tr>
<td>Series Input Resistance (In Series w/DI &amp; DI)</td>
<td>100Ω</td>
</tr>
<tr>
<td>Input Coupling Capacitance</td>
<td>$1.0 \mu F$</td>
</tr>
<tr>
<td>AEC Capacitor (Connected between AEC+ &amp; AEC−)</td>
<td>50 pF to 1 μF</td>
</tr>
<tr>
<td>Cable Input Voltage Swing (1)</td>
<td>720 to 880 mVpp</td>
</tr>
<tr>
<td>DO/DO Minimum Voltage (2)</td>
<td>$V_{CC} - 1.6V$</td>
</tr>
</tbody>
</table>

(1) These specifications assume an 800 mVpp signal at the cable input. Levels above and below 800 mV are allowable, but performance may vary. The cable will attenuate the signal prior to entering the equalizer.

(2) To maintain specified performance, do not reduce DO/DO below this level.
## Electrical Characteristics

\(V_{CC} = +5V, \ V_{EE} = 0V, \ \text{signal source swing} = 0.8 \ \text{Vpp}^{(1)}, \ C_{AEC} = 100 \ \text{pF}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>(+25^\circ C)</th>
<th>(+25^\circ C)</th>
<th>(+85^\circ C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Residual Jitter</td>
<td>10 meters Belden 8281</td>
<td>311 Mbps PRN(^{(3)})</td>
<td>150</td>
<td>250</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td>300 meters Belden 8281</td>
<td>311 Mbps PRN(^{(3,4)})</td>
<td>350</td>
<td>500</td>
<td>750</td>
</tr>
<tr>
<td>Equalization Time Constant</td>
<td>100 meters Belden 8281</td>
<td>(C_{AEC} = 100 \ \text{pF}^{(5)})</td>
<td>1.5</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>200 meters Belden 8281</td>
<td>(C_{AEC} = 100 \ \text{pF}^{(5)})</td>
<td>2.0</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>300 meters Belden 8281</td>
<td>(C_{AEC} = 100 \ \text{pF}^{(5)})</td>
<td>3.2</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>output rise and fall time (20%–80%)</td>
<td>(R_{\text{collector}} = 75\Omega)</td>
<td></td>
<td>750</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>output duty cycle distortion</td>
<td></td>
<td></td>
<td>30</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>minimum average transition density</td>
<td></td>
<td></td>
<td>1/50</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>maximum average data rate</td>
<td>150m Belden 8281(^{(6)})</td>
<td></td>
<td>650</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td><strong>(V_{CC}) Jitter Sensitivity</strong></td>
<td>27 MHz</td>
<td></td>
<td>0.85</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>270 MHz</td>
<td></td>
<td>1.90</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td><strong>(V_{EE}) Jitter Sensitivity</strong></td>
<td>27 MHz</td>
<td></td>
<td>0.55</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>270 MHz</td>
<td></td>
<td>1.45</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td><strong>STATIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current (Includes Output Current)</td>
<td>(V_{AEC} = 0V)</td>
<td>See(^{(4)})</td>
<td>68</td>
<td>48/75</td>
<td>40/80</td>
</tr>
<tr>
<td></td>
<td>(V_{AEC} = 0.4V)</td>
<td>See(^{(4)})</td>
<td>53</td>
<td>43/64</td>
<td>37/70</td>
</tr>
<tr>
<td>Input and Output Parameters</td>
<td>(DO/DO) output current</td>
<td></td>
<td>10</td>
<td>8.7/11.3</td>
<td>8.0/12</td>
</tr>
<tr>
<td></td>
<td>(DO/DO) output voltage swing</td>
<td>(R_{\text{collector}} = 75\Omega^{(4)})</td>
<td>750</td>
<td>650/850</td>
<td>600/900</td>
</tr>
<tr>
<td></td>
<td>(DI/DO) common mode voltage</td>
<td></td>
<td>3.4</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>AEC differential voltage</td>
<td>Belden 8281</td>
<td>1.5</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>(AE_{C}/AE_{C}−) common mode</td>
<td></td>
<td>3.6</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>output eye monitor (OEM) bias potential</td>
<td></td>
<td>3.2</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>Loss of Signal (LOS) current output-HIGH</td>
<td>(V_{OH} = 4.5V)</td>
<td>(-400)</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>Loss of Signal (LOS) current output-LOW</td>
<td>(V_{OL} = 0.5V)</td>
<td>600</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>(MUTE) voltage input-HIGH</td>
<td>See(^{(4)})</td>
<td>1.8</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>(MUTE) voltage input-LOW</td>
<td>See(^{(4)})</td>
<td>1.2</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>(MUTE) current input-HIGH</td>
<td>(V_{IH} = 5V^{(4)})</td>
<td>5.0</td>
<td>(\pm100)</td>
<td>(\pm500)</td>
</tr>
<tr>
<td></td>
<td>(MUTE) current input-LOW</td>
<td>(V_{IL} = 0V^{(4)})</td>
<td>0.2</td>
<td>(\pm100)</td>
<td>(\pm500)</td>
</tr>
</tbody>
</table>

\(^{(1)}\) These specifications assume an 800 mVpp signal at the cable input. Levels above and below 800 mV are allowable, but performance may vary. The cable will attenuate the signal prior to entering the equalizer.

\(^{(2)}\) Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

\(^{(3)}\) Peak-to-peak jitter is defined as 6 times the rms jitter.

\(^{(4)}\) J-level: spec. is 100% tested at +25°C.

\(^{(5)}\) For more information, see Operation and Design Guidelines.

\(^{(6)}\) 50% eye opening.
## Electrical Characteristics (continued)

\((V_{CC} = +5V, V_{EE} = 0V, \text{ signal source swing} = 0.8 \, V_{pp}^{(1)}, C_{AEC} = 100 \, \text{pF})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min/Max</th>
<th>Min/Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>@ +25°C</td>
<td>@ +85°C</td>
<td></td>
</tr>
<tr>
<td><strong>TIMING PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LOS Response Time</td>
<td>carrier applied</td>
<td>See (^{(7)})</td>
<td>150</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>carrier removed</td>
<td>See (^{(8)})</td>
<td>150</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>MUTE response time</td>
<td>See (^{(9)})</td>
<td>2.0</td>
<td>_</td>
</tr>
<tr>
<td><strong>MISCELLANEOUS PERFORMANCE</strong></td>
<td>input resistance</td>
<td>single-ended</td>
<td>7.3</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>input capacitance</td>
<td>single-ended (^{(10)})</td>
<td>1.0</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>input return loss @ 270 MHz</td>
<td>(Z_0 = 75Ω (^{(11)})</td>
<td>19</td>
<td>_</td>
</tr>
<tr>
<td></td>
<td>maximum cable attenuation</td>
<td>200 MHz (^{(12)})</td>
<td>40</td>
<td>_</td>
</tr>
</tbody>
</table>

\(^{(7)}\) Time from application of a valid signal to when the LOS output asserts high.

\(^{(8)}\) Time from the removal of a valid signal to when the LOS output asserts low.

\(^{(9)}\) Time from assertion of MUTE to when the output responds.

\(^{(10)}\) Device only. Does not include typical pc board parasitics.

\(^{(11)}\) Includes typical pc board parasitics.

\(^{(12)}\) This sets the maximum cable length for the equalizer.
Typical Performance Characteristics

Before Equalization: 155Mbps
50m of Belden 8281 Coaxial Cable

After Equalization: 155Mbps
50m of Belden 8281 Coaxial Cable

Before Equalization: 155Mbps
100m of Belden 8281 Coaxial Cable

After Equalization: 155Mbps
100m of Belden 8281 Coaxial Cable

Before Equalization: 155Mbps
200m of Belden 8281 Coaxial Cable

After Equalization: 155Mbps
200m of Belden 8281 Coaxial Cable

Figure 2.

Figure 3.

Figure 4.

Figure 5.

Figure 6.

Figure 7.
Typical Performance Characteristics (continued)

Before Equalization: 155Mbps
300m of Belden 8281 Coaxial Cable

After Equalization: 155Mbps
300m of Belden 8281 Coaxial Cable

Before Equalization: 622Mbps
50m of Belden 8281 Coaxial Cable

After Equalization: 622Mbps
50m of Belden 8281 Coaxial Cable

Before Equalization: 622Mbps
100m of Belden 8281 Coaxial Cable

After Equalization: 622Mbps
100m of Belden 8281 Coaxial Cable
Typical Performance Characteristics (continued)

Before Equalization: 622Mbps
200m of Belden 8281 Coaxial Cable

After Equalization: 622Mbps
200m of Belden 8281 Coaxial Cable

Maximum Data Rate* vs. Cable Length (Typical)

"*Max data rate for 50% eye opening. Eye boundary defined as point where BER = 1 x 10^-9."

Jitter vs. Cable Length

Return Loss

CLC012 LOS Response
<table>
<thead>
<tr>
<th>Name</th>
<th>Pin #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DI, DI</td>
<td>8, 9</td>
<td>Differential data inputs.</td>
</tr>
<tr>
<td>DO, DO</td>
<td>13, 14</td>
<td>Differential collector data outputs (ECL compatible).</td>
</tr>
<tr>
<td>AEC+, AEC−</td>
<td>6, 7</td>
<td>AEC loop filter pins. &lt;br&gt;A capacitor connected between these pins governs the loop response for the adaptive equalization loop.</td>
</tr>
<tr>
<td>OEM</td>
<td>3</td>
<td>Eye monitor output. The output of the equalization filter.</td>
</tr>
<tr>
<td>LOS</td>
<td>5</td>
<td>Loss of Signal. (Low when no signal is present).</td>
</tr>
<tr>
<td>MUTE</td>
<td>12</td>
<td>Output MUTE. (Active low.) &lt;br&gt;Loss of Signal (LOS) may be tied to this pin to inhibit the output when no signal is present.</td>
</tr>
<tr>
<td>VCC</td>
<td>1, 2, 4</td>
<td>Positive supply pins (ground or +5V).</td>
</tr>
<tr>
<td>VEE</td>
<td>10, 11</td>
<td>Negative supply pins (−5.2V or ground).</td>
</tr>
</tbody>
</table>

**Operation**

The CLC012 Adaptive Cable Equalizer provides a complete solution for equalizing high-bit-rate digital data transmitted over long transmission lines. The following sections furnish design and application information to assist in completing a successful design:

- Block diagram explanation of the CLC012
- Recommended standard input and output interface connections
- Common applications for the CLC012
- Measurement, PC layout, and cable emulation boxes

For applications assistance in the U.S., go to the WEBENCH® Design Center Team’s website at www.ti.com/ww/en/analog/webench/.

![Figure 20. CLC012 Equalizer Application Circuit](image-url)
BLOCK DESCRIPTION

The CLC012 is an adaptive equalizer that reconstructs serial digital data received from transmission lines such as coaxial cable or twisted pair. Its transfer function approximates the reciprocal of the cable loss characteristic. The block diagram in Figure 21 depicts the main signal conditioning blocks for equalizing digital data at the receiving end of a cable. The CLC012 receives baseband differential or single-ended digital signals at its inputs DI and DI.

The **Equalizer** block is a two-stage adaptive filter. This filter is capable of equalizing cable lengths from zero meters to lengths that require 40 dB of boost at 200 MHz.

The **Quantized Feedback Comparator** block receives the differential signals from the equalizer filter block. This block includes two comparators. The first comparator incorporates a self-biasing DC restore circuit. This is followed by a second high-speed comparator with output mute capability. The second comparator receives and slices the DC-restored data. Its outputs DO and DO are taken from the collectors of the output transistors. MUTE latches DO and DO when a TTL logic low level is applied.

The **Adaptive Servo Control** block produces the signal for controlling the filter block, and outputs a voltage proportional to cable length. It receives differential signals from the output of the filter block and from the quantized-feedback comparator (QFBC) to develop the control signal. The servo loop response is controlled by an external capacitor placed across the AEC+ and AEC− pins. Its output voltage, as measured differentially across AEC+ and AEC−, is roughly proportional to the length of the transmission line. For Belden 8281 coaxial cable this differential voltage is about 1.5 mV/meter. Once this voltage exceeds 500 mV, no additional equalization is provided.

The **Loss of Signal (LOS)** block monitors the signal power out of the equalizing filter and compares it to an internal reference to determine if a valid signal is present. A CMOS high output indicates that data is present. The output of LOS can be connected to the MUTE input to automatically latch the outputs (DO and DO), preventing random transitions when no data is present.

The **Output Eye Monitor (OEM)** provides a single-ended buffered output for observing the equalized eye pattern. The OEM output is a low impedance high-speed voltage driver capable of driving an AC-coupled 100Ω load.

![Figure 21. CLC012 Block Diagram](image)
**DEVICE TESTING**

Performance or compliancy testing of the CLC012 with **Cable Clones** is not allowed. Use of these devices is contrary to the product's specifications and test procedures. Testing for product specifications or performance using cable clones is invalid since cable clones have a different frequency response than the actual cable. Testing with full length cable samples is recommended.

**Input Interfacing**

The CLC012 accepts either differential or single-ended input voltage specified in **Static Performance** section of the **Electrical Characteristics** table. The following sections show several suggestions for interfaces for the inputs and outputs of the CLC012.

**SINGLE-ENDED INPUT INTERFACE: 75Ω Coaxial Cable**

The input is connected single-ended to either DI or DI as shown in **Figure 22**. Balancing unused inputs helps to lessen the effects of noise. Use the equivalent termination of 37.4Ω to balance the input impedance seen by each pin. It also helps to terminate grounds at a common point. Resistors $R_x$ and $R_y$ are recommended for optimum performance. The equalizer inputs are self-biasing. Signals should be AC coupled to the inputs as shown in **Figure 22**.

![Figure 22. Single-Ended 75Ω Cable Input Interface](image)

**DIFFERENTIAL INPUT INTERFACE: Twisted Pair**

A recommended differential input interface is shown in **Figure 23**. Proper voltage levels must be furnished to the input pins and the proper cable terminating impedance must be provided. For Category 5 UTP this is approximately 100Ω. **Figure 23** shows a generalized network which may be used to receive data over a twisted pair. Resistors $R_1$ and $R_2$ provide the proper terminating impedance and signal level adjustment. The blocking capacitors provide AC coupling of the attenuated signal levels. The plots in the **Typical Performance Characteristics** section demonstrate various equalized data rates using Category 5 UTP at 100 meter lengths. A full schematic of a recommended driver and receiver circuit for 100Ω Category 5 UTP is provided in the **Typical Applications** section with further explanation.

![Figure 23. Twisted Pair Input Interface](image)
Output Interfacing

The outputs $DO$ and $DO$ produce ECL logic levels when the recommended output termination networks are used. The $DO$ and $DO$ pins are not complementary emitter coupled logic outputs. Instead, the outputs are taken off of the collectors of the transistors. Therefore, care must be taken to meet the interface threshold levels required by ECL families. Recommended interfaces for standard ECL families are shown in the following circuits.

DIFFERENTIAL LOAD-TERMINATED OUTPUT INTERFACE

Figure 24 shows a recommended circuit for implementing a differential output that is terminated at the load. A diode or $75\Omega$ resistor provides a voltage drop from the positive supply ($+5V$ for PECL or Ground for ECL operation) to establish proper ECL levels. The resistors terminate the cable to the characteristic impedance. The output voltage swing is determined by the CLC012 output current ($10\ mA$) times the termination resistor. For the circuit in Figure 24, the nominal output voltage swing is $750\ mV$.

![Figure 24. Differential Load Terminated Output Interface](https://www.ti.com/lit/ds/symlink/clc012.pdf?ts=1697734803670&es=23)

DIFFERENTIAL SOURCE-TERMINATED OUTPUT INTERFACE

Figure 25 is similar to Figure 24 except that the termination is provided at the source. This configuration may also be used for single-ended applications. However, the unused output must still be terminated as shown.

![Figure 25. Differential Source Terminated Output Interface](https://www.ti.com/lit/ds/symlink/clc012.pdf?ts=1697734803670&es=23)
Terminating Physically Separated Outputs

When the two outputs must be routed to physically separate locations, the circuit in Figure 25 may be applied. Alternatively, if load termination is desired, the circuit in Figure 26 may be used. The resistive divider network provides 75Ω termination and establishes proper ECL levels. This circuit consumes slightly more power than the previous circuits.

![Figure 25](image1)

**Design Guidelines**

**Selecting the Automatic Equalizer Capacitor**

The AEC capacitor sets the loop time constant \( \tau \) for the equalizer’s adaptive loop response time. The following formula is used to set the loop time constant:

\[
\tau = R \cdot C_{AEC} \cdot 10^{-6}
\]  

(1)

R is a conversion factor that is set by internal equalizer parameters and cable length. For Belden 8281 coaxial cable, the R values are (\( \tau = \mu s \), \( C_{AEC} \) in pF):

<table>
<thead>
<tr>
<th>Cable Length</th>
<th>R Value (Ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 meters</td>
<td>15000</td>
</tr>
<tr>
<td>200 meters</td>
<td>20000</td>
</tr>
<tr>
<td>300 meters</td>
<td>32000</td>
</tr>
</tbody>
</table>

For example, a \( C_{AEC} \) value of 100 pF results in an adaptive loop time constant of 2 \( \mu s \) at 200 meters of cable.

**Connection and Operation of LOS and MUTE**

**Loss of Signal (LOS)** is a CMOS output that indicates the presence of equalized data from the filter. This LOS output can be connected to MUTE to suspend changes in the data outputs DO and DO, if no valid signal exists. This simple configuration prevents random output transitions due to noise. For sparse transition patterns it is recommended that a capacitor be connected to LOS as shown in Figure 20.

Add a capacitor to pin 5 to slow the response time of Loss of Signal when LOS is connected to MUTE. The capacitor reduces sensitivity to pathological patterns. Pathological patterns are defined as sparse data sequences with few transitions.

**Output Eye Monitor OEM Connections**

The OEM is a high-speed, buffered output for monitoring the equalized eye pattern prior to the output comparator. Its output is designed to drive an AC-coupled 50Ω coaxial cable with a series 50Ω backmatch resistor. The cable should be terminated with 50Ω at the oscilloscope. Figure 20 shows a schematic with a typical connection.
MINIMUM DATA TRANSITIONS
The CLC012 specifies a minimum transition rate. For the CLC012 this sets the minimum data rate for transmitting data through any cable medium. The CLC012 minimum average transition density is found in the Electrical Characteristics section of the datasheet.

POWER SUPPLY OPERATION AND THERMAL CONSIDERATIONS
The CLC012 operates from either +5V or −5.2V single supplies. Refer to Figure 20 when operating the part from +5V. When operating with a −5.2V supply, the VEE pins should be bypassed to ground. The evaluation board and associated literature provide for operation from either supply.

Maximum power dissipation occurs at minimum cable length. Under that condition, ICC = 58 mA.

Total power dissipated:
\[ P_T = (58 \text{ mA})(5\text{V}) = 290 \text{ mW} \]  \hspace{1cm} (2)

Power in the load:
\[ P_L = (0.7\text{V})(11 \text{ mA}) + (37.5)(11 \text{ mA})^2 = 12 \text{ mW} \]  \hspace{1cm} (3)

Maximum power dissipated on the die:
\[ P_{DMAX} = P_T - P_L = 278 \text{ mW} \]  \hspace{1cm} (4)

Junction Temperature =
\[ (\theta_{JA})(278 \text{ mW}) + T_A = T_A + 26^\circ\text{C} \]  \hspace{1cm} (5)

Layout and Measurement
The printed circuit board layout for the CLC012 requires proper high-speed layout to achieve the performance specifications found in the datasheet. The following list contains a few rules to follow:
1. Use a ground plane.
2. Decouple power pins with 0.1 \( \mu \text{F} \) capacitors placed ≤ 0.1" (3mm) from the power pins.
3. Design transmission strip lines from the CLC012’s input and output pins to the board connectors.
4. Route outputs away from inputs.
5. Keep ground plane ≥ 0.025” (0.06mm) away from the input and output pads.

Figure 27 shows a block level measurement diagram, while Figure 34 depicts a detailed schematic. A pseudo-random pattern generator with low output jitter was used to provide a NRZI pattern to create the eye diagrams shown in the Typical Performance Characteristics section.

Since most pattern generators have a 50\( \Omega \) output impedance, a translation can be accomplished using a CLC005 Cable Driver as an impedance transformer. A wide bandwidth oscilloscope is needed to observe the high data rate eye pattern. When monitoring a single output that is terminated at both the equalizer output and the oscilloscope, the effective output load is 37.4\( \Omega \). Consequently, the signal swing is half that observed for a single-ended 75\( \Omega \) termination.

![Figure 27. Typical Measurement Block](image-url)
Troubleshooting with scope probes can affect the equalization. For high data rates, use a low capacitance probe with less than 2 pF probe capacitance. Evaluation boards and literature are available for quick prototyping and evaluation of the CLC012 Adaptive Cable Equalizer. The CLC012 contains CMOS devices and operators should use grounding straps when handling the parts.

*Figure 28* shows the CLC012’s internal power supply routing. Bypass \( V_{CC} \) (pin 4) by:
- Monolithic capacitor of about 0.1 \( \mu \)F placed less than 0.1” (3mm) from the pin
- Tantalum capacitor of about 6.8 \( \mu \)F for large current signal swings placed as close as convenient to the CLC012

![Figure 28. Power Package Routing Fixture](image)

To minimize ringing at the CLC012’s inputs, place a 100\( \Omega \) resistor in series with the input. This resistor reduces inductance effects.

Several layout techniques can improve high speed performance:
- Keep input, output and AEC traces well separated
- Use balanced input termination’s
- Avoid routing traces close to the CLC012’s input trace
- Maintain common return points for components
- Use guard traces

The input lines of the CLC012 use a 1000\( \Omega \) series resistors at the input pins. This decreases the inductive effects internal to the part to reduce ringing on fast rise and fall times. Refer to the Evaluation Board layout for further suggestions on layout for the CLC012 Adaptive Equalizer.
EQUALIZATION CURVE

The CLC012 Adaptive Cable Equalizer has a maximum equalization response as shown in Figure 29. This response may be obtained by forcing >0.5V differentially at the AEC pins.

![Figure 29. Maximum Equalization Response](image)

CABLE EMULATION BOXES

Some cable emulation boxes will not mimic cables correctly. When evaluating the CLC012, it is strongly recommended that actual cable be used to determine the various performance parameters.

Typical Applications

COAXIAL CABLE RECEIVER

The CLC012 equalizer application shown in Typical Application will equalize a variety of coaxial cables up to lengths that attenuate the signal by 40 dB at 200 MHz. The application shows the proper connection for a single cable driven with a CLC005 driver. Loss of Signal (LOS) is connected to MUTE to latch outputs DO and DO in the absence of an input signal to the equalizer.

Refer to the CLC012's Evaluation Board layout for additional suggestions.

TI can supply most of the major components required to design a transmission line repeater. Figure 30 shows a typical repeater design using the CLC005, CLC012, and the CLC016. The design functions supported by each chip are:

CLC005: Cable connection chip
- Boosts drive for transmission to next repeater or final destinations

CLC012: Receive serialized digital data from incoming transmission lines
- Equalizes the incoming data

CLC016: Retimes the equalized data (improving jitter)

The CLC016 is a multi-rate data retiming PLL. The circuit (Figure 30) will work at up to 4 different data rates with no additional components or manual tuning.
DIGITAL VIDEO (SDV) ROUTERS

The CLC012 provides performance that complies with the ITU-T G.703 standard for serial digital data transmission over coaxial cable. One common application is in routers, which provide a switching matrix for connecting source equipment to destination equipment.

Figure 31 shows a typical configuration for a router, including equalizers, a crosspoint switch, data retimers, and cable drivers. The CLC012 is used in its standard configuration in this application, and automatically equalizes cable lengths from zero meters to greater than 300 meters at 360 MHz (see plots in Typical Performance Characteristics section). The equalized outputs are connected to the differential inputs of the crosspoint switch. The CLC016 Data Retimer receives the data from the crosspoint and performs the clock and data recovery functions, further reducing jitter. Finally, the retimed data is driven into the coaxial cable by a CLC005 ITU-T G.703 Cable Driver (with two amplitude-adjustable outputs).
TWISTED PAIR DRIVER

A low-cost medium for transmitting data is twisted pair. Category 5 UTP has an attenuation characteristic similar to Belden 8281 coaxial cable but scaled in length: 120 meters of Category 5 UTP is roughly equivalent to 300 meters of Belden 8281 cable. When properly implemented, the CLC012 will equalize data rates up to 625 Mbps over Category 5 UTP. The maximum data rate depends upon the cable length. A plot of Maximum Data Rate vs Cable Length is found in the Typical Performance Characteristics section for Belden 8281, and can be scaled as stated above to estimate maximum cable lengths and data rates for UTP.

Category 5 UTP has a characteristic impedance of approximately 100Ω. The CLC005 in Figure 32 is used to drive the twisted pair AC-coupled with a series 0.1 μF capacitor and a 50Ω resistor in each differential output. The CLC012 Adaptive Equalizer requires 800 mVpp from the transmit side of the cable. A voltage divider is necessary to scale the voltage to the required level at the input of the CLC012. This resistor network also provides the correct impedance match for twisted pair.

For Category 5 UTP, the approximate AEC voltage per length is 3.75 mV/m (see BLOCK DESCRIPTION). The CLC005 provides a trim adjust for fine tuning the output signal with the resistor R. Refer to the CLC005 datasheet for tuning directions.

![Figure 32. Twisted Pair Equalization](image)

![Figure 33. Before and After Equalization at 622 Mbps Through 50 Meters of Category 5 UTP](image)
Evaluation Board

Evaluation boards are available for a nominal charge that demonstrate the basic operation of the SDI/SDV/SDH devices. The evaluation boards can be ordered through TI's Distributors. Supplies are limited, please check for current availability.

The SD012EVK evaluation kit for the CLC012, Adaptive Cable Equalizer for ITU-T G.703 Data Recovery, provides an operating environment in which the cable equalizer can be evaluated by system / hardware designers. The evaluation board has all the needed circuitry and connectors for easy connection and checkout of the device circuit options as discussed in the CLC012 datasheet. A schematic, parts list and pictorial drawing are provided with the board.

From the WWW, the following information may be viewed / downloaded for most evaluation boards: www.ti.com
- Device Datasheet and / or EVK User Manual
- View a picture of the EVK
- View the EVK Schematic
- View the top assembly drawing and BOM
- View the bottom assembly drawing and BOM

PCB LAYOUT

The CLC012 requires proper high-speed layout techniques to obtain best results. A few recommended layout rules to follow for best results when using the CLC012 Adaptive Cable Equalizer are:
1. Use a ground plane.
2. Decouple power pins with 0.01 μF capacitors placed ≤ 0.1” (3mm) from the power pins.
3. Design transmission lines to the inputs and outputs.
4. Route outputs away from inputs.
5. Remove ground plane ≥ 0.025” (0.06mm) from the input and output pads.
## REVISION HISTORY

**Changes from Revision D (April 2013) to Revision E**

<table>
<thead>
<tr>
<th>Changes from Revision D (April 2013) to Revision E</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>19</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| Audio       | www.ti.com/audio |
| Amplifiers  | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP         | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface   | interface.ti.com |
| Logic       | logic.ti.com |
| Power Mgmt  | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID        | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom    | www.ti.com/communications |
| Computers and Peripherals     | www.ti.com/computers |
| Consumer Electronics          | www.ti.com/consumer-apps |
| Energy and Lighting           | www.ti.com/energy |
| Industrial                    | www.ti.com/industrial |
| Medical                      | www.ti.com/medical |
| Security                     | www.ti.com/security |
| Space, Avionics and Defense   | www.ti.com/space-avionics-defense |
| Video and Imaging             | www.ti.com/video |
| TI E2E Community              | e2e.ti.com |
| TI E2E Community              | e2e.ti.com |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated