LME49810 200V Audio Power Amplifier Driver with Baker Clamp

Check for Samples: LME49810

FEATURES

- **Very High Voltage Operation**
- **Output Clamp Logic Output**
- **Thermal Shutdown and Mute**
- **Customizable External Compensation**
- **Scalable Output Power**

APPLICATIONS

- **Guitar Amplifiers**
- **Powered Studio Monitors**
- **Powered Subwoofers**
- **Pro Audio**
- **Audio Video Receivers**
- **High Voltage Industrial Applications**

KEY SPECIFICATIONS

- **Wide operating voltage range: ±20V to ±100V**
- **Slew Rate: 50V/µs (Typ)**
- **Output Drive Current: 60mA (Typ)**
- **PSRR (f = DC): 110dB (Typ)**
- **THD+N (f = 1kHz): 0.0007 (Typ)**

DESCRIPTION

The LME49810 is a high fidelity audio power amplifier driver designed for demanding consumer and pro-audio applications. Amplifier output power may be scaled by changing the supply voltage and number of power transistors. The LME49810's minimum output current is 50mA. When using a discrete output stage the LME49810 is capable of delivering in excess of 300 watts into a single-ended 8Ω load.

Unique to the LME49810 is an internal Baker Clamp. This clamp insures that the amplifier output does not saturate when over driven. The resultant "soft clipping" of high level audio signals suppresses undesirable audio artifacts generated when conventional solid state amplifiers are driven hard into clipping.

The LME49810 includes thermal shutdown circuitry that activates when the die temperature exceeds 150°C. The LME49810's mute function, when activated, mutes the input drive signal and forces the amplifier output to a quiescent state.

Typical Application

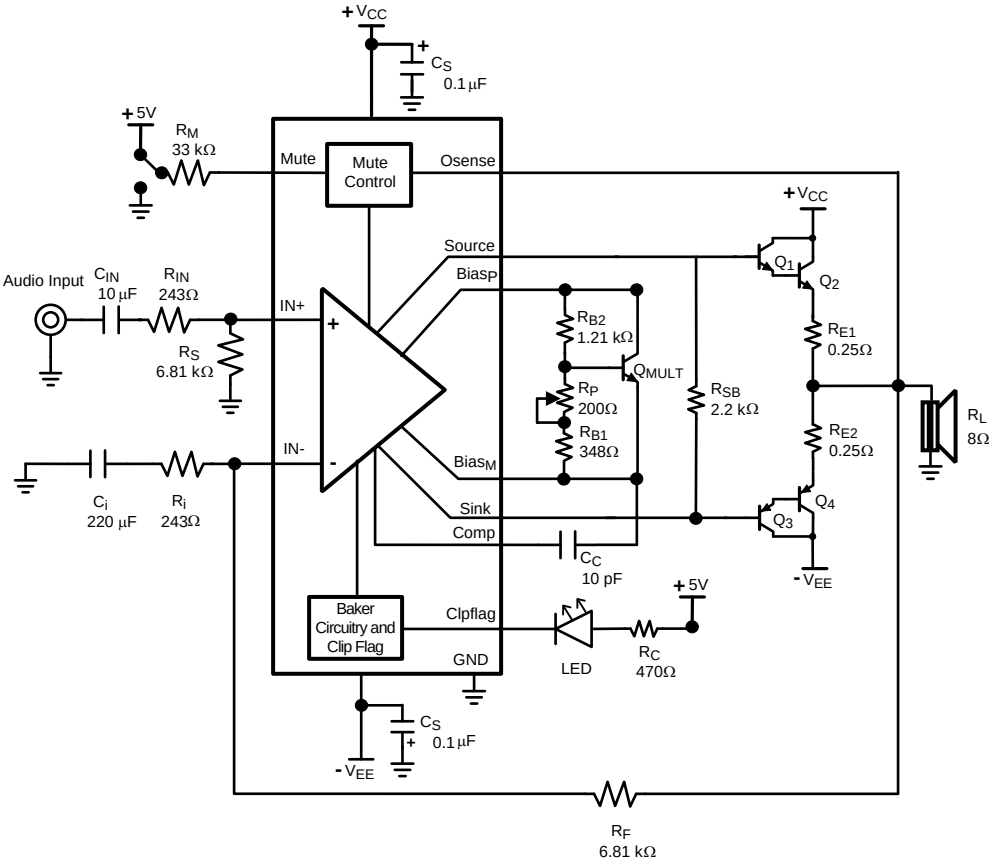


Figure 1. LME49810 Audio Amplifier Schematic

Connection Diagram

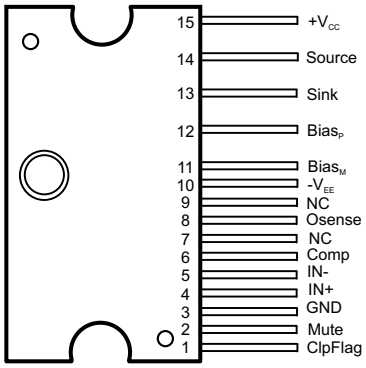


Figure 2. 15-Pin PFM (Top View)
See NDN0015A Package

PIN DESCRIPTIONS

Pin	Pin Name	Description
1	ClpFlag	Baker Clamp Clip Flag Output
2	Mute	Mute Control
3	GND	Device Ground
4	IN+	Non-Inverting Input
5	IN–	Inverting Input
6	Comp	External Compensation Connection
7	NC	No Connect, Pin electrically isolated
8	Osense	Output Sense
9	NC	No Connect, Pin electrically isolated
10	$-V_{EE}$	Negative Power Supply
11	$Bias_M$	Negative External Bias Control
12	$Bias_P$	Positive External Bias Control
13	Sink	Output Sink
14	Source	Output Source
15	$+V_{CC}$	Positive Power Supply

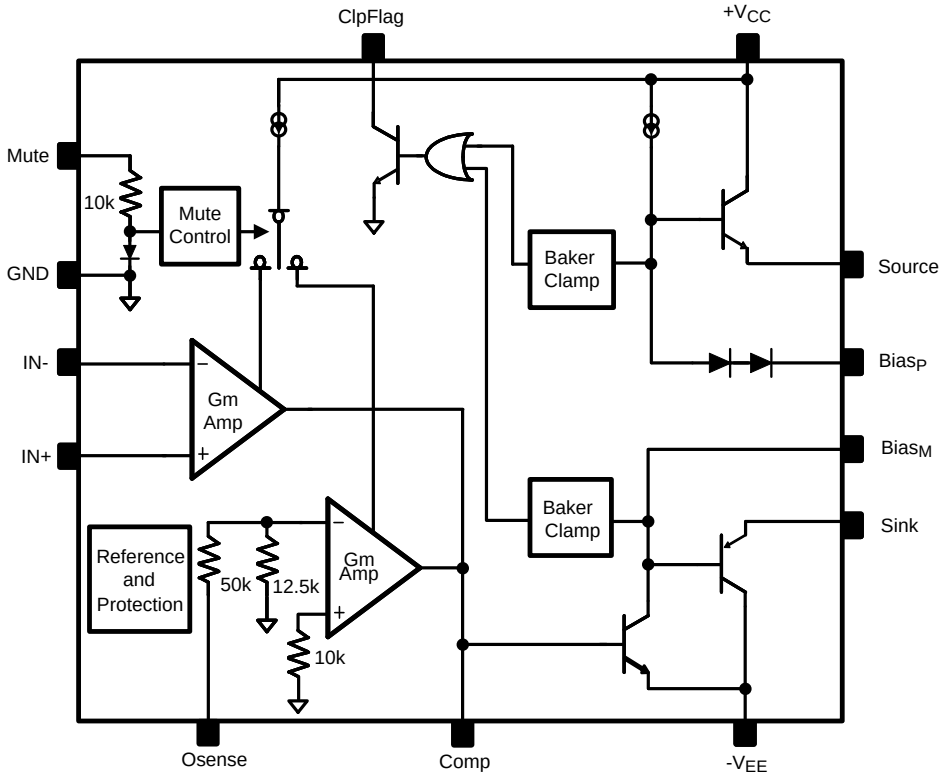


Figure 3. LME49810 Simplified Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage $\|V^+\| + \|V^-\|$		200V
Differential Input Voltage		±6V
Common Mode Input Range		$0.4V_{EE}$ to $0.4V_{CC}$
Power Dissipation(4)		4W
ESD Susceptibility(5)		1kV
ESD Susceptibility(6)		200V
Junction Temperature (T_{JMAX})(7)		150°C
Soldering Information	PFM Package (10 seconds)	260°C
Storage Temperature		–40°C to +150°C
Thermal Resistance	θ_{JA}	73°C/W
	θ_{JC}	4°C/W

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JC}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JC}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LME49810, T_{JMAX} = 150°C and the typical θ_{JC} is 4°C/W.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model, 220pF - 240pF discharged through all pins.
(7) The maximum operating junction temperature is 150°C.

OPERATING RATINGS

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +8\ 5°C$
Supply Voltage		$\pm20V \le V_{SUPPLY} \le \pm100V$

ELECTRICAL CHARACTERISTICS V_{CC} = +100V, V_{EE} = –100V(1)(2)

The following specifications apply for I_{MUTE} = 100µA, unless otherwise specified. Limits apply for T_A = 25°C, C_C = 10pF, and A_V = 29dB.

Symbol	Parameter	Conditions	LME49810		Units (Limits)
			Typical(3)	Limits(4)(5)	
I_{CC}	Quiescent Power Supply Current	V_{CM} = 0V, V_O = 0V, I_O = 0A	11	18	mA (max)
I_{EE}	Quiescent Power Supply Current	V_{CM} = 0V, V_O = 0V, I_O = 0A	13		mA (max)
THD+N	Total Harmonic Distortion + Noise	No Load, BW = 30kHz, V_{OUT} = $30V_{RMS}$, f = 1kHz	0.0007		% (max)
A_V	Open Loop Gain	f = DC f = 1kHz, V_{IN} = $1mV_{RMS}$	120 88		dB dB
V_{OM}	Output Voltage Swing	THD+N = 0.05%, f = 1kHz	67.5		V_{RMS}
V_{NOISE}	Output Noise	BW = 30kHz, A-weighted	50 34	 150	µV µV (max)
I_{OUT}	Output Current	Current from Source to Sink Pins	60	50	mA (min)
I_{MUTE}	Current into Mute Pin	To activate the amplifier	100	50 200	µA (min) µA (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at +25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Data sheet min and max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS V_{CC} = +100V, V_{EE} = –100V[1][2] (continued)

The following specifications apply for I_{MUTE} = 100µA, unless otherwise specified. Limits apply for T_A = 25°C, C_C = 10pF, and A_V = 29dB.

Symbol	Parameter	Conditions	LME49810		Units (Limits)
			Typical[3]	Limits[4][5]	
SR	Slew Rate	V_{IN} = 1V_{P-P}, f = 10kHz square Wave	50		V/µs(min)
V_{OS}	Input Offset Voltage	V_{CM} = 0V, I_O= 0mA	1	3	mV (max)
I_B	Input Bias Current	V_{CM} = 0V, I_O= 0mA	100	200	nA (max)
PSRR	Power Supply Rejection Ratio	f = DC, Input Referred	110	105	dB (min)
V_{CLIP}	Baker Clamp Clipping Voltage	Clip Output Source pin Sink pin	 97.2 –96.4	 95.5 –95.5	 V (max) V (min)
V_{BC}	Baker Clamp Flag Output Voltage	I_{FLAG} = 4.7mA	0.4		V
V_{BA}	Bias P&M Pin Open Voltage	BiasP - BiasM	10		V
I_{BIAS}	Bias Adjust Function Current		2.8		mA

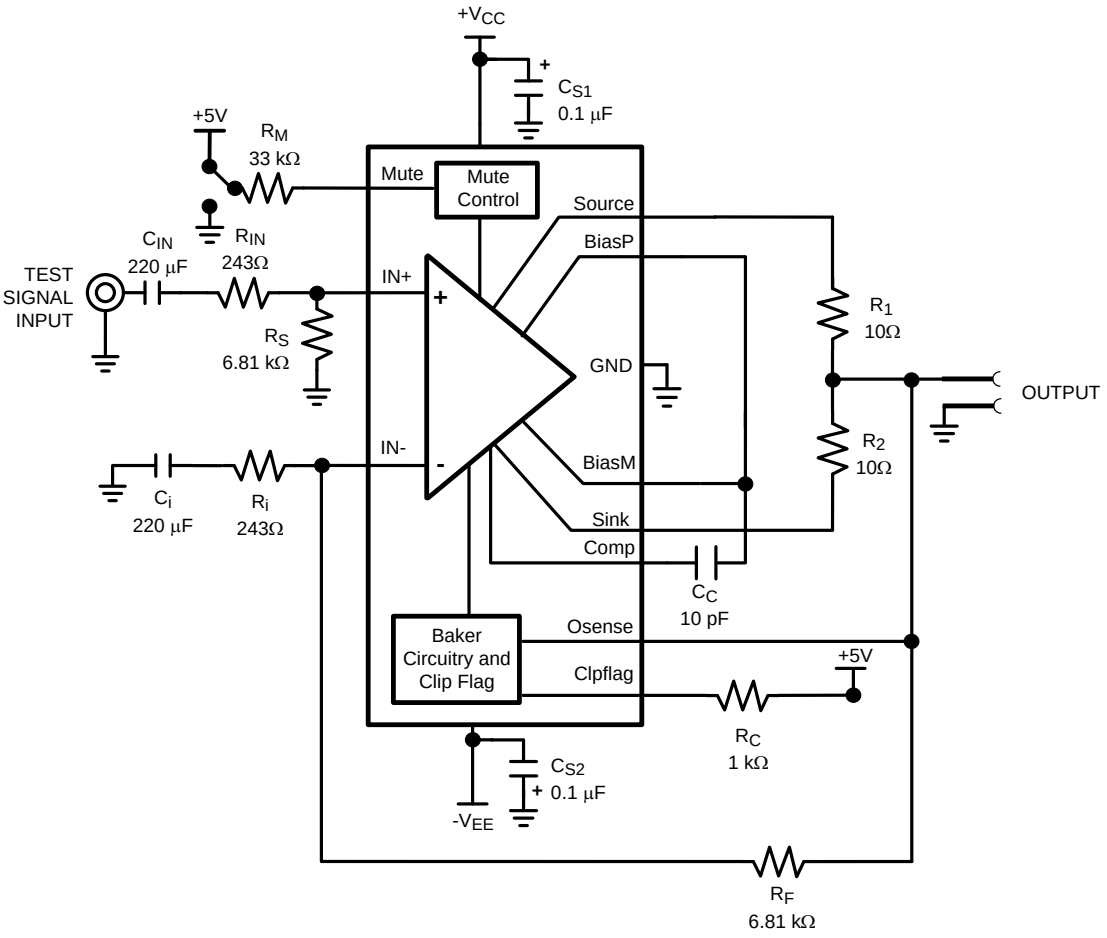


Figure 4. LME49810 Test Circuit Schematic (DC Coupled)

TYPICAL PERFORMANCE CHARACTERISTICS

Data taken with Bandwidth = 30kHz, AV = 29dB, CC = 10pF, and TA = 25°C except where specified.

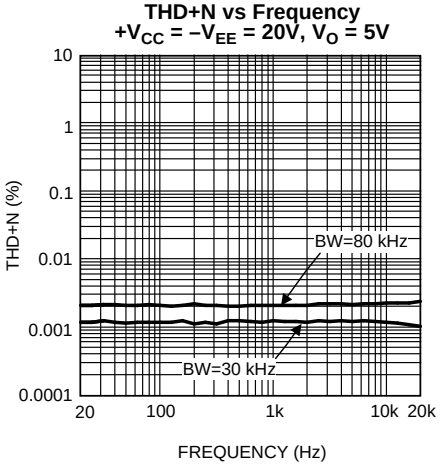


Figure 5.

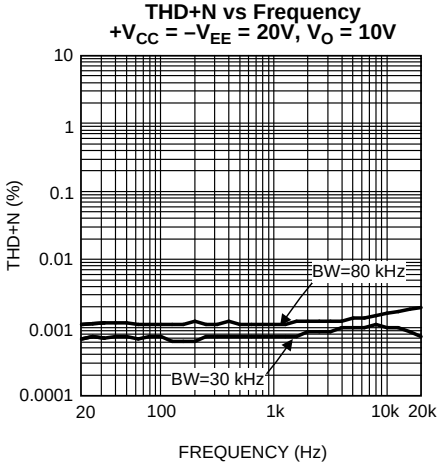


Figure 6.

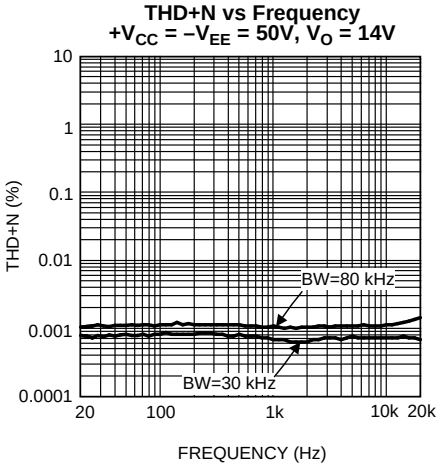


Figure 7.

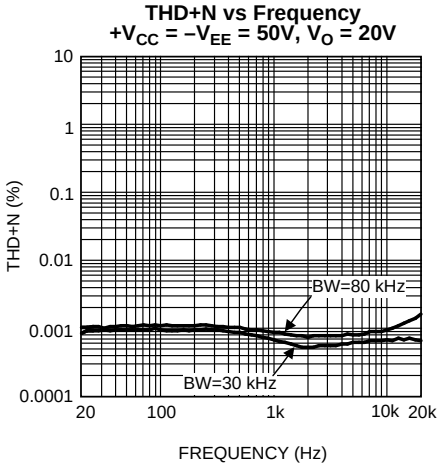


Figure 8.

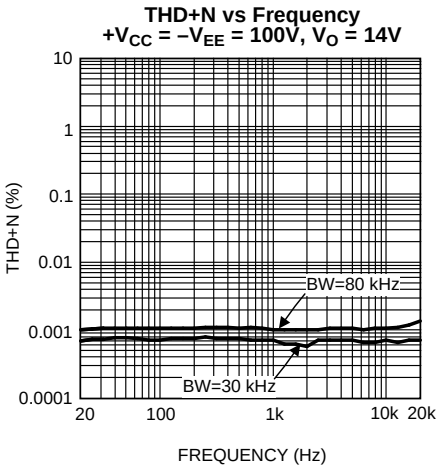


Figure 9.

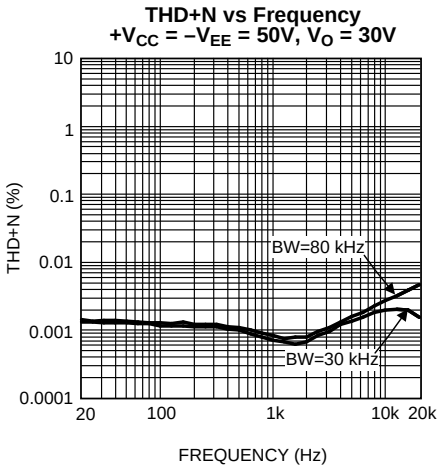


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, AV = 29dB, CC = 10pF, and TA = 25°C except where specified.

THD+N vs Output Voltage
$+V_{CC}$ = – V_{EE} = 50V, f = 20Hz

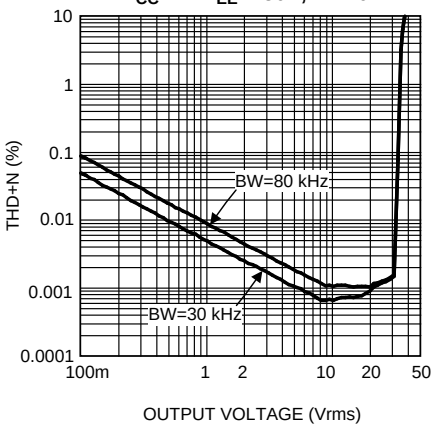


Figure 11.

THD+N vs Output Voltage
$+V_{CC}$ = –V_{EE} = 100V, f = 20Hz

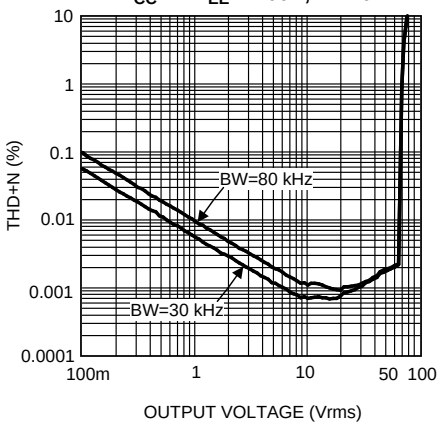


Figure 12.

THD+N vs Output Voltage
$+V_{CC}$ = –V_{EE} = 50V, f = 1kHz

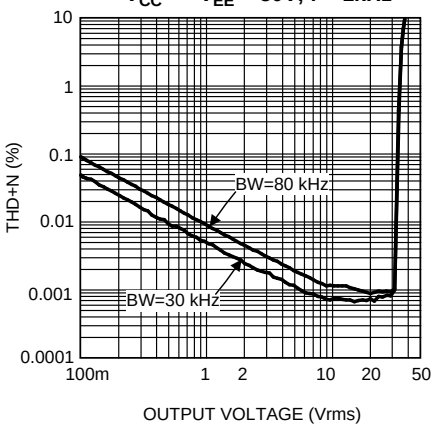


Figure 13.

THD+N vs Output Voltage
$+V_{CC}$ = – V_{EE} = 100V, f = 1kHz

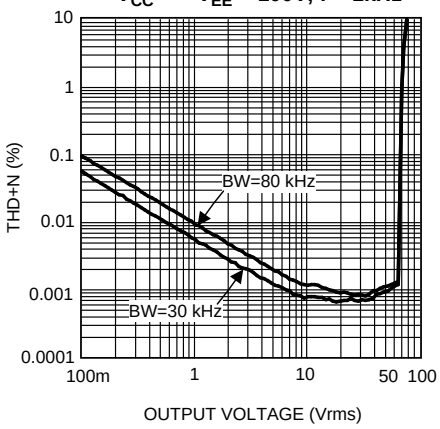


Figure 14.

THD+N vs Output Voltage
$+V_{CC}$ = –V_{EE} = 50V, f = 20kHz

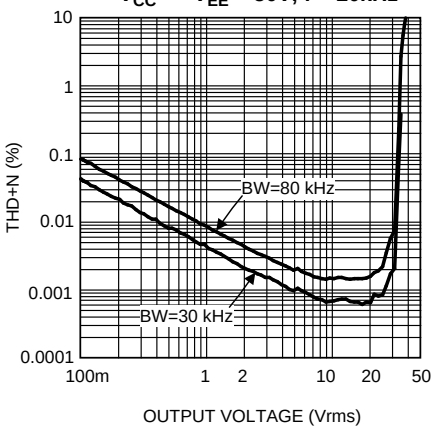


Figure 15.

THD+N vs Output Voltage
$+V_{CC}$ = –V_{EE} = 100V, f = 20kHz

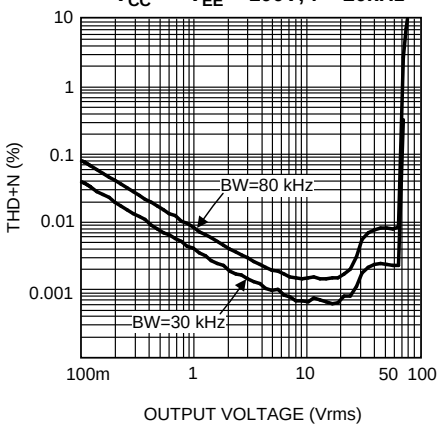


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, AV = 29dB, CC = 10pF, and TA = 25°C except where specified.

THD+N vs Output Voltage
$+V_{CC} = -V_{EE}$ = 20V, f = 20Hz

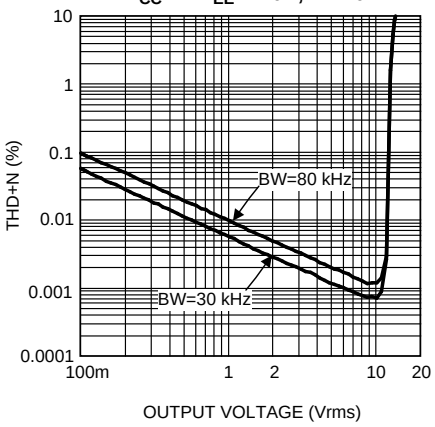


Figure 17.

THD+N vs Output Voltage
$+V_{CC} = -V_{EE}$ = 20V, f = 1kHz

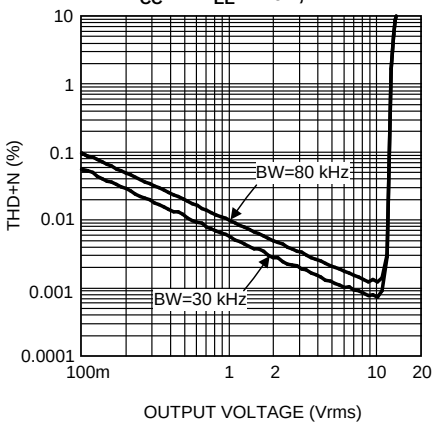


Figure 18.

THD+N vs Output Voltage
$+V_{CC} = -V_{EE}$ = 20V, f = 20kHz

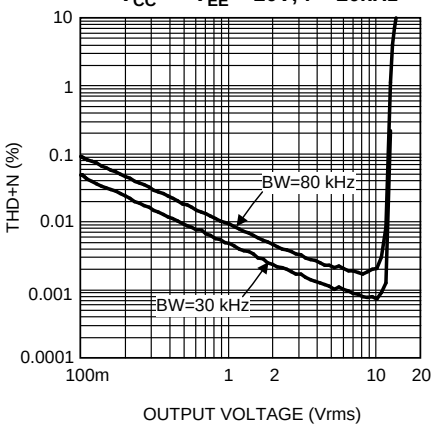


Figure 19.

Closed Loop Frequency Response
$+V_{CC} = -V_{EE}$ = 50V, V_{IN} = 1V_{RMS}

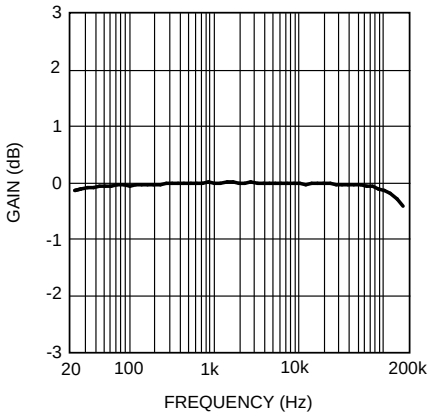


Figure 20.

Closed Loop Frequency Response
$+V_{CC} = -V_{EE}$ = 100V, V_{IN} = 1V_{RMS}

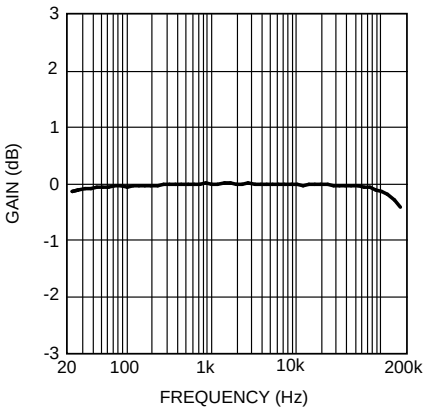


Figure 21.

PSRR vs Frequency
$+V_{CC} = -V_{EE}$ = 100V,
No Filters, Input referred, V_{RIPPLE} = 1V_{RMS} on V_{CC} pin

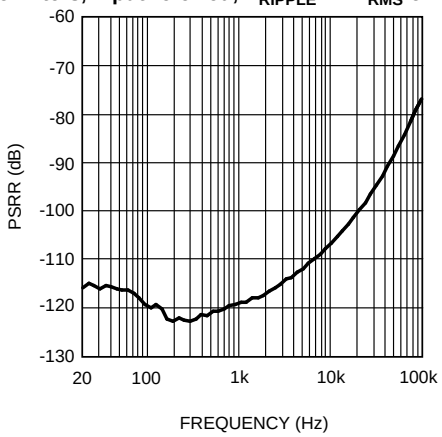


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, AV = 29dB, CC = 10pF, and TA = 25°C except where specified.

PSRR vs Frequency
$+V_{CC}$ = $-V_{EE}$ = 100V,
No Filters, Input referred, V_{RIPPLE} = 1V_{RMS} on V_{EE} pin

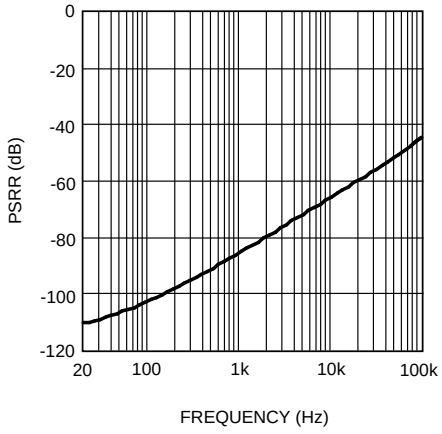


Figure 23.

Mute Attenuation vs I_{MUTE}
$+V_{CC}$ = $-V_{EE}$ = 100V

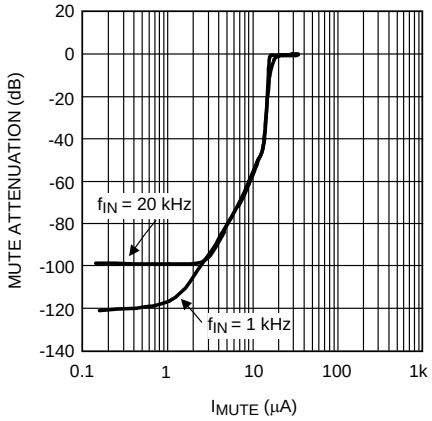


Figure 24.

Output Voltage vs Supply Voltage

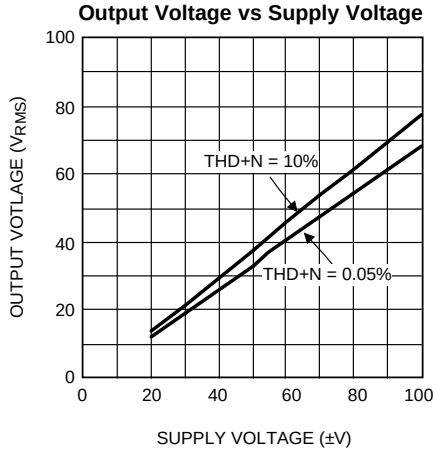


Figure 25.

Slew Rate vs Compensation Capacitor
$+V_{CC}$ = $-V_{EE}$ = 100V, V_{IN} = 1.2V_P 10kHz squarewave

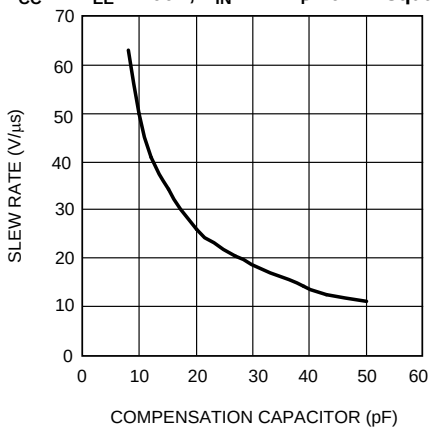


Figure 26.

Supply Current vs Supply Voltage

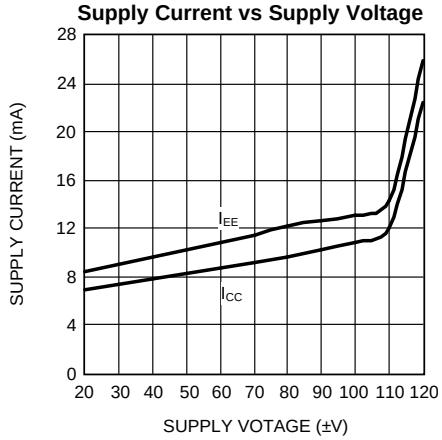


Figure 27.

Input Offset Voltage vs Supply Voltage

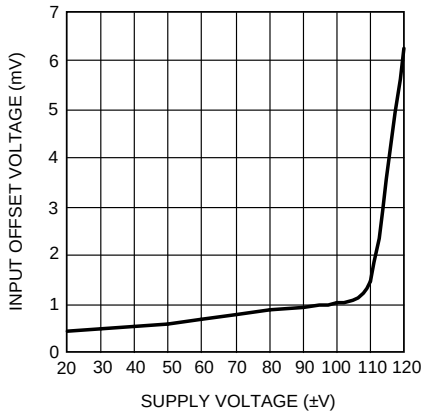


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, AV = 29dB, CC = 10pF, and TA = 25°C except where specified.

Open Loop Gain and Phase Margin
$+V_{CC} = -V_{EE} = 100V$

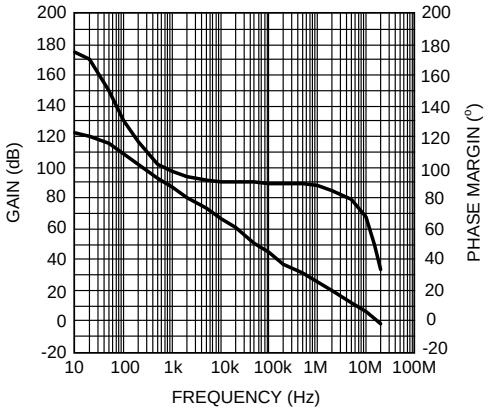


Figure 29.

CMRR vs Frequency
$+V_{CC} = -V_{EE} = 100V$

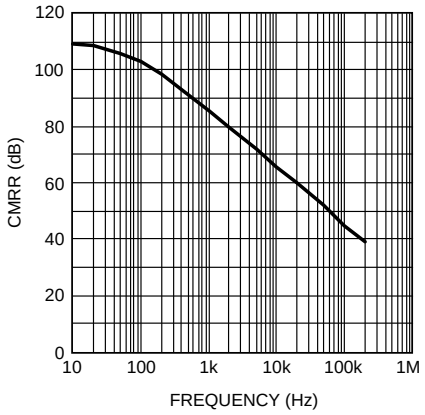


Figure 30.

Noise Floor
$+V_{CC} = -V_{EE} = 50V$, $V_{IN} = 0V$

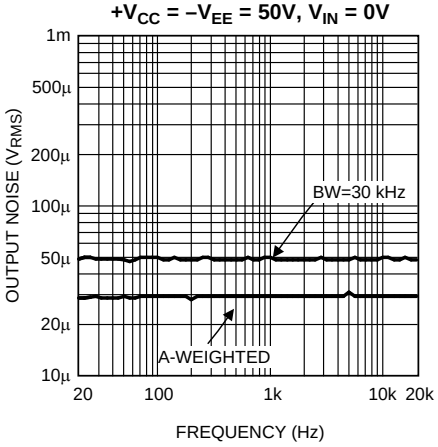


Figure 31.

Noise Floor
$+V_{CC} = -V_{EE} = 100V$, $V_{IN} = 0V$

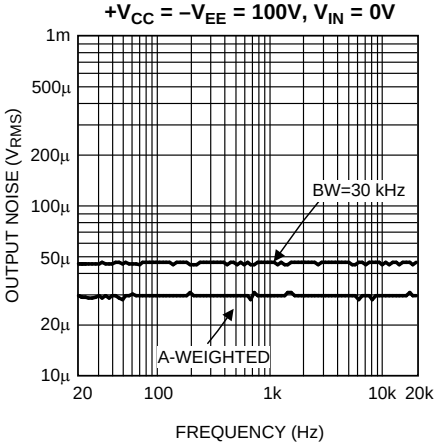


Figure 32.

Baker Clamp Flag Output
$+V_{CC} = -V_{EE} = 100V$, $V_{IN} = 4V_{RMS}$, $f_{IN} = 20kHz$
Ch1: Output, Ch2: CLPFLAG Output

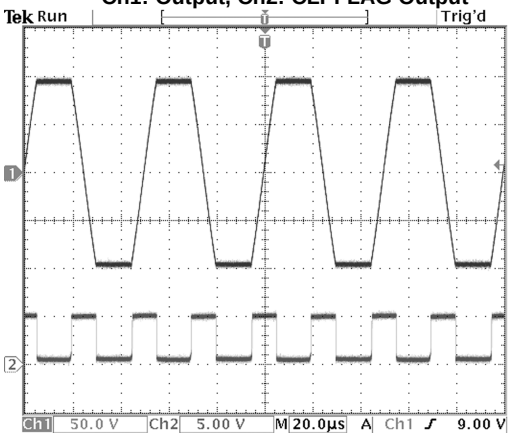


Figure 33.

APPLICATION INFORMATION

MUTE FUNCTION

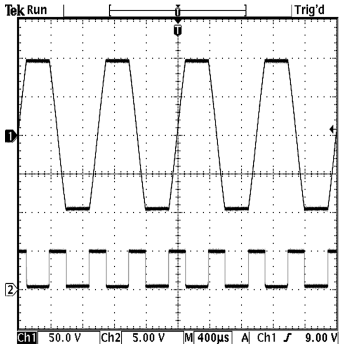
The mute function of the LME49810 is controlled by the amount of current that flows into the MUTE pin. LME49810 typically requires 50µA to 100µA of mute current flowing in order to be in "play" mode. This can be done by connecting a reference voltage (V_{MUTE}) to the MUTE pin through a resistor (R_M). The following formula can be used to calculate the mute current.

$$I_{MUTE} = (V_{MUTE}\text{-}0.7V) / (R_M\text{+}10k\Omega)\ (A) \quad (1)$$

The 10kΩ resistor value in Equation (1) is internal. Please refer to Figure 3, LME49810 Simplified Schematic, for additional details. For example, if a 5V voltage is connected through a 33kΩ resistor to the MUTE pin, then the mute current will be 100µA, according to Equation (1). Consequently, R_M can be changed to suit any other reference voltage requirement. The LME49810 will enter Mute mode if I_{MUTE} is less than 1µA which can be accomplished by shorting the MUTE pin to ground or by floating the MUTE pin. It is not recommended that more than 200µA flow into the MUTE pin because damage to LME49810 may occur and device may not function properly.

BAKER CLAMP AND CLAMP FLAG OUTPUT

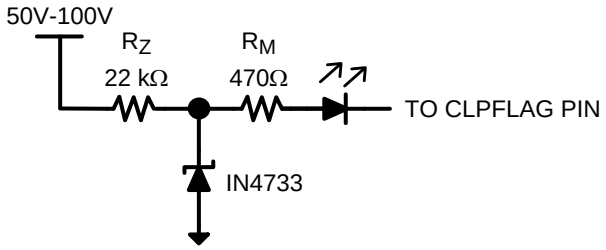
The LME49810 features a Baker Clamp function with corresponding CLPFLAG output pin. The clamp function keeps all transistors in linear operation when the output goes into clipping. In addition, when the output goes into clipping, a logic low level appears at the CLPFLAG pin. The CLPFLGAG pin can be used to drive an LED or some other visual display as shown by Figure 1. The value of logic low voltage varies and depends on I_{FLAG}. For example, if I_{FLAG} is 4.7mA then a voltage (V_{BC}) of 0.4V will appear at the CLPFLAG output pin. The smooth response of the Baker Clamp and the corresponding CLPFLAG logic output is shown in the scope photo below:



$+V_{CC} = -V_{EE} = 100V$,
$V_{IN} = 4V_{RMS}$,
$f_{IN} = 1kHz$,
$R_C = 1k\Omega$ Ch1: Output,
Ch2: CLPFLAG Output

Figure 34.

The CLPFLAG pin can source up to 10mA, and since the CLPFLAG output is an open collector output as shown by Figure 3, LME49810 Simplified Schematic, it should never be left to float under normal operation. If CLPFLAG pin is not used, then it should be connected through a resistor to a reference voltage so that I_{FLAG} is below 10mA. For example, a resistor of 1k can be used with a 5V reference voltage. This will give the I_{FLAG} of 4.7mA. In a typical LED setup, if +5V reference voltage is not available, the following circuit using a Zener diode can be used to power the CLPFLAG pin from the higher supply voltage rails of the LME49810. The power dissipation rating of R_Z will need to be at-least ½W if using a 5V Zener Diode. Alternately, the following basic formula can be used to find the proper power rating of R_Z : $P_{DZ} = (V_{CC} - V_Z)^2/R_Z$ (W). This formula can also be used to meet the design requirements of any other reference voltage that the user desires.



THERMAL PROTECTION

The LME49810 has a thermal protection scheme to prevent long-term thermal stress of the device. When the temperature on the die exceeds 150°C, the LME49810 goes into thermal shutdown. The LME49810 starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur again above 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle between the thermal shutdown temperature limits of 150°C and 145°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions. Since the die temperature is directly dependent upon the heat sink used, the heat sink should be chosen so that thermal shutdown is not activated during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device, as discussed in the DETERMINING THE CORRECT HEAT SINK section.

POWER DISSIPATION

When in “play” mode, the LME49810 draws a constant amount of current, regardless of the input signal amplitude. Consequently, the power dissipation is constant for a given supply voltage and can be computed with the equation $P_{DMAX} = I_{CC} * (V_{CC} – V_{EE})$. For a quick calculation of P_{DMAX}, approximate the current to be 11mA and multiply it by the total supply voltage (the current varies slightly from this value over the operating range).

DETERMINING THE CORRECT HEAT SINK

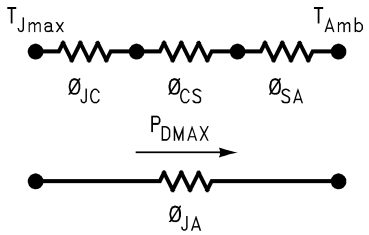
The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry is not activated under normal circumstances.

The thermal resistance from the die to the outside air, θ_{JA} (junction to ambient), is a combination of three thermal resistances, θ_{JC} (junction to case), θ_{CS} (case to sink), and θ_{SA} (sink to ambient). The thermal resistance, θ_{JC} (junction to case), of the LME49810 is 4°C/W. Using Thermalloy Thermacote thermal compound, the thermal resistance, θ_{CS} (case to sink), is about 0.2°C/W. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LME49810 is equal to the following:

$$P_{DMAX} = (T_{JMAX} - T_{AMB}) / \theta_{JA} \quad (2)$$

where

- T_{JMAX} = 150°C
- T_{AMB} is the system ambient temperature
- $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



Once the maximum package power dissipation has been calculated using Equation (2), the maximum thermal resistance, θ_{SA}, (heat sink to ambient) in °C/W for a heat sink can be calculated. This calculation is made using Equation (3) which is derived by solving for θ_{SA} from Equation (2).

$$\theta_{SA} = [(T_{JMAX} - T_{AMB}) - P_{DMAX}(\theta_{JC} + \theta_{CS})] / P_{DMAX} \quad (3)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier requirements. If the ambient temperature that the audio amplifier is to be working under is higher than 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components is required to meet the design targets of an application. The choice of external component values that will affect gain and low frequency response are discussed below.

The overall gain of the amplifier is set by resistors R_F and R_i for the non-inverting configuration shown in Figure 1. The gain is found by Equation (4) below given $R_i = R_{IN}$ and $R_F = R_S$.

$$A_V = R_F / R_i \text{ (V/V)} \quad (4)$$

For best Noise performance, lower values of resistors are used. A value of 243 is commonly used for R_i and setting the value for R_F for desired gain. For the LME49810 the gain should be set no lower than 10V/V. Gain settings below 10V/V may experience instability.

The combination of R_i and C_i (see Figure 1) creates a high pass filter. The gain at low frequency and therefore the response is determined by these components. The -3dB point can be determined from Equation (5) shown below:

$$f_i = 1 / (2\pi R_i C_i) \text{ (Hz)} \quad (5)$$

If an input coupling capacitor (C_{IN}) is used to block DC from the inputs as shown in Figure 1, there will be another high pass filter created with the combination of C_{IN} and R_{IN}. The resulting -3dB frequency response due to the combination of C_{IN} and R_{IN} can be found from Equation (6) shown below:

$$f_{IN} = 1 / (2\pi R_{IN} C_{IN}) \text{ (Hz)} \quad (6)$$

For best audio performance, the input capacitor should not be used. Without the input capacitor, any DC bias from the source will be transferred to the load. The feedback capacitor (C_i) is used to set the gain at DC to unity. Because a large value is required for a low frequency -3dB point, the capacitor is an electrolytic type. An additional small value, high quality film capacitor may be used in parallel with the feedback resistor to improve high frequency sonic performance. If DC offset in the output stage is acceptable without the feedback capacitor, it may be removed but DC gain will now be equal to AC gain.

COMPENSATION CAPACITOR

The compensation capacitor (C_C) is one of the most critical external components in value, placement and type. The capacitor should be placed close to the LME49810 and a silver mica type will give good performance. The value of the capacitor will affect slew rate and stability. The highest slew rate is possible while also maintaining stability through out the power and frequency range of operation results in the best audio performance. The value shown in Figure 1 should be considered a starting value with optimization done on the bench and in listening testing. Please refer to Slew Rate vs. C_C Graph in TYPICAL PERFORMANCE CHARACTERISTICS for determining the proper slew rate for your particular application.

SUPPLY BYPASSING

The LME49810 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as “motorboating” or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large electrolytic capacitor (10µF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1µF) to prevent any high frequency feedback through the power supply lines. If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470µF or more.

OUTPUT STAGE USING BIPOLAR TRANSISTORS

With a properly designed output stage and supply voltage of ±100V, an output power up to 500W can be generated at 0.05% THD+N into an 8Ω speaker load. With an output current of several amperes, the output transistors need substantial base current drive because power transistors usually have quite low current gain—typical h_{fe} of 50 or so. To increase the current gain, audio amplifiers commonly use Darlington style devices. Power transistors should be mounted together with the V_{BE} multiplier transistor on the same heat sink to avoid thermal run away. Please see the section BIASING TECHNIQUES AND AVOIDING THERMAL RUNAWAY for additional information.

BIASING TECHNIQUES AND AVOIDING THERMAL RUNAWAY

A class AB amplifier has some amount of distortion called Crossover distortion. To effectively minimize the crossover distortion from the output, a V_{BE} multiplier may be used instead of two biasing diodes. The LME49810 has two dedicated pins ($BIAS_M$ and $BIAS_P$) for Bias setup and provide a constant current source of about 2.8mA. A V_{BE} multiplier normally consists of a bipolar transistor (Q_{MULT}, see Figure 1) and two resistors (R_{B1} and R_{B2}, see Figure 1). A trim pot can also be added in series with R_{B1} for optional bias adjustment. A properly designed output stage, combine with a V_{BE} multiplier, can eliminate the trim pot and virtually eliminate crossover distortion. The V_{CE} voltage of Q_{MULT} (also called BIAS of the output stage) can be set by following formula:

$$V_{BIAS} = V_{BE}(1+R_{B2}/R_{B1}) \text{ (V)} \quad (7)$$

When using a bipolar output stage with the LME49810 (as in Figure 1), the designer must beware of thermal runaway. Thermal runaway is a result of the temperature dependence of V_{BE} (an inherent property of the transistor). As temperature increases, V_{BE} decreases. In practice, current flowing through a bipolar transistor heats up the transistor, which lowers the V_{BE}. This in turn increases the current gain, and the cycle repeats. If the system is not designed properly this positive feedback mechanism can destroy the bipolar transistors used in the output stage. One of the recommended methods of preventing thermal runaway is to use the same heat sink on the bipolar output stage transistor together with V_{BE} multiplier transistor. When the V_{BE} multiplier transistor is mounted to the same heat sink as the bipolar output stage transistors, it temperature will track that of the output transistors. Its V_{BE} is dependent upon temperature as well, and so it will draw more current as the output transistors heat up, reducing the bias voltage to compensate. This will limit the base current into the output transistors, which counteracts thermal runaway. Another widely popular method of preventing thermal runaway is to use low value emitter degeneration resistors (R_{E1} and R_{E2}). As current increases, the voltage at the emitter also increases, which decreases the voltage across the base and emitter. This mechanism helps to limit the current and counteracts thermal runaway.

LAYOUT CONSIDERATION AND AVOIDING GROUND LOOPS

A proper layout is virtually essential for a high performance audio amplifier. It is very important to return the load ground, supply grounds of output transistors, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. When ground is routed in this fashion, it is called a star ground or a single point ground. It is advisable to keep the supply decoupling capacitors of 0.1µF close as possible to LME49810 to reduce the effects of PCB trace resistance and inductance. Following the general rules will optimize the PCB layout and avoid ground loops problems:

a. Make use of symmetrical placement of components.
b. Make high current traces, such as output path traces, as wide as possible to accomodate output stage current requirement.
c. To reduce the PCB trace resistance and inductance, same ground returns paths should be as short as possible. If possible, make the output traces short and equal in length.
d. To reduce the PCB trace resistance and inductance, ground returns paths should be as short as possible.
e. If possible, star ground or a single point ground should be observed. Advanced planning before starting the PCB can improve audio performance.

Demo Board Schematic

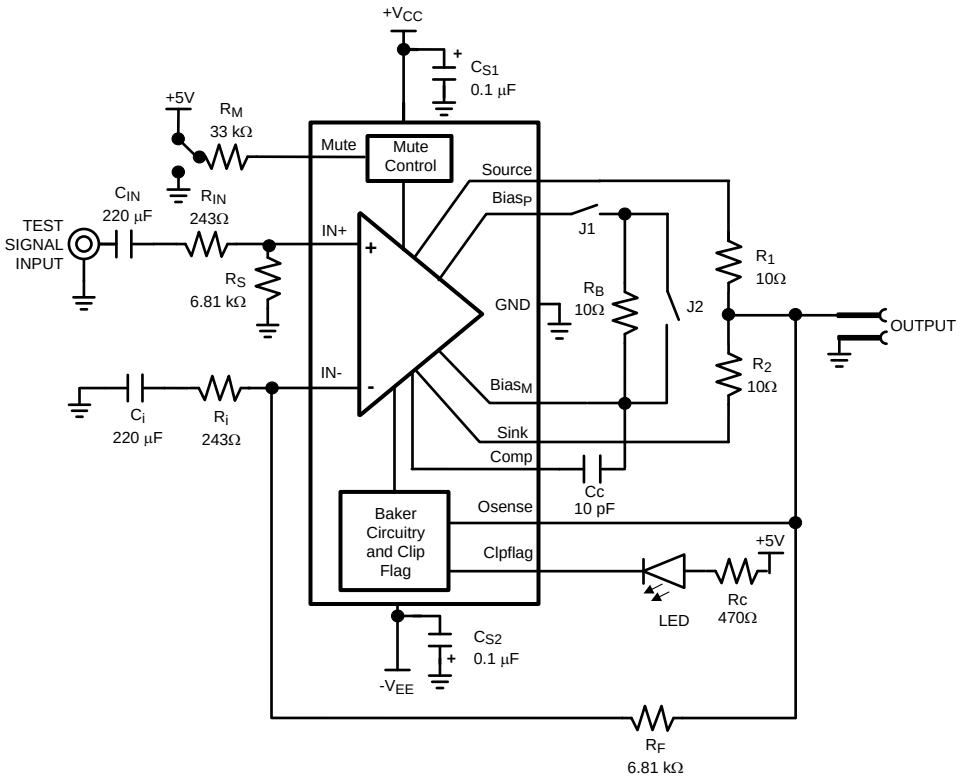


Figure 35. LME49810 Test Demo Board Schematic

Demonstration Board Layout

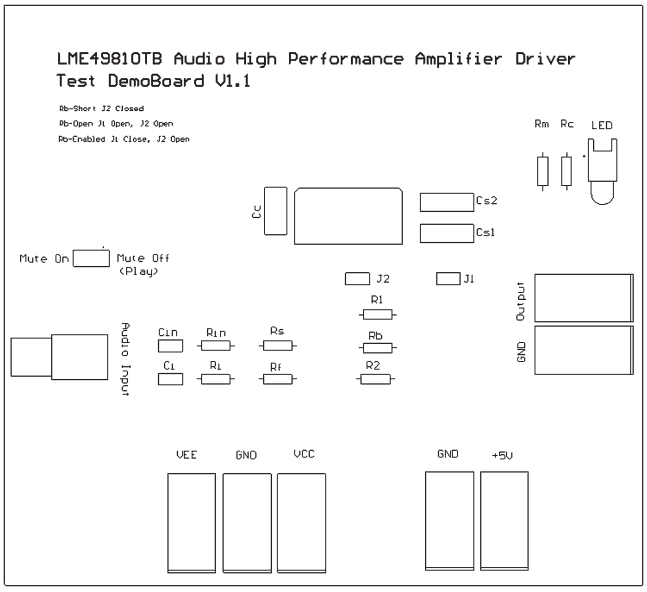


Figure 36. Silkscreen Layer

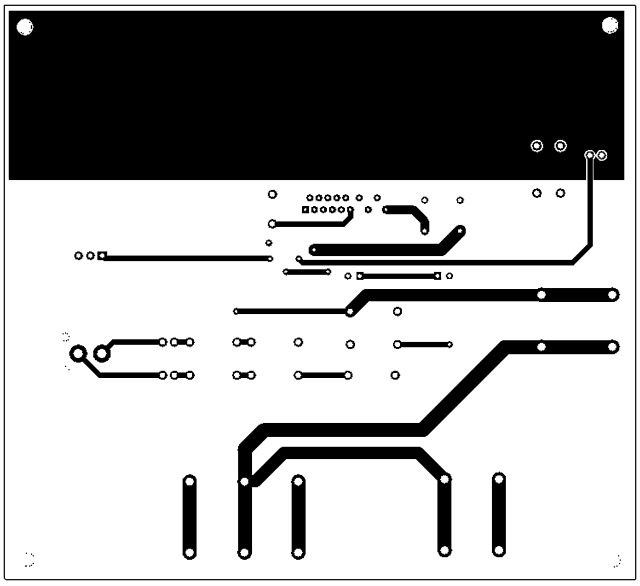


Figure 37. Top Layer

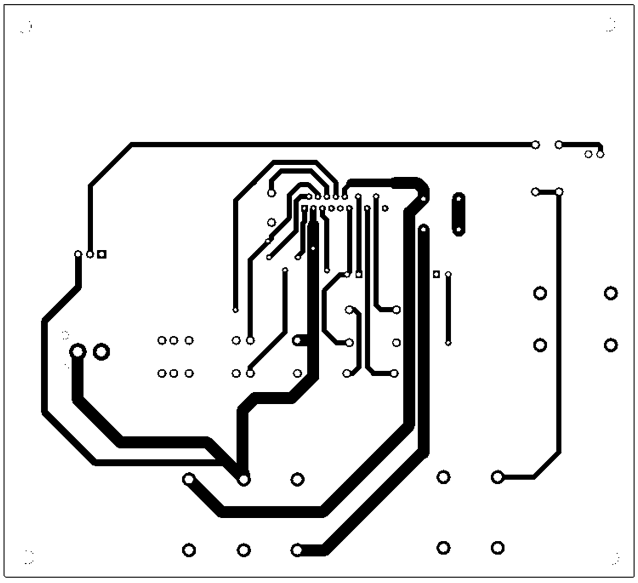


Figure 38. Bottom Layer

REVISION HISTORY

Rev	Date	Description
1.0	05/24/07	Initial WEB release.
1.01	05/29/07	Few text edits.
1.02	09/17/07	Edited curve 20216724.
C	04/05/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49810TB/NOPB	NRND	TO-OTHER	NDN	15	24	TBD	Call TI	Call TI	-20 to 85	LME49810 TB	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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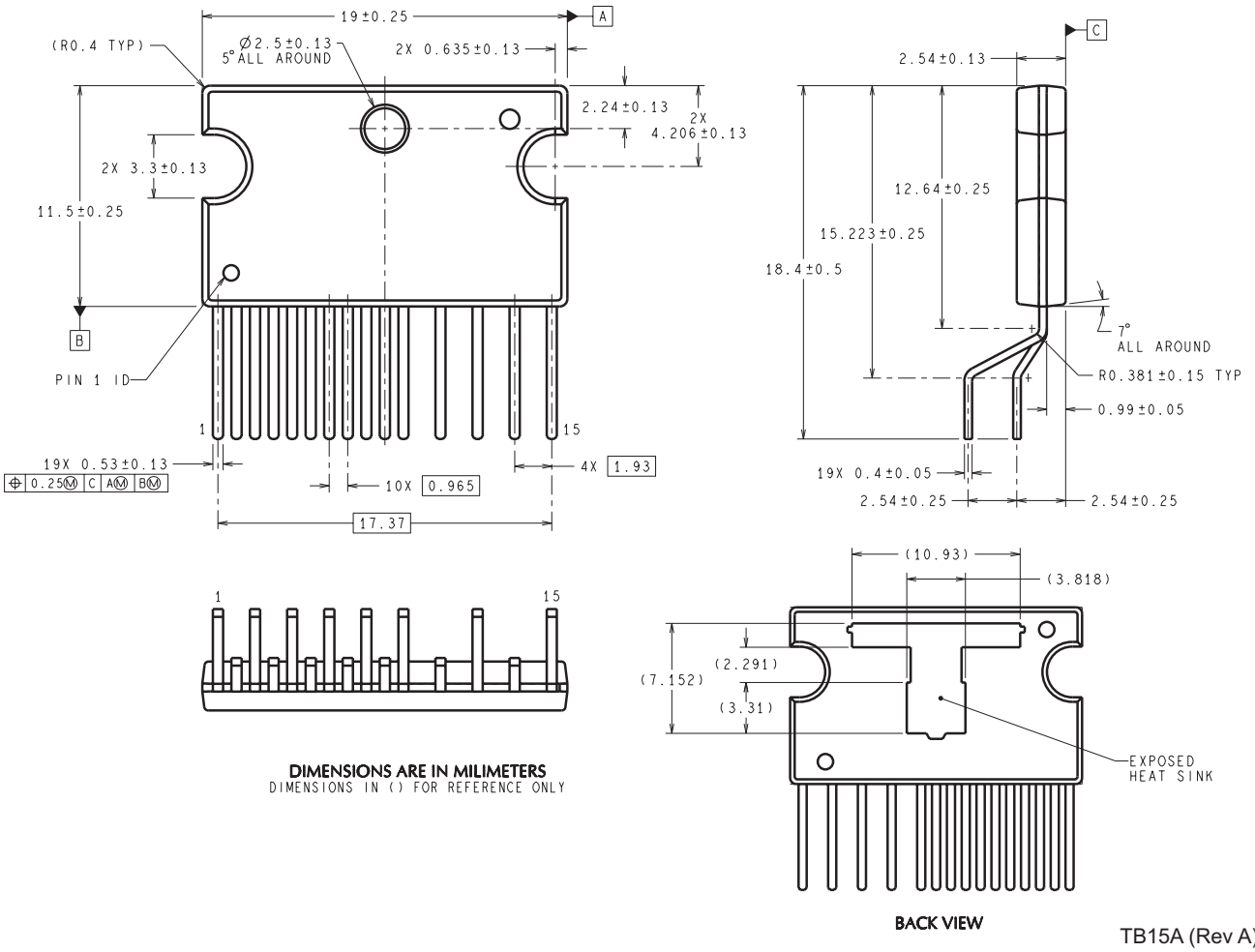
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

NDN0015A



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