LP3986
Dual Micropower 150 mA Ultra Low-Dropout CMOS Voltage Regulators in micro SMD Package

General Description
The LP3986 is a 150 mA dual low dropout regulator designed for portable and wireless applications with demanding performance and board space requirements. The LP3986 is stable with a small 1 µF ±30% ceramic output capacitor requiring smallest possible board space. The LP3986’s performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current independent of load current. Regulator ground current increases very slightly in dropout, further prolonging the battery life. Optional external bypass capacitor reduces the output noise further without slowing down the load transient response. Fast start-up time is achieved by utilizing a speed-up circuit that actively pre-charges the bypass capacitor. Power supply rejection is better than 60 dB at low frequencies and 55 dB at 10 kHz. High power supply rejection is maintained at low input voltage levels common to battery operated circuits. The LP3986 is available in a micro SMD package. Performance is specified for a −40˚C to +125˚C temperature range. For single LDO applications, please refer to the LP3985 datasheet.

Features
- Miniature 8-I/O micro SMD package
- Stable with 1µF ceramic and high quality tantalum output capacitors
- Fast turn-on
- Two independent regulators
- Logic controlled enable
- Over current and thermal protection

Key Specifications
- Guaranteed 150 mA output current per regulator
- 1nA typical quiescent current when both regulators in shutdown mode
- 60 mV typical dropout voltage at 150 mA output current
- 115 µA typical ground current
- 40 µV typical output noise
- 200 µs fast turn-on circuit
- −40˚C to +125˚C junction temperature

Applications
- CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- Portable battery applications

Typical Application Circuit

© 2005 National Semiconductor Corporation DS200034 www.national.com
**Pin Descriptions**

<table>
<thead>
<tr>
<th>Name</th>
<th>*micro SMD</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT2}$</td>
<td>A1</td>
<td>Output Voltage of the second LDO</td>
</tr>
<tr>
<td>EN2</td>
<td>B1</td>
<td>Enable input for the second LDO</td>
</tr>
<tr>
<td>BYPASS</td>
<td>C1</td>
<td>Bypass capacitor for the bandgap</td>
</tr>
<tr>
<td>GND</td>
<td>C2</td>
<td>Common ground</td>
</tr>
<tr>
<td>GND</td>
<td>C3</td>
<td>Common ground</td>
</tr>
<tr>
<td>EN1</td>
<td>B3</td>
<td>Enable input for the first LDO</td>
</tr>
<tr>
<td>$V_{OUT1}$</td>
<td>A3</td>
<td>Output Voltage of the first LDO</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>A2</td>
<td>Common input for both LDOs</td>
</tr>
</tbody>
</table>

* Note: The pin numbering scheme for the micro SMD package was revised in April 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had $V_{OUT2}$ as pin 1, EN2 as pin 2, BYPASS as pin 3, GND as pins 4 and 5, EN1 as pin 6, $V_{OUT1}$ as pin 7, and $V_{IN}$ as pin 8.
### Ordering Information

For micro SMD Package (BL has thickness of 0.995mm)

<table>
<thead>
<tr>
<th>Output Voltage (V)</th>
<th>Grade</th>
<th>Package Marking</th>
<th>LP3986 Supplied as 250 Units, Tape and Reel</th>
<th>LP3986 Supplied as 3000 Units, Tape and Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 2.5</td>
<td>STD</td>
<td>27</td>
<td>LP3986BL-2525</td>
<td>LP3986BLX-2525</td>
</tr>
<tr>
<td>2.5 2.8</td>
<td>STD</td>
<td>14</td>
<td>LP3986BL-2528</td>
<td>LP3986BLX-2528</td>
</tr>
<tr>
<td>2.5 1.8</td>
<td>STD</td>
<td>30</td>
<td>LP3986BL-2518</td>
<td>LP3986BLX-2518</td>
</tr>
<tr>
<td>2.6 2.6</td>
<td>STD</td>
<td>29</td>
<td>LP3986BL-2626</td>
<td>LP3986BLX-2626</td>
</tr>
<tr>
<td>2.8 1.8</td>
<td>STD</td>
<td>25</td>
<td>LP3986BL-2818</td>
<td>LP3986BLX-2818</td>
</tr>
<tr>
<td>2.8 2.8</td>
<td>STD</td>
<td>10</td>
<td>LP3986BL-2828</td>
<td>LP3986BLX-2828</td>
</tr>
<tr>
<td>2.85 2.85</td>
<td>STD</td>
<td>11</td>
<td>LP3986BL-285285</td>
<td>LP3986BLX-285285</td>
</tr>
<tr>
<td>2.9 2.9</td>
<td>STD</td>
<td>15</td>
<td>LP3986BL-2929</td>
<td>LP3986BLX-2929</td>
</tr>
<tr>
<td>3.0 2.8</td>
<td>STD</td>
<td>26</td>
<td>LP3986BL-3028</td>
<td>LP3986BLX-3028</td>
</tr>
<tr>
<td>3.0 3.0</td>
<td>STD</td>
<td>12</td>
<td>LP3986BL-3030</td>
<td>LP3986BLX-3030</td>
</tr>
<tr>
<td>3.1 3.1</td>
<td>STD</td>
<td>13</td>
<td>LP3986BL-3131</td>
<td>LP3986BLX-3131</td>
</tr>
<tr>
<td>3.1 3.3</td>
<td>STD</td>
<td>16</td>
<td>LP3986BL-3133</td>
<td>LP3986BLX-3133</td>
</tr>
<tr>
<td>3.3 3.3</td>
<td>STD</td>
<td>17</td>
<td>LP3986BL-3333</td>
<td>LP3986BLX-3333</td>
</tr>
</tbody>
</table>

For micro SMD Package (TL has thickness of 0.600mm)

<table>
<thead>
<tr>
<th>Output Voltage (V)</th>
<th>Grade</th>
<th>Package Marking</th>
<th>LP3986 Supplied as 250 Units, Tape and Reel</th>
<th>LP3986 Supplied as 3000 Units, Tape and Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 2.5</td>
<td>STD</td>
<td>27</td>
<td>LP3986TL-2525</td>
<td>LP3986TLX-2525</td>
</tr>
<tr>
<td>2.5 2.8</td>
<td>STD</td>
<td>14</td>
<td>LP3986TL-2528</td>
<td>LP3986TLX-2528</td>
</tr>
<tr>
<td>2.5 1.8</td>
<td>STD</td>
<td>30</td>
<td>LP3986TL-2518</td>
<td>LP3986TLX-2518</td>
</tr>
<tr>
<td>2.6 2.6</td>
<td>STD</td>
<td>28</td>
<td>LP3986TL-2626</td>
<td>LP3986TLX-2626</td>
</tr>
<tr>
<td>2.8 1.8</td>
<td>STD</td>
<td>25</td>
<td>LP3986TL-2818</td>
<td>LP3986TLX-2818</td>
</tr>
<tr>
<td>2.8 2.8</td>
<td>STD</td>
<td>10</td>
<td>LP3986TL-2828</td>
<td>LP3986TLX-2828</td>
</tr>
<tr>
<td>2.85 2.85</td>
<td>STD</td>
<td>11</td>
<td>LP3986TL-285285</td>
<td>LP3986TLX-285285</td>
</tr>
<tr>
<td>2.9 2.9</td>
<td>STD</td>
<td>15</td>
<td>LP3986TL-2929</td>
<td>LP3986TLX-2929</td>
</tr>
<tr>
<td>3.0 2.8</td>
<td>STD</td>
<td>26</td>
<td>LP3986TL-3028</td>
<td>LP3986TLX-3028</td>
</tr>
<tr>
<td>3.0 3.0</td>
<td>STD</td>
<td>12</td>
<td>LP3986TL-3030</td>
<td>LP3986TLX-3030</td>
</tr>
<tr>
<td>3.1 3.1</td>
<td>STD</td>
<td>13</td>
<td>LP3986TL-3131</td>
<td>LP3986TLX-3131</td>
</tr>
<tr>
<td>3.1 3.3</td>
<td>STD</td>
<td>16</td>
<td>LP3986TL-3133</td>
<td>LP3986TLX-3133</td>
</tr>
<tr>
<td>3.3 3.3</td>
<td>STD</td>
<td>17</td>
<td>LP3986TL-3333</td>
<td>LP3986TLX-3333</td>
</tr>
</tbody>
</table>

For 3K Units on Tape and Reel

Order Information LP 3986 Micro SMD package

- V<sub>OUT1</sub>
- V<sub>OUT2</sub>

For 3K Units on Tape and Reel
Absolute Maximum Ratings (Notes 1, 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- $V_{IN}, V_{EN}$: -0.3 to 6.5V
- $V_{OUT}$: -0.3 to $(V_{IN}+0.3V) \leq 6.5V$
- Junction Temperature: 150°C
- Storage Temperature: -65°C to +150°C
- Pad Temp. (Note 3): 235°C
- Maximum Power Dissipation (Note 4): 364mW
- ESD Rating (Note 5):
  - Human Body Model: 2kV
  - Machine Model: 200V

Operating Ratings (Notes 1, 2)

- $V_{IN}$: 2.7 to 6V
- $V_{EN}$: 0 to $(V_{IN}+0.3V) \leq 6V$
- Junction Temperature: -40°C to +125°C
- Thermal Resistance $\theta_{JA}$: 220°C/W
- Maximum Power Dissipation (Note 6): 250mW

Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5V$, $C_{IN} = 1 \mu F$, $I_{OUT} = 1mA$, $C_{OUT} = 1 \mu F$, $C_{BYPASS} = 0.01\mu F$. Typical values and limits appearing in standard typeface are for $T_{J} = 25°C$. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, -40°C to +125°C. (Note 7) (Note 8)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Limit</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_{OUT}$</td>
<td>Output Voltage Tolerance</td>
<td>$I_{OUT} = 1mA$</td>
<td>$-2.5$</td>
<td>$2.5$</td>
<td>% of $V_{OUT(nom)}$</td>
</tr>
<tr>
<td></td>
<td>Line Regulation Error (Note 9)</td>
<td>$V_{IN} = (V_{OUT(nom)} + 0.5V)$ to 6.0V, $I_{OUT} = 1mA$</td>
<td>0.006</td>
<td>0.092</td>
<td>%/V</td>
</tr>
<tr>
<td></td>
<td>Load Regulation Error (Note 10)</td>
<td>$I_{OUT} = 1mA$ to 150mA</td>
<td>0.003</td>
<td>0.006</td>
<td>%/mA</td>
</tr>
<tr>
<td></td>
<td>Output AC Line Regulation</td>
<td>$V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 150mA$ (Figure 1)</td>
<td>1.5</td>
<td></td>
<td>mV P-P</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>$V_{IN} = 3.1V$, $f = 1kHz$, $I_{OUT} = 50mA$ (Figure 2)</td>
<td>60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>Both Regulators ON $V_{EN} = 1.4V$, $I_{OUT} = 0mA$</td>
<td>115</td>
<td>200</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Both Regulators ON $V_{EN} = 1.4V$, $I_{OUT} = 0$ to 150mA</td>
<td>220</td>
<td>320</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>One Regulator ON $V_{EN} = 1.4V$, $I_{OUT} = 0mA$</td>
<td>75</td>
<td>130</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>One Regulator ON $V_{EN} = 1.4V$, $I_{OUT} = 0$ to 150mA</td>
<td>130</td>
<td>200</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN} = 0.4V$, Both Regulators OFF (shutdown)</td>
<td>0.001</td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short Circuit Current Limit</td>
<td>Output Grounded</td>
<td>600</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OUT(PK)}$</td>
<td>Peak Output Current (Note 15)</td>
<td>$V_{OUT} \geq V_{OUT(nom)} + 5%$</td>
<td>500</td>
<td>300</td>
<td>mA</td>
</tr>
</tbody>
</table>
### Electrical Characteristics (Continued)

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5V$, $C_{IN} = 1 \mu F$, $I_{OUT} = 1mA$, $C_{OUT} = 1 \mu F$, $C_{BYPASS} = 0.01\mu F$. Typical values and limits appearing in standard typeface are for $T_J = 25^\circ C$. Limits appearing in boldface type apply over the entire junction temperature range for operation, $-40^\circ C$ to $+125^\circ C$. (Note 7) (Note 8)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Limit</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{ON}$</td>
<td>Turn-On Time (Note 12)</td>
<td>$C_{BYPASS} = 0.01 \mu F$</td>
<td>200</td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Output Noise Voltage</td>
<td>$BW = 10$ Hz to 100 kHz, $C_{OUT} = 1 \mu F$</td>
<td>40</td>
<td></td>
<td>$\mu V_{rms}$</td>
</tr>
<tr>
<td>$\rho_n(1/f)$</td>
<td>Output Noise Density</td>
<td>$f = 120$ Hz, $C_{OUT} = 1 \mu F$</td>
<td>1</td>
<td></td>
<td>$\mu V/\sqrt{Hz}$</td>
</tr>
<tr>
<td>$I_{EN}$</td>
<td>Maximum Input Current at $EN$</td>
<td>$V_{EN} = 0.4$ and $V_{IN} = 6V$</td>
<td>±10</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Maximum Low Level Input Voltage at $EN$</td>
<td>$V_{IN} = 2.7$ to $6V$</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Minimum High Level Input Voltage at $EN$</td>
<td>$V_{IN} = 2.7$ to $6V$</td>
<td>1.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Xtalk</td>
<td>Crosstalk Rejection</td>
<td>$\Delta I_{Load1} = 150$ mA at 1KHz rate, $\Delta I_{Load2} = 1$ mA, $\Delta V_{OUT1}/\Delta V_{OUT}$</td>
<td>−60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\Delta I_{Load1} = 150$ mA at 1KHz rate, $\Delta I_{Load2} = 1$ mA, $\Delta V_{OUT1}/\Delta V_{OUT}$</td>
<td>−60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input capacitance (Note 13)</td>
<td>All $V_{OUT} &gt; 2.5V$, $V_{IN,MN} &gt; = 2.9V$</td>
<td>1</td>
<td></td>
<td>$\mu F$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If $V_{OUT} = 1.8V$, $V_{IN,MN} &gt; = 2.9V$</td>
<td>4.7</td>
<td></td>
<td>$\mu F$</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>Capacitance (Note 13)</td>
<td>All $V_{OUT} &gt; 2.5V$, $V_{IN,MN} &gt; = 2.9V$</td>
<td>1</td>
<td>22</td>
<td>$\mu F$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If $V_{OUT} = 1.8V$, $V_{IN,MN} &gt; = 2.9V$</td>
<td>2.2</td>
<td>22</td>
<td>$\mu F$</td>
</tr>
<tr>
<td>ESR</td>
<td></td>
<td>(Note 14)</td>
<td>5</td>
<td>500</td>
<td>m$\Omega$</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All voltages are with respect to the potential at the GND pin.

**Note 3:** Additional information on pad temperature can be found in National Semiconductor Application Note (AN-1112).

**Note 4:** The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula:

$$P_D = \frac{(T_J - T_A)}{\theta_{JA}}$$

Where $T_J$ is the junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance. The 364mW rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, $150^\circ C$, for $T_J$, $70^\circ C$ for $T_A$, and $220^\circ C/W$ for $\theta_{JA}$. More power can be dissipated safely at ambient temperatures below $70^\circ C$. Less power can be dissipated safely at ambient temperatures above $70^\circ C$. The Absolute Maximum power dissipation can be increased by 4.5mW for each degree below $70^\circ C$, and it must be derated by 4.5mW for each degree above $70^\circ C$.

**Note 5:** The human body model is $100pF$ discharged through a $1.5k\Omega$ resistor into each pin. The machine model is a $200pF$ capacitor discharged directly into each pin.

**Note 6:** Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250mW rating appearing under Operating Ratings results from substituting the maximum junction temperature, $125^\circ C$, for $T_J$, $70^\circ C$ for $T_A$, and $220^\circ C/W$ for $\theta_{JA}$ into (1) above. More power can be dissipated at ambient temperatures below $70^\circ C$. Less power can be dissipated at ambient temperatures above $70^\circ C$. The maximum power dissipation for operation can be increased by 4.5mW for each degree below $70^\circ C$, and it must be derated by 4.5mW for each degree above $70^\circ C$.

**Note 7:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with $T_J = 25^\circ C$ or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 8:** The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.

**Note 9:** The output voltage changes slightly with line voltage. An increase in the line voltage results in a slight increase in the output voltage and vice versa.

**Note 10:** The output voltage changes slightly with load current. An increase in the load current results in a slight decrease in the output voltage and vice versa. Tested limit applies to $V_{OUT} < 5V$.

**Note 11:** Dropout voltage is the input-to-output voltage difference at which the output voltage is $100mV$ below its nominal value.

**Note 12:** Turn-on time is that between the enable input just exceeding $V_{IH}$ and the output voltage just reaching $95\%$ of its nominal value.

**Note 13:** Range of capacitor values for which the device will remain stable. This electrical specification is guaranteed by design.

**Note 14:** Range of capacitor ESR values for which the device will remain stable. This electrical specification is guaranteed by design.

**Note 15:** $I_{PEAK}$ guaranteed for $V_{OUT} > 5V$.
Test Signals

FIGURE 1. Line Regulation Input Test Signal

FIGURE 2. PSRR Input Test Signal
Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu F$ Ceramic, $C_{BP} = 0.01\mu F$, $V_{IN} = V_{OUT} + 0.5$, $T_A = 25^\circ C$, both enable pins are tied to $V_{IN}$.

**Power Supply Rejection Ratio ($C_{BP} = 0.001\mu F$)**

![PSRR Graph for $C_{BP} = 0.001\mu F$](20003410)

**Power Supply Rejection Ratio ($C_{BP} = 0.01\mu F$)**

![PSRR Graph for $C_{BP} = 0.01\mu F$](20003447)

**Power Supply Rejection Ratio ($C_{BP} = 0.1\mu F$)**

![PSRR Graph for $C_{BP} = 0.1\mu F$](20003448)

**Output Noise Spectral Density**

![Noise Spectral Density Graph](20003451)

**Line Transient Response ($C_{BP} = 0.001\mu F$)**

![Line Transient Response Graph for $C_{BP} = 0.001\mu F$](20003413)

**Line Transient Response ($C_{BP} = 0.01\mu F$)**

![Line Transient Response Graph for $C_{BP} = 0.01\mu F$](20003449)
Typical Performance Characteristics

Unless otherwise specified, $C_{\text{IN}} = C_{\text{OUT}} = 1\mu\text{F Ceramic}$, $C_{\text{BP}} = 0.01\mu\text{F}$, $V_{\text{IN}} = V_{\text{OUT}} + 0.5$, $T_A = 25^\circ\text{C}$, both enable pins are tied to $V_{\text{IN}}$ (Continued).

**Load Transient & Cross Talk ($V_{\text{IN}} = V_{\text{OUT}} + 0.2\text{V}$)**

- $I_1 = 150\text{mA}$ to $1\text{mA}$
- $I_2 = 1\text{mA}$
- $C_{\text{OUT}} = 4.7\mu\text{F}$
- $C_{\text{BP}} = 0.01\mu\text{F}$

**Start-Up Time ($C_{\text{BP}} = 0.001, 0.01, 0.1\mu\text{F}$)**

- $V_{\text{IN}} (2\text{V/Div})$
- $V_{\text{OUT1}} (1\text{V/Div})$
- $V_{\text{OUT2}} (1\text{V/Div})$

**Enable Response ($V_{\text{IN}} = 4.2\text{V}$)**

- $V_{\text{EN1}}$
- $V_{\text{OUT1}} (1\text{V/Div})$
- $V_{\text{OUT2}} (100\text{mV/Div})$

**Enable Response ($V_{\text{IN}} = V_{\text{OUT}} + 0.2\text{V}$)**

- $V_{\text{EN2}} = \text{Hi}$
- $V_{\text{OUT1}} (1\text{V/Div})$
- $V_{\text{OUT2}} (100\text{mV/Div})$

---

www.national.com
Typical Performance Characteristics

Unless otherwise specified, \( C_{IN} = C_{OUT} = 1 \mu F \) Ceramic, \( C_{BF} = 0.01 \mu F \), \( V_{IN} = V_{OUT} + 0.5 \), \( T_A = 25^\circ C \), both enable pins are tied to \( V_{IN} \) (Continued)
Application Hints

EXTERNAL CAPACITORS
Like any low-dropout regulator, the LP3986 requires external capacitors for regulator stability. The LP3986 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR
An input capacitance of ≈ 1µF is required between the LP3986 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≈ 1µF over the entire operating temperature range.

OUTPUT CAPACITOR
The LP3986 is designed specifically to work with very small ceramic output capacitors, any ceramic capacitor (temperature characteristics X7R, X5R, Z5U or Y5V) in 1 to 22 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3986 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range.

NO-LOAD STABILITY
The LP3986 will remain stable and in regulation with no-load (other than the internal voltage divider). This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS
The LP3986 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3986.

The ceramic capacitor’s capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55˚C to +125˚C, will only vary the capacitance to within ±15%. Most large value ceramic capacitors (≈ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25˚C to 85˚C. Therefore, X7R is recommended over Z5U and Y5 in applications where the ambient temperature will change significantly above or below 25˚C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to −40˚C, so some guard band must be allowed.

NOISE BYPASS CAPACITOR
Connecting a 0.01µF capacitor between the CBYPASS pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The use of this 0.01µF bypass capacitor is strongly recommended to prevent overshoot on the output during start up.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDO’s, addition of a noise reduction capacitor does not effect the transient response of the device.

ON/OFF INPUT OPERATION
The LP3986 is turned off by pulling the VEN pin low, and turned on by pulling it high. If this feature is not used, the VEN pin should be tied to VIN to keep the regulator output on at all times. To assure proper operation, the signal source used to drive the VEN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under VIL and VIH*.

FAST ON-TIME
The LP3986 outputs are turned on after Vref voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70µA current source. The current source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass capacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.
Application Hints (Continued)

MICRO SMD MOUNTING
The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note (AN-1112). Referring to the section Surface Mount Technology (SMT) Assembly Considerations.
For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

MICRO SMD LIGHT SENSITIVITY
Exposing the micro SMD device to direct sunlight will cause misoperation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A micro SMD test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.
Physical Dimensions

inches (millimeters) unless otherwise noted

The dimensions for X1, X2 and X3 are as follows:

X1 = 1.55mm
X2 = 1.55mm
X3 = 0.995mm
Physical Dimensions

inches (millimeters) unless otherwise noted (Continued)

micro SMD, 8 Bump
NS Package Number ATL08CCA
The dimensions for X1, X2 and X3 are as follows:
X1 = 1.55mm
X2 = 1.55mm
X3 = 0.600mm

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves
the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL’S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS
WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR
CORPORATION. As used herein:

1. Life support devices or systems are devices or systems

   which, (a) are intended for surgical implant into the body, or
   (b) support or sustain life, and whose failure to perform when
   properly used in accordance with instructions for use
   provided in the labeling, can be reasonably expected to result
   in a significant injury to the user.

2. A critical component is any component of a life support
device or system whose failure to perform can be reasonably
expected to cause the failure of the life support device or
system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products
Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain
no “Banned Substances” as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.