TOSHIBA Insulated Gate Bipolar Transistor  Silicon N Channel IGBT

GT8G134

Strobe Flash Applications
- Compact and Thin (TSSOP-8) package
- Enhancement-mode
- Peak collector current: IC = 150 A (max)
  \( (\text{at } V_{GE}=2.5\text{V(min)})/ \)

Absolute Maximum Ratings (Ta = 25°C)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-emitter voltage</td>
<td>VCES</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>Gate-emitter voltage DC</td>
<td>VGES</td>
<td>± 4</td>
<td>V</td>
</tr>
<tr>
<td>Gate-emitter voltage Pulse</td>
<td>VGES</td>
<td>± 5</td>
<td>V</td>
</tr>
<tr>
<td>Collector current Pulse (Note 1)</td>
<td>ICP</td>
<td>150</td>
<td>A</td>
</tr>
<tr>
<td>Collector power dissipation (t=10 s) (Note 2a)</td>
<td>P_C (1)</td>
<td>1.1</td>
<td>W</td>
</tr>
<tr>
<td>Collector power dissipation (t=10 s) (Note 2b)</td>
<td>P_C (2)</td>
<td>0.6</td>
<td>W</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>Tj</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>Tstg</td>
<td>59~150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (Handling Precautions/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance, junction to ambient (t=10 s) (Note 2a)</td>
<td>Rth (j-a) (1)</td>
<td>114</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal resistance, junction to ambient (t&gt;10 s) (Note 2b)</td>
<td>Rth (j-a) (2)</td>
<td>208</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Marking (Note 3)

Note: For (Note 1), (Note 2a), (Note 2b) and (Note 3), Please refer to the next page.

Part No. (or abbreviation code)

Weight: 0.035 g (typ.)

Circuit Configuration

Lot No. A line indicates lead (Pb)-free package or lead (Pb)-free finish.
### Electrical Characteristics (Ta = 25°C)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate leakage current</td>
<td>$I_{GES}$</td>
<td>$V_{GE} = \pm 4 \text{ V}, V_{CE} = 0$</td>
<td></td>
<td>---</td>
<td>± 10</td>
<td>μA</td>
</tr>
<tr>
<td>Collector cut-off current</td>
<td>$I_{CES}$</td>
<td>$V_{CE} = 400 \text{ V}, V_{GE} = 0$</td>
<td></td>
<td>---</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>Gate-emitter cut-off voltage</td>
<td>$V_{GE} (\text{OFF})$</td>
<td>$I_C = 1 \text{ mA}, V_{CE} = 5 \text{ V}$</td>
<td>0.05</td>
<td>1.0</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>Collector-emitter saturation voltage</td>
<td>$V_{CE (sat)}$</td>
<td>$I_C = 150 \text{ A}, V_{GE} = 2.5 \text{ V}$</td>
<td>3.4</td>
<td>---</td>
<td>---</td>
<td>V</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>$C_{ies}$</td>
<td>$V_{CE} = 10 \text{ V}, V_{GE} = 0, f = 1 \text{ MHz}$</td>
<td>≥ 560</td>
<td>---</td>
<td>---</td>
<td>pF</td>
</tr>
</tbody>
</table>

#### Switching time

- **Rise time** $t_r$:
  - $3 \text{ V}$
  - $0.6$ μs
- **Turn-on time** $t_{on}$:
  - $0.8$ μs
- **Fall time** $t_f$:
  - $1.2$ μs
- **Turn-off time** $t_{off}$:
  - $1.8$ μs

#### Note

**Note 1:** Please use devices on condition that the junction temperature is below 150°C. Repetitive rating: pulse width limited by maximum junction temperature.

**Note 2a:** Device mounted on a glass-epoxy board (a)

**Note 2b:** Device mounted on a glass-epoxy board (b)

**Note 3:** ○ on lower right of the marking indicates Pin 1.

- Weekly code: (Three digits)
  - 01 for first week of year, continues up to 52 or 53
- Year of manufacture
  - (One low-order digits of calendar year)

- Pb-Free Finish (Only a coating lead terminal):
  - It is marking about an underline to a week of manufacture mark.
Caution on handling

This device is MOS gate type. Therefore, please care of a protection from ESD in your handling.

Caution in design

You should be design dV/dt value under Icp=150A is below 400 V/μs when IGBT turn off under Ta=70°C. You should be design to don’t flow collector current through terminal number 3.

● definition of dV/dt

The slope of $V_{CE}$ from 30V to 90V (attached figure.1)

$$dv/dt = (90V - 30V) / (\Delta t)$$

= $60V / \Delta t$

● waveform

![Waveform Diagram]

● Gate drive connection

![Gate Drive Connection Diagram]
Capacitance $C (\mu F)$

Collector-emitter voltage $V_{CE}$ (V)

Peak collector current $I_{CP}$ (A)

Main capacitance $C_M$ ($\mu F$)

Gate-emitter voltage $V_{GE}$ (V)

Minimum Gate Drive Area

Maximum Operating Area

Common emitter $V_{GE} = 0$ V

$T = 1$ MHz

$T_a = 25^\circ$C

Collector-emitter voltage $V_{CE}$ (V)

Peak collector current $I_{CP}$ (A)

$V_{CM} = 350$ V

$T_a \leq 70^\circ$C

$V_{GE} = 2.5$ V

$56 \Omega \leq R_G \leq 91 \Omega$
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