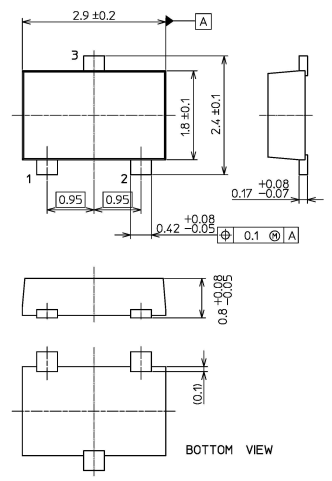
TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

SSM3K324R

○ Power Management Switch Applications

○ DC-DC Converter

Unit: mm



SOT-23F

1. Gate
2. Source
3. Drain

JEDEC	―
JEITA	―
TOSHIBA	2-3Z1A

Weight: 11 mg (typ.)

- 1.8V drive
- Low ON-resistance: $R_{DS(ON)}$ = 56 mΩ (max) (@V_{GS} = 4.5 V)
  : $R_{DS(ON)}$ = 72 mΩ (max) (@V_{GS} = 2.5 V)
  : $R_{DS(ON)}$ = 109 mΩ (max) (@V_{GS} = 1.8 V)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±12	V
Drain current	DC	I_D(Note 1)	4.0	A
	Pulse	I_{DP}(Note 1,2)	10	
Power dissipation		P_D (Note 3)	1	W
		t ≦ 10s	2	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

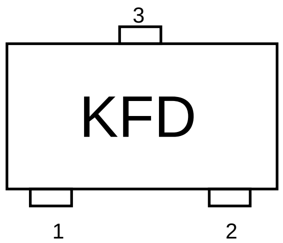
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

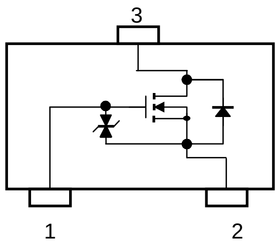
Note 2: PW≦10ms,Duty≦1%

Note 3: Mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th\ (ch\text{-}a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

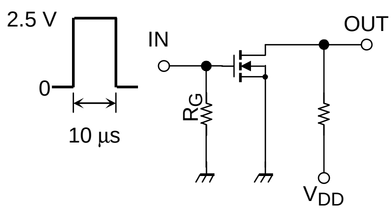
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)DSX}$	I_D = 1 mA, V_{GS} = –12 V (Note 5)	18	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 10 V, V_{DS} = 0 V	—	—	±10	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.4	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 2.0 A (Note 4)	—	10.5	—	S
Drain–source ON-resistance		$R_{DS (ON)}$	I_D = 2.0 A, V_{GS} = 4.5 V (Note 4)	—	45	56	mΩ
			I_D = 1.0 A, V_{GS} = 2.5 V (Note 4)	—	55	72	
			I_D = 0.5 A, V_{GS} = 1.8 V (Note 4)	—	69	109	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	200	—	pF
Output capacitance		C_{oss}		—	40	—	
Reverse transfer capacitance		C_{rss}		—	13	—	
Total gate charge		Q_g	V_{DS} = 10 V, I_D = 2.4 A V_{GS} = 4.5 V	—	2.2	—	nC
Gate-source charge		Q_{gs1}		—	0.5	—	
Gate-drain charge		Q_{gd}		—	0.9	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 2.0 A, V_{GS} = 0 to 2.5V, R_G = 4.7 Ω	—	9	—	ns
	Turn-off time	t_{off}		—	9.5	—	
Drain-source forward voltage		V_{DSF}	I_D = -4.0 A, V_{GS} = 0 V (Note 4)	—	-0.8	-1.2	V

Note 4: Pulse test.

Note 5: If a reverse bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

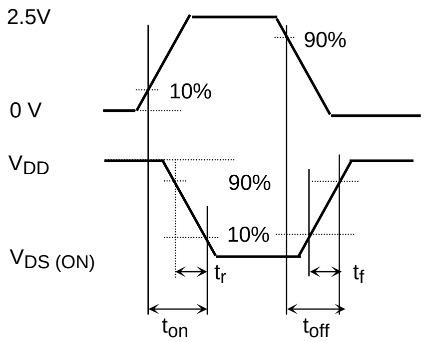
(a) Test Circuit



V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}

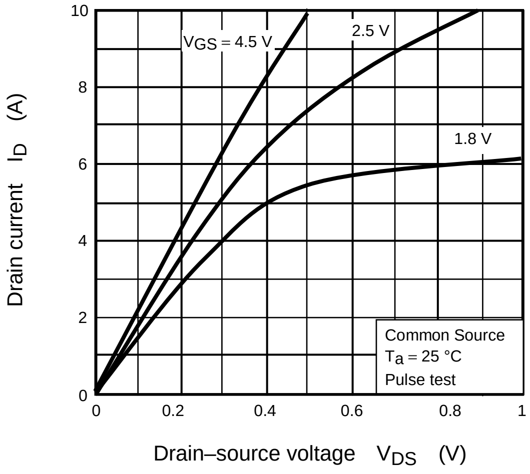


Usage Considerations

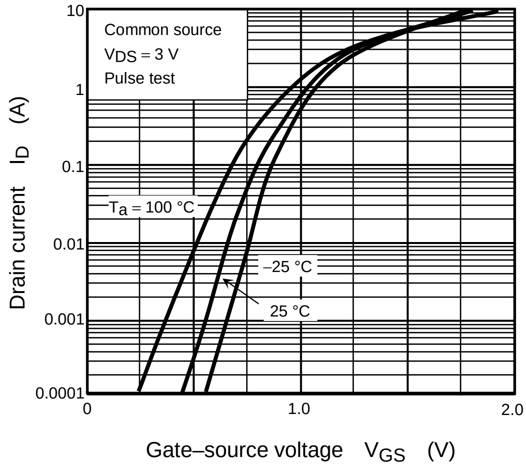
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the SSM3K324R). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th,}$ and $V_{GS(off)}$ must be lower than $V_{th.}$ This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

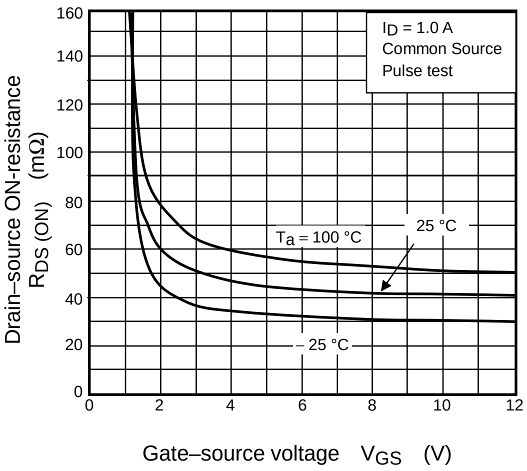
I_D – V_{DS}



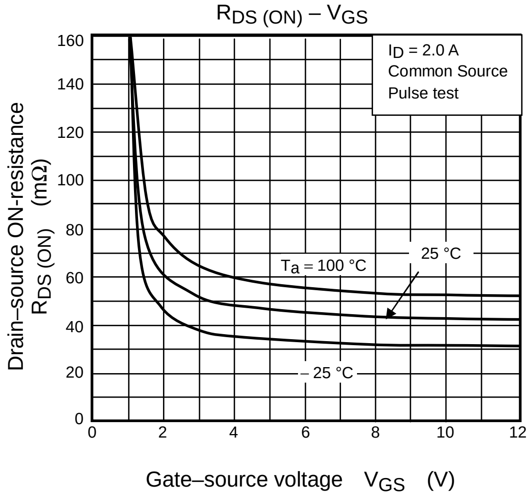
I_D – V_{GS}



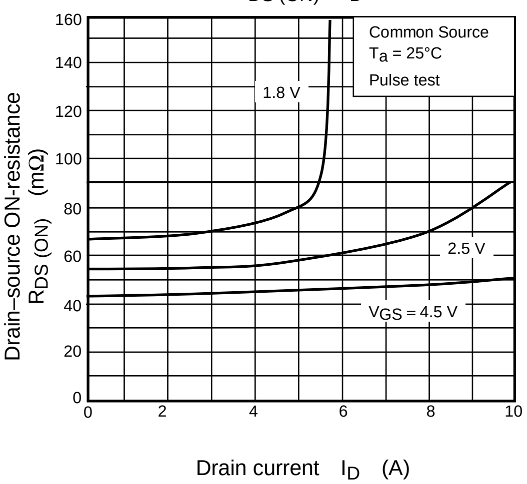
$R_{DS\ (ON)}$ – V_{GS}



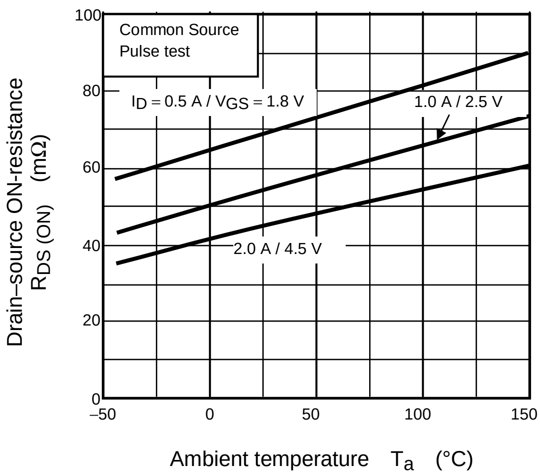
$R_{DS\ (ON)}$ – V_{GS}

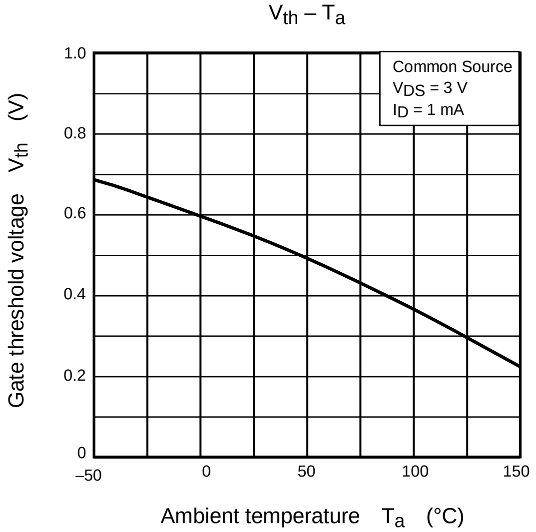


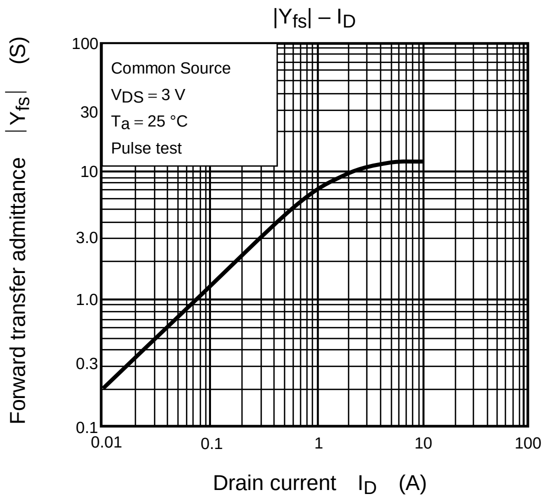
$R_{DS\ (ON)}$ – I_D

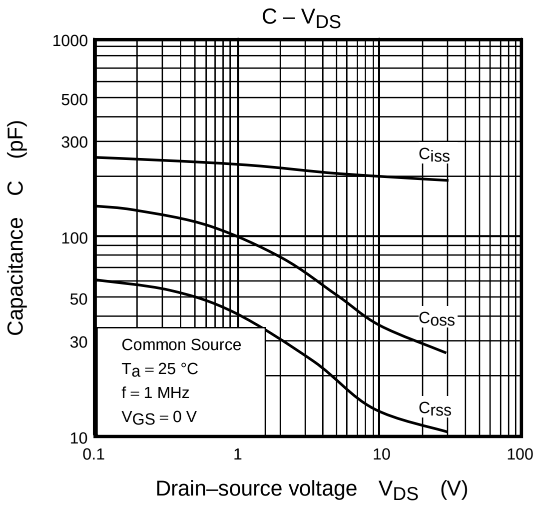


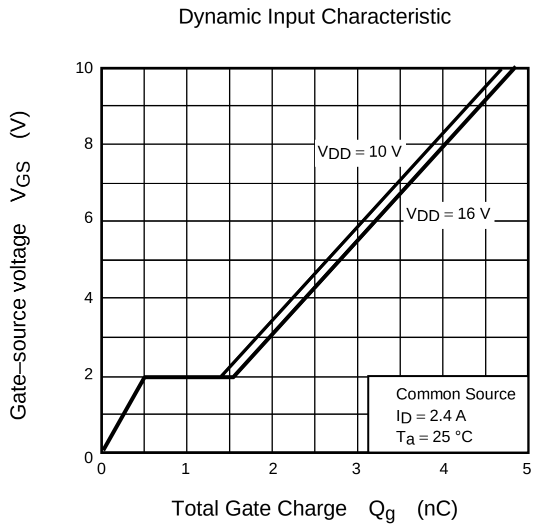
$R_{DS\ (ON)}$ – T_a

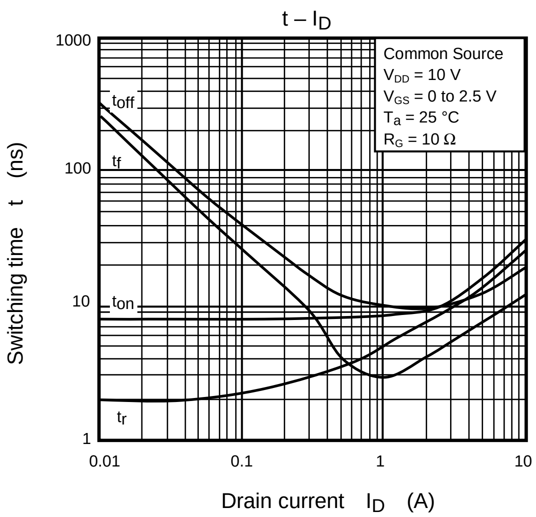


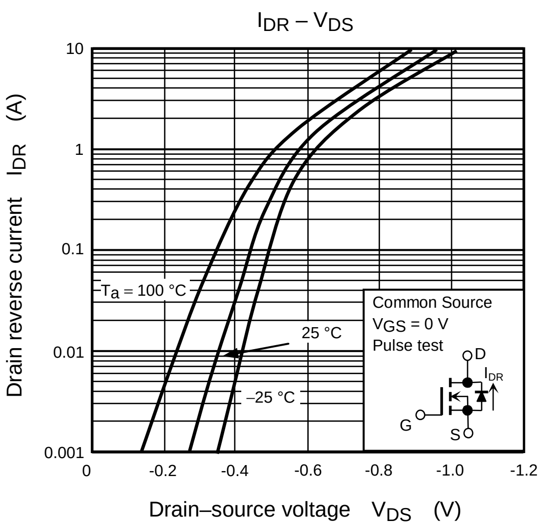

Vth – Ta
Common Source
VDS = 3 V
ID = 1 mA
Gate threshold voltage Vth (V)
Ambient temperature Ta (°C)

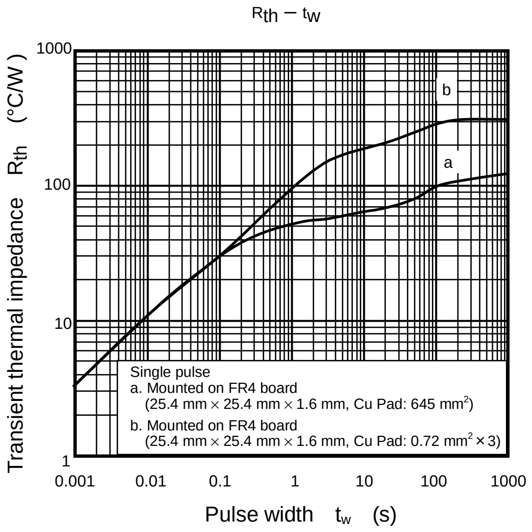

|Yfs| – ID
Common Source
VDS = 3 V
Ta = 25 °C
Pulse test
Forward transfer admittance |Yfs| (S)
Drain current ID (A)

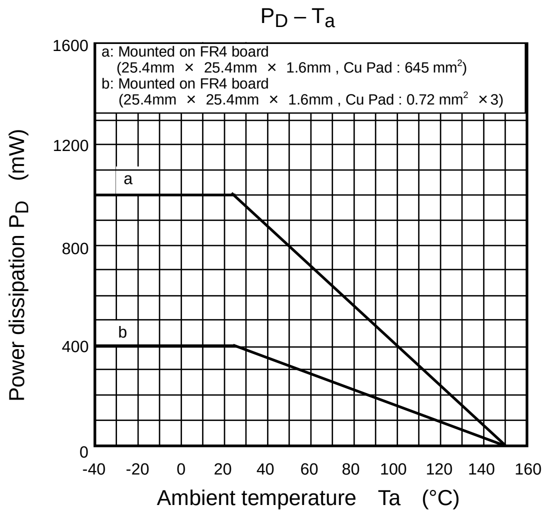

C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25 °C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
Drain–source voltage VDS (V)


Dynamic Input Characteristic
VDD = 10 V
VDD = 16 V
Common Source
ID = 2.4 A
Ta = 25 °C
Gate–source voltage VGS (V)
Total Gate Charge Qg (nC)


t – ID
Common Source
VDD = 10 V
VGS = 0 to 2.5 V
Ta = 25 °C
RG = 10 Ω
toff
tf
ton
tr
Switching time t (ns)
Drain current ID (A)


IDR – VDS
Ta = 100 °C
25 °C
−25 °C
Common Source
VGS = 0 V
Pulse test
D
IDR
G
S
Drain reverse current IDR (A)
Drain–source voltage VDS (V)


Rth – tw
Transient thermal impedance Rth (°C/W)
1000
100
10
1
0.001 0.01 0.1 1 10 100 1000
Pulse width tw (s)
b
a
Single pulse
a. Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm2)
b. Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.72 mm2 × 3)


PD – Ta
Power dissipation PD (mW)
1600
1200
800
400
0
-40 -20 0 20 40 60 80 100 120 140 160
Ambient temperature Ta (°C)
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 645 mm2)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 0.72 mm2 × 3)
a
b

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