Product Update

Errata to Z8 Encore!® 8K Series Silicon

Z8 Encore!® 8K Series Silicon with Date Codes 0402 and Later

The errata listed in Table 1 are found in the Z8 Encore!® 8K Series devices with date codes 0402 and later, where the date code is YYWW (year and week of assembly). When reviewing the following errata, it is recommended that users also download the most recent version of the Product Specification. Data contained in this document is **PRELIMINARY** only. For older devices in this product family, refer to the following pages for information.

Table 1. Z8 Encore!® 8K Series Errata for Devices with Date Codes 0402 and Later

No.	Summary	Detailed Description
1	Read Protect Option Bit may be bypassed	Error: The Read Protect (RP) Option Bit does not prevent Flash access when bypassing the Flash Controller as described in ZiLOG Application Note AN0017 entitled *Third Party Flash Programming Support of the Z8 Encore!® MCU*. User code cannot be read through the On-Chip Debugger when read protect is enabled. User code can only be read out when bypassing the Flash Controller. Work-Around: None

Z8 Encore!® 8K Series Silicon with Date Codes Prior to 0402

The errata listed in Table 2 on pages 2–4 are found in the production Z8 Encore!® 8K Series devices with date codes prior to 0402, where the date code is YYWW (year and week of assembly). When reviewing the following errata, it is recommended that users also download the most recent version of the Product Specification, available from www.zilog.com.

Table 2. Z8 Encore!® 8K Series Silicon Errata for Devices with Date Codes Prior to 0402

No.	Summary	Detailed Description
1	When the CPU exits from Halt mode, it fails to reset the master Interrupt Request Enable (IRQE) bit.	Error: When the CPU exits from HALT mode, it fails to reset the master Interrupt Request Enable (IRQE) bit (bit 7 of the Interrupt Control Register). WDT interrupts cause the Program Counter (PC) and Flags to be pushed twice on the stack. The first push is the PC and Flags from where the interrupt occurred. The second push is the starting address and Flags of the Interrupt Service Routine (ISR). This problem also affects exits from HALT mode caused by other interrupt sources if more than one interrupt is pending. If only a single interrupt is pending then the routine executes normally except that interrupts are not disabled. Work-Around: To mimic standard interrupt operation, the ISR executes a Disable Interrupts (DI) instruction to reset the master Interrupt Request Enable (IRQE) bit to 0. Further, on WDT interrupts before exiting, the ISR adds three (3) to the Stack Pointer (SP). On Normal interrupts the ISR checks the Program Counter on the stack. If the PC on the stack contains the starting address of the ISR, then the ISR adds three (3) to the Stack Pointer (SP). This problem only affects exits from HALT mode.
2	On-Chip Debugger does not support hardware breakpoints.	Error: The On-Chip Debugger does not break when the Program Counter (PC) equals the value written to the OCD Counter Register or when the OCD Counter decrements to zero. Work-Around: The other breakpoint functions available from the On-Chip Debugger can be used to for debug operations.
3	System Reset latency may exceed specification limits.	Error: When exiting STOP mode and after a POR/VBO reset, the System Reset Latency is 514 WDT cycles plus 16 System Clock cycles rather than the 66 WDT cycles plus 16 System Clock cycles as specified. Work-Around: None. This error is unlikely to affect system operation.
4	UART NEWFRM status bit does not function.	Error: The NEWFRM status bit (Bit 2 of the UART Status 1 register) does not indicate the start of a new frame. Work-Around: None.

Table 2. Z8 Encore!® 8K Series Silicon Errata for Devices with Date Codes Prior to 0402

No.	Summary	Detailed Description
5	UART Address Compare function does not work.	Error: Setting Bit 7 (MPMD[1]) of the UART Control 1 register to 1 does not produce the desired effect of enabling the UART Address Compare and associated interrupt functionality. Work-Around: MPMD[1] must be left in its reset state of 0.
6	UART Baud Rate Generator cannot be used as simple timer.	Error: Setting BRGCTL (Bit 2 of the UART Control 1 register) to 1 when the UART receiver is disabled does not enable UART Baud Rate Generator interrupt. Thus, the UART Baud Rate Generator cannot be used as a simple timer. Work-Around: Use one of the 4 standard Timers or the Baud Rate Generators in the SPI or I^2C blocks to perform the desired timing operations.
7	Unlocking the Flash Controller allows program and erase operations on all Flash pages.	Error: During the Flash Controller unlock sequence, the specification indicates that a second write to the Flash Page Select register is required (step 5 of the sequence) to unlock the Flash Controller for the selected Flash page. The Flash controller unlocks for all Flash pages once steps 1-4 of the unlock sequence have been completed. Work-Around: None.
8	Setting bits in the Flash Sector Protect register to 1 does not lock sectors.	Error: Writing bits in the Flash Sector Protect register to 1 fails to prevent program and erase operations on the selected Flash memory sector. Work-Around: None.
9	Watch-Dog Timer cannot be disabled in STOP mode.	Error: The Watch-Dog Timer and its associated internal RC oscillator cannot be disabled in STOP mode. Work-Around: None.
10	Watch-Dog Timer oscillator frequency is out of specification.	Error: The typical Watch-Dog Timer internal oscillator frequency is 50KHz rather than the currently specified 10KHz. This frequency can result in WDT timeout values that are less than expected. Work-Around: Increase the WDT reload value by a factor of 5 to compensate for the frequency error.

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No.	Summary	Detailed Description
11	Operating currents.	Error: Operating currents in the various mode (Normal, HALT, and STOP) may be higher than typical values. Work-Around: None.
12	$\overline{\text{RESET}}$ pin is not filtered.	Error: The $\overline{\text{RESET}}$ pin does not properly filter the input signal. The device may enter Reset when the $\overline{\text{RESET}}$ pin is asserted for less than the specified 4 system clock cycles (from Normal mode). Work-Around: Add external filtering to the printed-circuit board.
13	Timers can not be cascaded.	Error: Setting the CSC bit (Bit 4) of the Timer Control 0 Registers does not cascade the timers as indicated by the spec. Work-Around: Timers can be cascaded using the Timer Out and Timer In functions using the general-purpose I/O pins.

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