

PCN Number: UMC OCT14
Chgnot.doc rev 13 1/14

Product/Process Change Notification (PCN)

Customer: DIGI KEY

Date:

Customer Part # and/or Lot# affected: A3903EEETR-T

Originator: J.Hurley

Phone: 508-854-5431

Duration of Change:

Permanent Temporary (explain)

Summary description of change: Part Change: Process Change: Other:

Allegro currently manufactures the A3903EEETR-T at wafer fab, Polar Semiconductor Inc. (PSI), Bloomington, MN, USA using ABCD4 technology. We will add a second source wafer fab known as United Microelectronics Corporation (UMC), Hsinshu, Taiwan using ABCD4 technology.

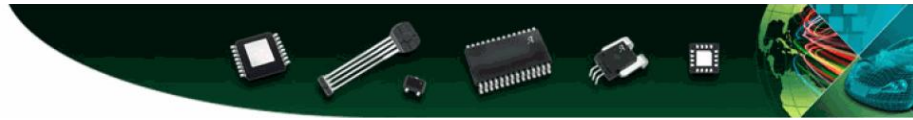
What is the part or process changing from (provide details)?

Allegro currently manufactures the A3903EEETR-T at wafer fab, Polar Semiconductor Inc. (PSI), Bloomington, MN, USA using ABCD4 technology.

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

The A3903EEETR-T will have a second source wafer fab known as United Microelectronics Corporation (UMC), Hsinshu, Taiwan using ABCD4 technology.

Note: Validation of equivalence within a specific application is at the discretion of the Customer.



PCN Number:
Chgnot.doc rev 13 1/14

Is a PPAP update required? Yes No

Is reliability testing required? (If Yes, refer to attached plan) Yes No (explain)

Device: 3903 (7803W)
Fab Location: UMC
Assy Lot #: 14303636L, 1424887QXAA
Package: EJ (MLP), EE (MLP)

Number of Leads: 10
Assembly Location: Carsem
Lead Finish: 100% Sn
Tracking Number: STR#2714, 2722

Reason For Qualification: 3903 (7803) - Low Voltage DC Motor Driver

Reliability Qualification Results						
3903 (7803), STR#2714, 2722					Requirements	
Stress Test	Abv.	Test #	Test Method	Test Conditions	S.S.	Results
Preconditioning	PC	A1	JESD22-A113/ J-STD-020	85°C/60% RH, 168 hrs, Peak Reflow=260°C;	77	0 Rejects
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 85% RH, 0, 96 hrs	77	0 Rejects
High Temperature Operating Life	HTRB	B1	JESD22-A108	150°C, 0, 168 hrs	77	0 Rejects
Electrostatic Discharge Human Body Model	HBM	E2	JESD22-A114	Test Conditions, Sampling Size are defined in the Test Method		Classification H2, HBM =2.5 kV
Electrostatic Discharge Charged Device Model	CDM	E3	JESD22-C101	Test Conditions, Sampling Size are defined in the Test Method		Classification = IV, > 1kV
Latch-Up	LU	E4	AEC Q100- 004	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A
Electrical Distributions	ED	E5	AEC Q100- 009	Tri-Temp Electrical Distributions (3 lots)	30 pcs/lot	0 Rejects; Cpk>1.67

This device qualification is considered to be passing all environmental stress evaluations per the *Allegro MicroSystems, LLC*. 900019 specification and JEDEC JESD47.
Approved by:

Expected completion date for internal qualification: Complete

Expected PPAP availability date: N/A

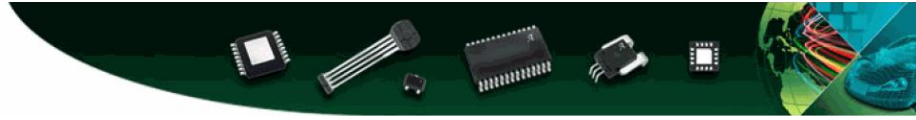
Target implementation date: March 2015

Estimated date of first shipment: April 2015

Expected sample availability date: Available Now

Customer Approval Required: Yes Date Required:

No Notification Only



Please note: It is our intention to inform our customer of changes as early as possible. Under Allegro's procedure for product/process change notification, Allegro strives, based on its technical judgment, to provide notification of significant changes that may affect form, fit or function. However, as Allegro cannot ensure evaluation of product/process changes for each and every application; the customer retains responsibility to validate the impact of a change on its application suitability. If samples are needed for validation of a change, requests may be made via the contact information provided herein. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled.

Customer comments/Conditions of Acceptance:

Approved by:

Date:

Title:

cc: Allegro Sales/Marketing/Quality