

**Product Change Notification - SYST-03ZZQY339**


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**Date:**

04 Feb 2020

**Product Category:**

32-bit Microcontrollers

**Affected CPNs:**

**Notification subject:**

Data Sheet - SAM D21/DA1 Family Data Sheet

**Notification text:**

SYST-03ZZQY339

 Microchip has released a new Product Documents for the SAM D21/DA1 Family Data Sheet of devices. If you are using one of these devices please read the document located at [SAM D21/DA1 Family Data Sheet](#).

**Notification Status:** Final

**Description of Change:**

Section	Description
<a href="#">Block Diagram</a>	Added arrow between PORT and AHB-APB BRIDGE B.
<a href="#">Pinout</a>	Updated section titles
<a href="#">Product Mapping</a>	Updated the diagram to show the Internal Flash.
<a href="#">PORT I/O Pin Controller</a>	Corrected the <a href="#">WRCONFIG</a> register to show the DRVSTR bit.
<a href="#">SERCOM</a>	Under <a href="#">Clock Generation - Baud-Rate Generator</a> , the <a href="#">table</a> was updated with a new information and equations.
<a href="#">SERCOM USART</a>	<ul style="list-style-type: none"> <li>&amp;bull; Information regarding FIFO was removed as it is not supported on this device</li> <li>&amp;bull; The FIFOCLR bit was removed from the CTRLB register</li> <li>&amp;bull; The FIFOSPACE and FIFOPTR registers were removed</li> </ul>
<a href="#">SERCOM SPI</a>	<ul style="list-style-type: none"> <li>&amp;bull; Information on FIFO was removed as it is not supported on this device</li> <li>&amp;bull; The FIFOCLR bit was removed from the <a href="#">CTRLB</a> register</li> <li>&amp;bull; The FIFOSPACE and FIFOPTR registers were removed</li> </ul>
<a href="#">SERCOM I2C</a>	<ul style="list-style-type: none"> <li>&amp;bull; Information on FIFO was removed as it is not supported on this device</li> <li>&amp;bull; The FIFOCLR bit was removed from the <a href="#">CTRLB</a> Slave Register</li> <li>&amp;bull; Bit fields RXFF and TXFE were removed from the <a href="#">INTENCLR</a>, <a href="#">INTENSET</a>, and <a href="#">INTFLAG</a> Slave Registers</li> <li>&amp;bull; The LENERR bit was removed from the <a href="#">STATUS</a> Slave Register</li> <li>&amp;bull; Registers FIFOSPACE and FIFOPTR were removed from the Slave Registers</li> <li>&amp;bull; The FIFOCLR bit was removed from the <a href="#">CTRLB</a> Master Register</li> <li>&amp;bull; Bit fields, RXFF and TXFE, were removed from the <a href="#">INTENCLR</a>, <a href="#">INTENSET</a>, and <a href="#">INTFLAG</a> Master Registers</li> <li>&amp;bull; Registers FIFOSPACE and FIFOPTR were removed from the Master Registers</li> </ul>

Timer Counter (TC)	<ul style="list-style-type: none"> <li>In <a href="#">Counter Mode</a>, <a href="#">Count32</a> was updated with new TC numbering</li> <li>The register summaries for <a href="#">8-bit Mode</a>, <a href="#">16-bit Mode</a>, and <a href="#">32-bit Mode</a> were updated to correctly display</li> </ul>
TCC	<ul style="list-style-type: none"> <li><a href="#">FCTRLA</a> and <a href="#">FCTRLB</a> had their naming corrected</li> <li>In the <a href="#">WEXCTRL</a> register the DTIEN bit had the numbering updated</li> <li>In the <a href="#">DRVCTRL</a> register the numbering was updated for the INVENx, NRVx, and NREx bits</li> <li>In the <a href="#">EVCTRL</a> register the numbering was updated for the MCEOx, MCEIx, TCEIx, and TCINVx Registers</li> <li>In the <a href="#">INTENCLR</a>, <a href="#">INTENSET</a>, and <a href="#">INTFLAG</a> registers the numbering was updated for the MCx bit</li> <li>In the <a href="#">STATUS</a> register the numbering was updated for the CMPx and FAULTx bits</li> <li>The <a href="#">PATT</a> register was updated to properly display the PGVx and PGEEx bits</li> <li>The <a href="#">PATTB</a> register was updated to properly display the PGVBx and PGEEx bits</li> </ul>
USB	Updated cross references.
ADC	Updated the MUXPOS Bit table in the <a href="#">INPUTCTRL</a> register.
AC	<ul style="list-style-type: none"> <li>Updated the STARTx bit numbering in the <a href="#">CTRLB</a> register</li> <li>Updated the bit numbering for the COMPEIx, COMPEOx, and WINEOx bits in the <a href="#">EVCTRL</a> register</li> <li>Updated the bit numbering for the WINx, and COMPx bits in the <a href="#">INTENCLR</a>, <a href="#">INTENSET</a>, and <a href="#">INTFLAG</a> registers</li> <li>Updated the bit numbering for the WSTATEx and STATEx bits in the <a href="#">STATUSA</a> register</li> <li>Updated the bit numbering for the READYx bit in the <a href="#">STATUSB</a> register</li> <li>Updated the bit numbering for the WSTATEx and STATEx bits in the <a href="#">STATUSC</a> register</li> <li>Updated the bit numbering for the WINTSELx and WENx bits in the <a href="#">WINCTRL</a> register</li> </ul>
<a href="#">SAM DA1 Electrical Characteristics</a>	This section was migrated into this data sheet from the original SAM DA1 data sheet.
<a href="#">Schematic Checklist</a>	Updated <a href="#">External Reset Circuit</a> with changes to the diagram <a href="#">External Reset Circuit Schematic</a> .
<a href="#">Packaging Information</a>	Updated <a href="#">Package Markings</a> with a new marking diagram.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Manufacturability

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 04 Feb 2020

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.



**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachment(s):**

[SAM D21/DA1 Family Data Sheet](#)

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Affected Catalog Part Numbers (CPN)

ATSAMD21E17D-MZ  
ATSAMD21E17D-MZVAO  
ATSAMD21E17L-MF  
ATSAMD21E17D-MF  
ATSAMD21G17D-MF  
ATSAMD21G17L-MF  
ATSAMD21E17L-AF  
ATSAMD21E17D-AF  
ATSAMD21E17D-AZ  
ATSAMD21J17D-MF  
ATSAMD21G17D-MZ  
ATSAMD21J17D-MZ  
ATSAMD21J17D-AF  
ATSAMD21J17D-AZ  
ATSAMD21J17D-AZVAO  
ATSAMD21G17D-AF  
ATSAMD21G17D-AZ  
ATSAMD21J17D-CU  
ATSAMD21E17D-MU  
ATSAMD21G17D-MU  
ATSAMD21G17L-MU  
ATSAMD21E17D-AU  
ATSAMD21J17D-MU  
ATSAMD21J17D-AU  
ATSAMD21G17D-AU  
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