Customer Information Notification

202102038I : i.MX 8M Nano Consumer and Industrial Datasheet Update to Rev.1 and Errata Update to Rev.1

Note: This notice is NXP Company Proprietary.

Issue Date: Apr 30, 2021 **Effective date:May 01, 2021**

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Change Category

[ ]Wafer Fab Process	[ ]Assembly Process	[ ]Product Marking	[ ]Test Process	[ ]Design
[ ]Wafer Fab Materials	[ ]Assembly Materials	[ ]Mechanical Specification	[ ]Test Equipment	[X]Errata
[ ]Wafer Fab Location	[ ]Assembly Location	[ ]Packing/Shipping/Labeling	[ ]Test Location	[X]Electrical spec./Test coverage
[ ]Firmware	[ ]Other			

PCN Overview

Description

NXP Semiconductors announces Industrial and Consumer Datasheet (DS) update for i.MX 8M Nano to revision 1 and Errata update for i.MX 8M Nano to revision 1. The revision history included in the updated document provides a detailed description of the changes.
Industrial and Consumer Datasheet Changes Summary:
Highlighted Changes:
01. Updated the title and the maximum values of VDD_ARM_PLL_0P8 and VDD_USB_0P8 in the Table 10, "Absolute maximum ratings for 14 x 14 mm package”
02. Updated the VDD_ANA_0P8, VDD_ARM_PLL_0P8, VDD_MIPI_0P8, VDD_USB_0P8, and USB1_VBUS in the Table 15, "Operating ranges for 14 x 14 mm package"; added footnotes in the Table 15, "Operating ranges for 14 x 14 mm package“
03. Updated the lock time, ARM_PLL, and GPU values in the Table 30, "PLL electrical parameters”; added M7_ALT_PLL in the Table 30, "PLL electrical parameters”
04. Updated and added Low-V suspend mode data in the Table 21, "Chip power in different LP mode for 14 x 14 mm package”
Pls refer the change summary for other changes.
There is a new package 11x11mm FCBGA306 adding in the new datasheet, pls refer datasheet for details.

The i.MX 8M Nano Industrial and Consumer Datasheet Rev.1 are attached to this notice, and can be

found at:
https://www.nxp.com/docs/en/data-sheet/IMX8MNIEC.pdf
https://www.nxp.com/docs/en/data-sheet/IMX8MNCEC.pdf

Errata changes Summary for i.MX 8M Nano.
4 new items are added:
ERR050144: SAI: Setting FCONT=1 when TMR>0 may not function correctly
ERR050447: [SPDIF]: SPDIF clock limitation
ERR050537: FlexSPI: Read timing sequence mismatches with several existing SPI NOR devices in dual, quad, and octal modes
ERR050542: SAI: The Bit Count Timestamp Register (TBCTR, RBCTR) may return a live rather than latched Timestamp
Please refer to the Errara doc for detail information.

The i.MX 8M Nano Errata Rev.1 can be found at:
https://www.nxp.com/docs/en/errata/IMX8MN_0N14Y.pdf
Reason
Datasheet has been updated to correct errors and provide additional technical clarification on some device features.
Errata has been updated with 4 additional items, and provided related workarounds.
Identification of Affected Products
Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No Impact on form, fit, function, reliability or quality
Data Sheet Revision
A new datasheet will be issued

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For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

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NXP Quality Management Team.
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