


PCN Number:	20180712001.1		PCN Date:	Jul 16, 2018	
Title:	Qualification of DMOS6 as an additional Fab site and Assembly material change at UTL1 for select devices				
Customer Contact:	PCN Manager		Dept:	Quality Services	
Proposed 1st Ship Date:	Oct 16, 2018		Estimated Sample Availability:	Date Provided at Sample request	
Change Type:					
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site	<input checked="" type="checkbox"/>	Wafer Fab Site
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input checked="" type="checkbox"/>	Wafer Fab Materials
				<input type="checkbox"/>	Wafer Fab Process
PCN Details					
Description of Change:					
This change notification is to announce the addition of DMOS6 as an additional Fab site and Assembly material change at UTL1 for select devices. Material differences as follows.					
Fab Site:					
Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter
DP1DM5	LBC8LV	200mm	DMOS6	LBC8LV	300mm
Material change:					
		From	To		
	Mount compound	PZ0037	PZ0076		
	Mold compound	CZ0141	CZ0288		
Reason for Change:					
Continuity of supply.					
Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):					
None					
Anticipated impact on Material Declaration					
<input type="checkbox"/>	No Impact to the Material Declaration	<input checked="" type="checkbox"/>	Material Declarations or Product Content reports are driven from production data and will be available following the production release. Upon production release the revised reports can be obtained from the TI Eco-Info website . There is no impact to the material meeting current regulatory compliance requirements with this PCN change.		
Changes to product identification resulting from this PCN:					
Fab Site change:					
Current:					
Current Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City		
DP1DM5	DM5	USA	Dallas		
New Fab Site:					
New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City		
DMOS6	DM6	USA	Dallas		

Sample Product Shipping Label (not actual product label)


TEXAS INSTRUMENTS
 MADE IN: Malaysia
 2DC: 2Q:

MSL 2 / 260C/1 YEAR	SEAL DT
MSL 1 / 235C/UNLIM	03/29/04

 OPT:
 ITEM: 39
LBL: 5A (L)T0:1750



(1P) SN74LS07NSR
 (Q) 2000 (D) 0336
 (31T) LOT: 3959047MLA
 (4W) TKY (1T) 7523483SI2
 (P)
 (2P) REV: (V) 0033317
 (20L) CSO: SHE (21L) CCO: USA
 (22L) ASO: MLA (23L) ACO: MYS

Product Affected:

TMP451AIDQFR	TMP451CIDQFR	TMP451EIDQFR	TMP451GIDQFR
TMP451AIDQFT	TMP451CIDQFT	TMP451EIDQFT	TMP451GIDQFT
TMP451BIDQFR	TMP451DIDQFR	TMP451FIDQFR	
TMP451BIDQFT	TMP451DIDQFT	TMP451FIDQFT	

Qualification Report

TMP451 RFAB/DMOS6-UTAC QUALIFICATION

Approve Date: 07/11/2018

Product Attributes

Attributes	Qual Device: <u>TMP451AIDQF</u>	QBS Process Reference: <u>TAS2553YFF</u>
Assembly Site	UTAC	CLARK-AT
Package Family	SON	DSBGA
Flammability Rating	UL 94 V-0	UL 94 V-0
Wafer Fab Supplier	RFAB / DMOS6 (MFF)	RFAB/DMOS6 (MFF)
Wafer Process	LBC8LV	LBC8LV

- QBS: Qual By Similarity
- Qual Device TMP451AIDQF is qualified at LEVEL1-260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: <u>TMP451AIDQF</u>	QBS Process Reference: <u>TAS2553YFF</u>
HTOL	High Temp Operating Life	125C 1000 Hours	1/77/0	3/231/0
HTSL	High Temp Storage Bake 170C	420 Hours	3/231/0	-
HAST	Biased HAST, 110C/85%RH	264 Hours	3/231/0	-
TC	Temperature Cycle, -65/150C	500 Cycles	3/231/0	-
UFAST	Unbiased HAST 110C/85%RH	264 Hours	3/231/0	-
CDM	ESD - CDM	1500 V	1/3/0	-
HBM	ESD - HBM	4000 V	1/3/0	-
LU	Latch-up	(per JESD78)	1/6/0	-
PD	Physical Dimensions	-	3/15/0	-
SD	Surface Mount Solderability (Pb Free)	8 Hours Steam Age	3/66/0	-
SD	Surface Mount Solderability (Pb)	8 Hours Steam Age	3/66/0	-
WBP	Bond Pull	Wires	3/90/0	-
WBS	Ball Bond Shear	Wires	3/90/0	-

Type	Test Name / Condition	Duration	Qual Device: <u>TMP451AIDQF</u>	QBS Process Reference: <u>TAS2553YFF</u>
ED	Electrical Characterization	Per Datasheet Parameters	1/30/0	-
BLR	BLR-Temp Cycle, -40C/125C	2000 Cycles	1/32/0	-

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Green/Pb-free Status: Qualified Pb-Free(SMT) and Green

THIS INFORMATION RELATING TO QUALITY AND RELIABILITY IS PROVIDED "AS IS." Product information detailed in this report may not accurately reflect TI's current product materials, processes and testing used in the construction of the TI products. Customers are solely responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications. Using TI products outside limits stated in TI's datasheet may void TI's warranty. See TI's Terms of Sale at "<http://www.ti.com/llds/ti/legal/termsofsale.page>"

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