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Product Information Notification

PIN

Product Group: SIL/Thu Jun 8, 2023/PIN-SIL-000511-2023-REV-0

SiC461/2/3/4 & SiC471/2/3/4 Datasheet Update

For further information, please contact your regional Vishay office.

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Description of Change: Enable pin internal resistance.

Classification of Change: New characterization data showed that the distribution limits moved, and therefore the change of datasheet limits

Expected Influence on Quality/Reliability/Performance: There will be no effect on performance, quality or reliability.

Part Numbers/Series/Families Affected: Please see materials list on the succeeding page.

Vishay Brand(S): Vishay Siliconix

Time Schedule:

Start Shipment Date: Mon Aug 14, 2023

Sample Availability: Samples are available now

Product Identification: Lot Number and Country of Origin

Qualification Data: Available upon Request

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SIC461ED-T1-GE3	SIC462ED-T1-GE3	SIC463ED-T1-GE3	SIC464ED-T1-GE3	SiC471ED-T1-GE3
SiC472ED-T1-GE3	SiC473ED-T1-GE3	SiC474ED-T1-GE3		

Data Sheet comparison

June 2023

Old Version

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, V_{EN} = 5 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fault Protections						
Valley current limit	I_{OCP}	SiC461 (10 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	10.4	13	15.6	A
		SiC462 (6 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	6.4	8	9.6	
		SiC463 (4 A), R_{ILIM} = 40 kΩ, T_J = -10 °C to +125 °C (2)	4.8	6	7.2	
		SiC464 (2 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	3.2	4	4.8	
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	50	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		-	1.35	-	V
EN logic low level	V_{EN_L}		-	1.2	-	
EN hysteresis	V_{HYST}		-	0.15	-	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Ultrasonic mode high Level	$V_{ULTRASONIC\_H}$		2	-	-	V
Ultrasonic mode low level	$V_{ULTRASONIC\_L}$		-	-	0.8	
Mode pull up current	I_{MODE}		3.75	5	6.25	µA
Mode 1	R_{MODE}	Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	2	100	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	494	499	504	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	900	1000	1100	

Notes

(1) Guaranteed by design

(2) Guaranteed by design for SiC463 OCP measurements

NEW Version

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, V_{EN} = 5 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fault Protections						
Valley current limit	I_{OCP}	SiC461 (10 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	10.4	13	15.6	A
		SiC462 (6 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	6.4	8	9.6	
		SiC463 (4 A), R_{ILIM} = 40 kΩ, T_J = -10 °C to +125 °C (2)	4.8	6	7.2	
		SiC464 (2 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	3.2	4	4.8	
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	50	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		-	1.35	-	V
EN logic low level	V_{EN_L}		-	1.2	-	
EN hysteresis	V_{HYST}		-	0.15	-	
EN pull down resistance	R_{EN}		5	7	9	MΩ
Ultrasonic mode high Level	$V_{ULTRASONIC\_H}$		2	-	-	V
Ultrasonic mode low level	$V_{ULTRASONIC\_L}$		-	-	0.8	
Mode pull up current	I_{MODE}		3.75	5	6.25	µA
Mode 1	R_{MODE}	Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	2	100	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	494	499	504	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	900	1000	1100	

Notes

(1) Guaranteed by design

(2) Guaranteed by design for SiC463 OCP measurements

Old Version

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, V_{EN} = 5 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fault Protections						
Valley current limit	I_{OCP}	SiC471 (12 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	12	15	18	A
		SiC472 (8 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	8	10	12	
		SiC473 (5 A), R_{ILIM} = 43 kΩ, T_J = -10 °C to +125 °C (2)	5.6	7	8.4	
		SiC474 (3 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	4	5	6	
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	50	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		-	1.35	-	V
EN logic low level	V_{EN_L}		-	1.2	-	
EN hysteresis	V_{HYST}		-	0.15	-	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Ultrasonic mode high Level	$V_{ULTRASONIC\_H}$		2	-	-	V
Ultrasonic mode low level	$V_{ULTRASONIC\_L}$		-	-	0.8	
Mode pull up current	I_{MODE}		3.75	5	6.25	µA
Mode 1	R_{MODE}	Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	2	100	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	494	499	504	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	900	1000	1100	

Notes

(1) Guaranteed by design

(2) Guaranteed by design for SiC473 OCP measurements

NEW Version

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, V_{EN} = 5 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fault Protections						
Valley current limit	I_{OCP}	SiC471 (12 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	12	15	18	A
		SiC472 (8 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	8	10	12	
		SiC473 (5 A), R_{ILIM} = 43 kΩ, T_J = -10 °C to +125 °C (2)	5.6	7	8.4	
		SiC474 (3 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	4	5	6	
Output OVP threshold	V_{OVP}	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	V_{UVP}		-	-80	-	
Over temperature protection	T_{OTP_RISING}	Rising temperature	-	150	-	°C
	T_{OTP_HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	V_{FB_HYST}		-	50	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		-	1.35	-	V
EN logic low level	V_{EN_L}		-	1.2	-	
EN hysteresis	V_{HYST}		-	0.15	-	
EN pull down resistance	R_{EN}		5	7	9	MΩ
Ultrasonic mode high Level	$V_{ULTRASONIC\_H}$		2	-	-	V
Ultrasonic mode low level	$V_{ULTRASONIC\_L}$		-	-	0.8	
Mode pull up current	I_{MODE}		3.75	5	6.25	µA
Mode 1	R_{MODE}	Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	2	100	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	494	499	504	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	900	1000	1100	

Notes

(1) Guaranteed by design

(2) Guaranteed by design for SiC473 OCP measurements